Renesas Electronics America Inc - R4F20203RNFD#V0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20203rnfd-v0

4.2.3 IRQ Enable Register (IER)

Address: H'FF0521

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	IRQ7E	IRQ7 enable	0: IRQ7 interrupts are disabled. 1: IRQ7 interrupts are enabled.	R/W
6	IRQ6E	IRQ6 enable	0: IRQ6 interrupts are disabled. 1: IRQ6 interrupts are enabled.	R/W
5	IRQ5E	IRQ5 enable	0: IRQ5 interrupts are disabled. 1: IRQ5 interrupts are enabled.	R/W
4	IRQ4E	IRQ4 enable	0: IRQ4 interrupts are disabled. 1: IRQ4 interrupts are enabled.	R/W
3	IRQ3E	IRQ3 enable	0: IRQ3 interrupts are disabled. 1: IRQ3 interrupts are enabled.	R/W
2	IRQ2E	IRQ2 enable	0: IRQ2 interrupts are disabled. 1: IRQ2 interrupts are enabled.	R/W
1	IRQ1E	IRQ1 enable	0: IRQ1 interrupts are disabled. 1: IRQ1 interrupts are enabled.	R/W
0	IRQ0E	IRQ0 enable	0: IRQ0 interrupts are disabled. 1: IRQ0 interrupts are enabled.	R/W

5.4.2 Trimming of High-Speed OCO

Users can trim the on-chip oscillator frequency, supplying the external reference pulses with the input capture function in the on-chip timer. An example of trimming flow using timer RC and a timing chart are shown in figures 5.15 and 5.16, respectively. Because HOTRMDR1 is initialized by a reset, when users have trimmed the oscillators, some operations after a reset are necessary, such as trimming it again or saving the trimming value in an external device for later reloading.

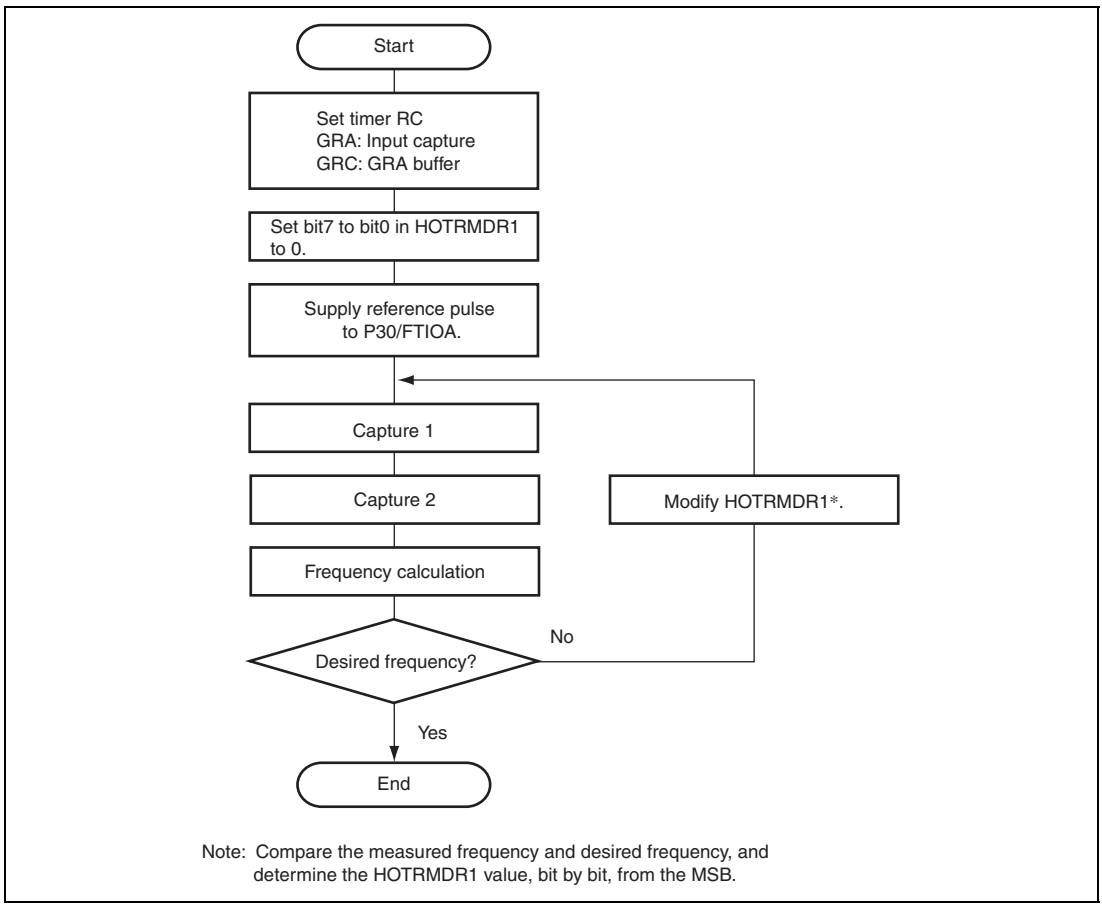


Figure 5.15 Example of Flow for Trimming High-Speed OCO Frequency

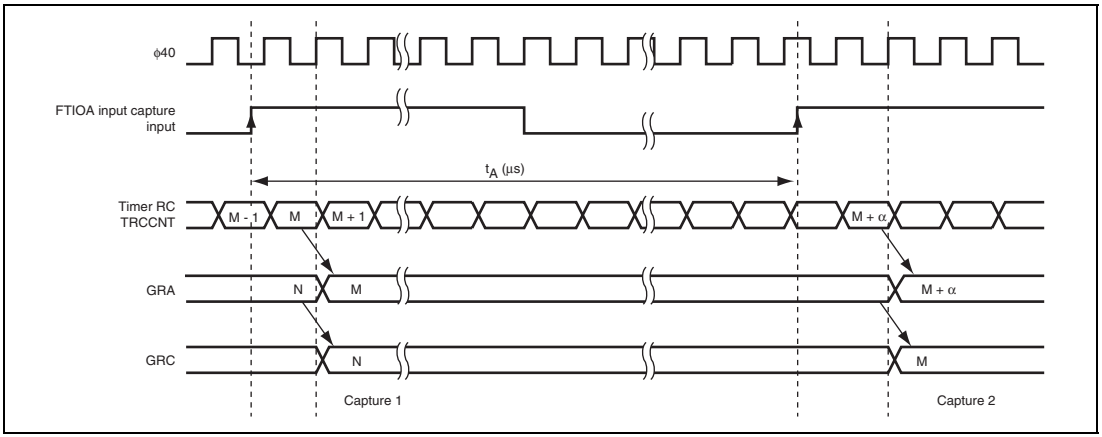


Figure 5.16 Timing Chart of Trimming of High-Speed OCO Frequency

The high-speed OCO frequency is obtained by the expression below. Since the input-capture input is sampled at the rate of the high-speed OCO, the calculated result includes a sampling error of ±1 clock cycle.

$$Foco = \frac{(M + \alpha) - M}{t_A} \text{ (MHz)}$$

Foco = High-speed OCO frequency

t_A = Cycle of reference clock (us)

M = Timer RC counter value

Note: For the H8S/20203R, H8S/20223R, H8S/20215R, and H8S/20235R Groups, timer RD should be used instead of timer RC.

6.3 Bus Master Clock Division Function

In active or sleep mode, the operating clock for the CPU, DTC, on-chip ROM, and on-chip RAM can be divided independently of the clock supplied to the peripheral modules. Using a divided clock can reduce power consumption.

The operating clock φs for the bus masters and the on-chip ROM and on-chip RAM can be selected from among φ, φ/2, φ/4, φ/8, φ/16, and φ/32 according to the PHIS[2:0] setting in LPCR3.

6.3.1 Reset States

For reset states, see section 3.3, Reset.

6.4 Module Standby Function

The module standby function is available for any peripheral module. When a module is set to the module standby state, the clock supply to the module stops placing the module in the power-down state. Setting the corresponding bit to the module in MSTCR to 1 places the module in the module standby state and clearing the bit cancels the module standby state. After release from a reset, all the modules except timer RE are in the module standby state; to use a module, cancel the module standby state of it.

Note that the registers of the module in the module standby state cannot be accessed.

6.5 PSC Divider Stop Function

When the peripheral modules do not use the PSC divider output, the PSC divider can be stopped by setting the PSCSTP bit in LPCR1 to 1.

When the PSC divider is stopped, the peripheral modules using φ/2 to φ/8192 can be stopped as shown in table 6.1 (register values are retained). Before setting the PSCSTP bit to 1, set the peripheral modules using the PSC divider output to the module standby state.

After release from a reset, the PSC divider is stopped since the PSCSTP bit is set to 1. For the PSCSTP bit, see section 5.2.3, Power-Down Control Register 1 (LPCR1).

Table 7.12 Bit Values in FLMSTR and Corresponding Errors

Bit Values in FLMSTR			
FMEBSF	**FMPRSF**	**Error**	**Error Generation Conditions**
0	0	Successful end	
0	1	Programming error	The programming command is executed and results in unsuccessful programming.
		Lock-bit programming error	The lock-bit program command is executed and results in unsuccessful programming.
1	0	Erasure error	The erasure command is executed and results in unsuccessful erasure.
		Blank checking error	The blank checking command is executed and it is detected that the specified block is not blank.
1	1	Command sequence error	• A command is not written correctly. • A data value other than H'D0 and H'FF is written in the last cycle of the command that consists of two command cycles. • The erasure command is input in erase-suspend mode. • The programming command is input for the suspended block in erase-suspend mode.

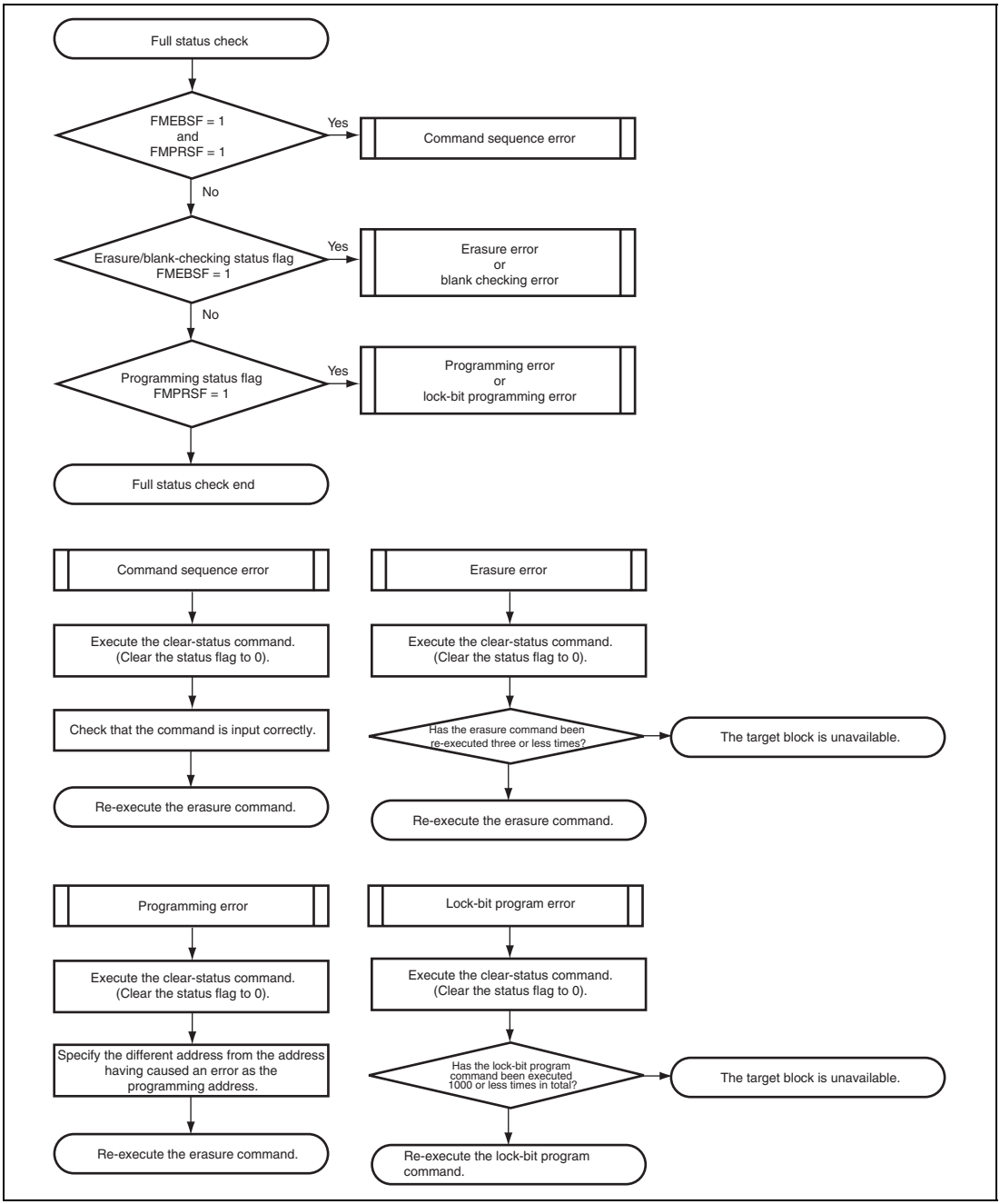


Figure 7.19 Full Status Checking Flowchart and Procedures of Handling Errors

(b) Port 6 Peripheral Function Mapping Register 2 (PMCR62)

Address: H'FF0055

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	P63MD[2:0]			—	P62MD[2:0]		
Value after reset:	0	1	0	1	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
7	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
6 to 4	P63MD[2:0]	P63 function select	000: Setting prohibited 001: $\overline{\text{IRQ3}}$ input 010: $\overline{\text{TRCOI}}$ input (timer RC)* 011: FTIOD input/output (timer RC)* 100: TGIOB input/output (timer RG) 101: FTIOD0 input/output (timer RD_0) (initial value) 110: TRAO output (timer RA) 111: Setting prohibited	R/W
3	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
2 to 0	P62MD[2:0]	P62 function select	000: Setting prohibited 001: $\overline{\text{IRQ2}}$ input 010: TXD output (SCI3) 011: FTIOC input/output (timer RC)* 100: TGIOA input/output (timer RG) 101: FTIOC0 input/output (timer RD_0) (initial value) 110: TRBO output (timer RB) 111: Setting prohibited	R/W

Note: * The timer RC is not available on the H8S/20203R, H8S/20223R, H8S/20215R, and H8S/20235R Groups. These bits are reserved and the function cannot be selected for these groups.

10.11.3 Port Pull-Up Control Register B (PUCRB)

Address: H'FF001A

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	PUCRB7	PUCRB6	PUCRB5	PUCRB4	PUCRB3	PUCRB2	PUCRB1	PUCRB0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	PUCRB7	Port B7 pull-up control	0: The pull-up MOS of corresponding pin is disabled.	R/W
6	PUCRB6	Port B6 pull-up control	1: The pull-up MOS of corresponding pin is enabled.	R/W
5	PUCRB5	Port B5 pull-up control	PUCRB is a register that controls the pull-up MOS in bit units of the pins set as the input ports.	R/W
4	PUCRB4	Port B4 pull-up control		R/W
3	PUCRB3	Port B3 pull-up control		R/W
2	PUCRB2	Port B2 pull-up control		R/W
1	PUCRB1	Port B1 pull-up control		R/W
0	PUCRB0	Port B0 pull-up control		R/W

- PUCRB7 bit to PUCRB0 bit (port B7 to B0 pull-up control)

  This function is valid only for the pin set as general input, and for the input pin with a function selected by the PMC. However, this setting is invalid for the analog input pin.

10.11.4 Notes on Using Port B

1. The PB0 pin is initially set as general I/O pin. If using this pin as the analog input pin for the A/D converter, set the PMRA2 bit in PMRA to 1.
2. Pins PB7 and PB6 can be used as analog input pins for the A/D converter or analog output pins for the D/A converter. Do not set these pins as analog input pins and analog output pins at the same time.

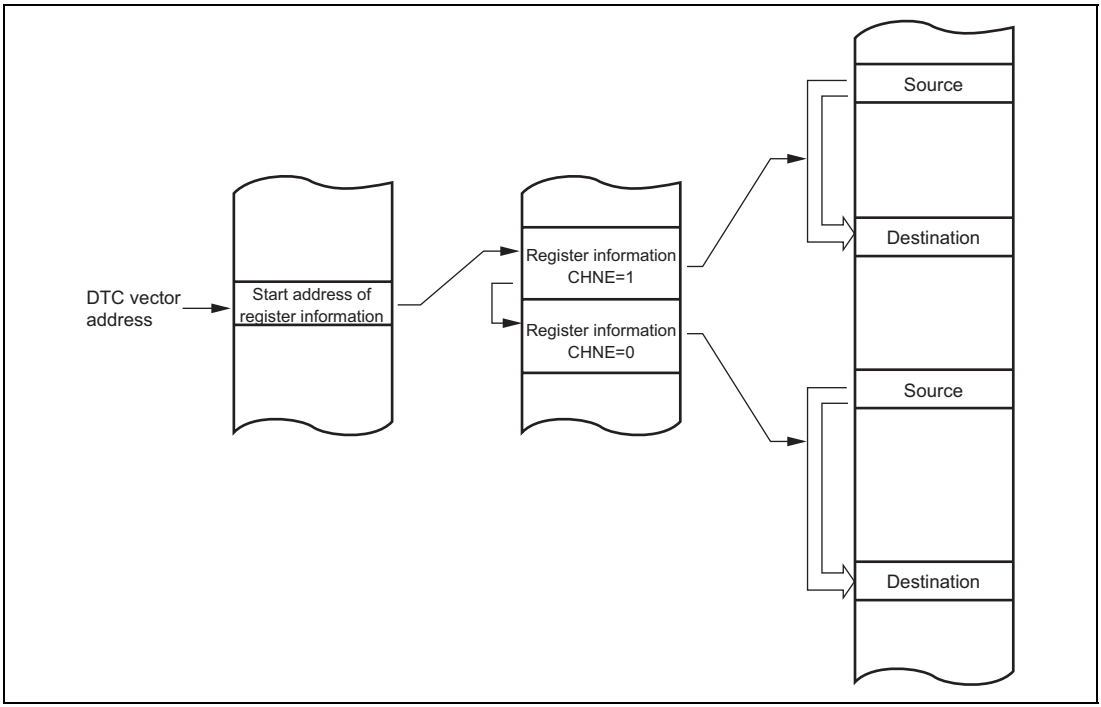


Figure 11.9 Operation of Chain Transfer

11.5.5 Interrupt Sources

An interrupt request is issued to the CPU when the DTC ends the specified number of data transfers, or when the DTC ends a data transfer for which the DISEL bit was set to 1. In the case of interrupt activation, the interrupt set as the activation source is generated. These interrupts to the CPU are subject to CPU mask level and interrupt controller priority level control.

In the case of activation by software, a software activated data transfer end interrupt (SWDTEND) is generated.

When the DISEL bit is 1 and one data transfer has ended or the specified number of transfers has ended, the SWDTE bit is held at 1 and an SWDTEND interrupt is generated after data transfer ends. The interrupt handling routine should clear the SWDTE bit to 0.

When the DTC is activated by software, an SWDTEND interrupt is not generated during a data transfer wait or during data transfer even if the SWDTE bit is set to 1.

13.3.7 Operation through an Event Link

Using the event link controller (ELC), timer RA can be made to operate in the following ways in relation to events occurring in other modules.

(1) Starting Counter Operation

The start of counting operations by timer RA can be selected by the ELOPA register of the ELC. When the event specified in ELSR0 occurs, the TSTART bit in the TRACR is set to 1, which starts counting by timer RA. However, if the specified event occurs when the TCSTF flag has already been set to 1, that event is not effective.

(2) Counting Events

The counting of events by timer RA can be selected by the ELOPA register of the ELC. When the event specified in ELSR0 occurs, event-counter operation proceeds with that event as the source to drive counting, regardless of the setting in the TCK[2:0] bits in TRAMR. When event-counter operation is to be employed, set the TSTART bit in TRACR to 1 beforehand. When the value of the counter is read, the value read out is the actual number of input events minus three.

Figure 15.11 shows an example of buffer operation when the FTIOB pin is set to PWM mode and GRD is set as the buffer register for GRB. TRCCNT is cleared on compare match A, and the FTIOB pin outputs 1 on compare match B and 0 on compare match A.

Due to the buffer operation, the FTIOB output levels are changed and the value of buffer register GRD is transferred to GRB whenever compare match B occurs. This procedure is repeated every time compare match B occurs.

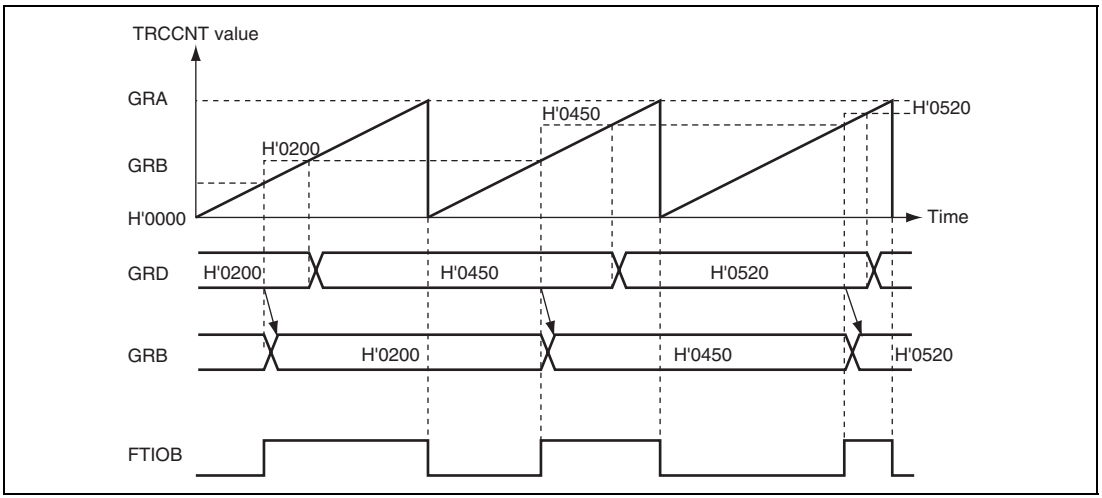


Figure 15.11 Buffer Operation Example (Output Compare)

15.4.5 Buffer Operation Timing

Figures 15.31 and 15.32 show the buffer operation timing.

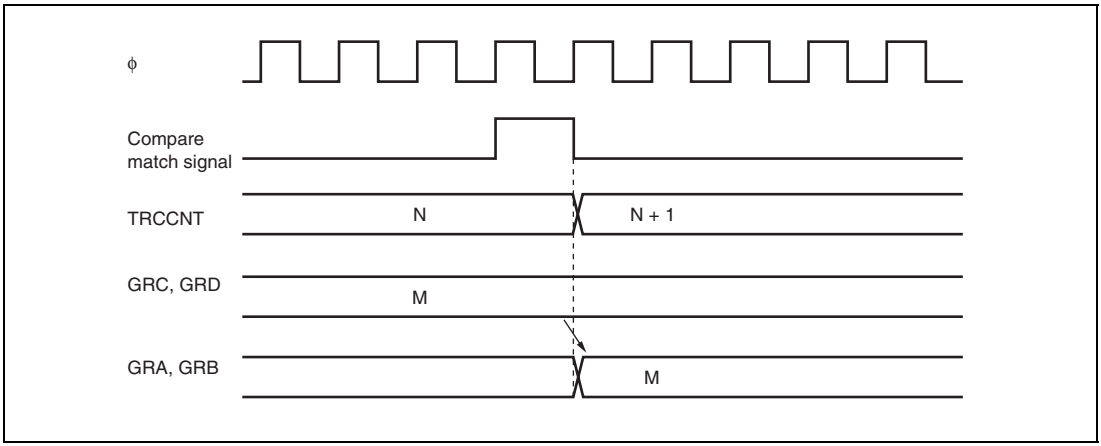


Figure 15.31 Buffer Operation Timing (Compare Match)

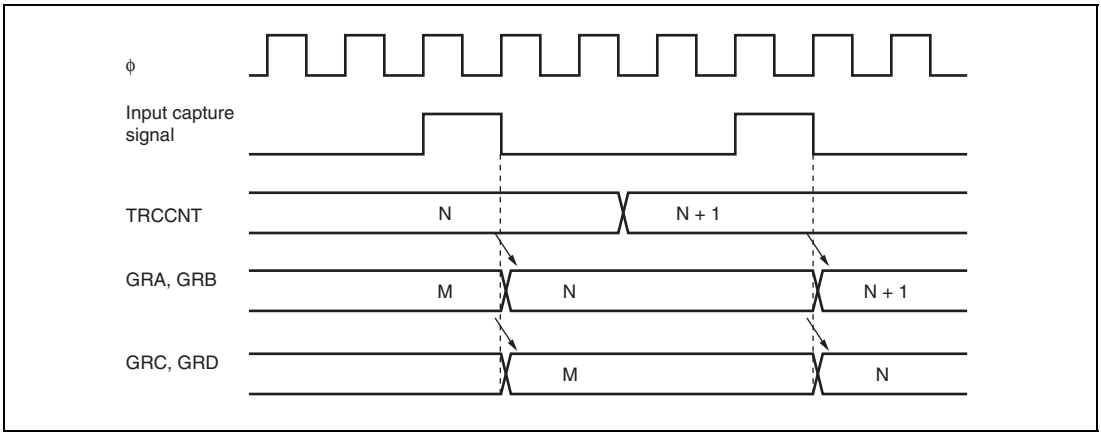


Figure 15.32 Buffer Operation Timing (Input Capture)

16.3 Operation

Timer RD has the following operating modes.

- Timer mode operation

  Enables output compare and input capture functions by setting the IOA2 to IOA0 and IOB2 to IOB0 bits in TRDIORA and the IOC3 to IOC0 and IOD3 to IOD0 bits in TRDIORC
- PWM mode operation

  Enables PWM mode operation by setting TRDPMR
- PWM3 mode operation

  Enables PWM3 mode operation by setting the PWM3 bit in TRDFCR
- Reset synchronous PWM mode operation

  Enables reset synchronous PWM mode operation by setting the CMD1 and CMD0 bits in TRDFCR
- Complementary PWM mode operation

  Enables complementary PWM mode operation by setting the CMD1 and CMD0 bits in TRDFCR

The following tables show the operating modes of the FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pins set by the appropriate bits in the registers mentioned above. Set 1 to the PMR bits corresponding to the pins allocated by the PMC.

17.2.1 Timer RE Second Data Register/Counter Data Register (TRESEC)

Address: H'FFFFA8

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00
Value after reset:	—	—	—	—	—	—	—	—

- Realtime clock mode

Bit	Symbol	Bit Name	Description	R/W
7	BSY	Timer RE busy	This bit is set to 1 when the timer RE is updating (calculating) the values of second, minute, hour, and day-of-week data registers. When this bit is 0, the values of second, minute, hour, and day-of-week data registers must be adopted.	R
6	SC12	Counting ten's position of seconds	Counts on 0 to 5 for 60-second counting.	R/W
5	SC11			R/W
4	SC10			R/W
3	SC03	Counting one's position of seconds	Counts on 0 to 9 once per second. When a carry is generated, 1 is added to the ten's position.	R/W
2	SC02			R/W
1	SC01			R/W
0	SC00			R/W

- Output-compare mode

Bit	Symbol	Bit Name	Description	R/W
7	BSY	—	Used as an 8-bit register for reading the counter data.	R
6	SC12		The counter value is retained when counting is stopped.	R/W
5	SC11		This register is initialized to H’00 with a compare-match.	R/W
4	SC10			R/W
3	SC03			R/W
2	SC02			R/W
1	SC01			R/W
0	SC00			R/W

TRESEC counts the BCD-coded second value in realtime clock mode. TRESEC is incremented from decimal 00 to 59. TRESEC is used as an 8-bit register for reading the counter data in output-compare mode.

(c) Output compare output timing

A compare match signal is generated in the final state in which TRGCNT and GR match (the point at which the count value matched by TRGCNT is updated). When a compare match signal is generated, the output value set in TRGIOR is output at the output compare output pin (TGIOA, TGIOB). After a match between TRGCNT and GR, the compare match signal is not generated until the TRGCNT input clock is generated.

Figure 18.5 shows output compare output timing.

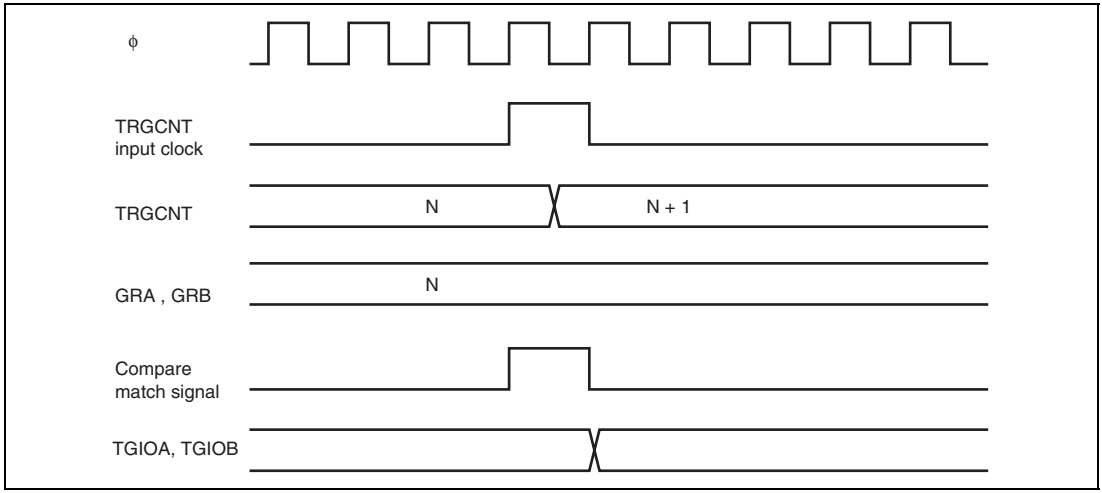
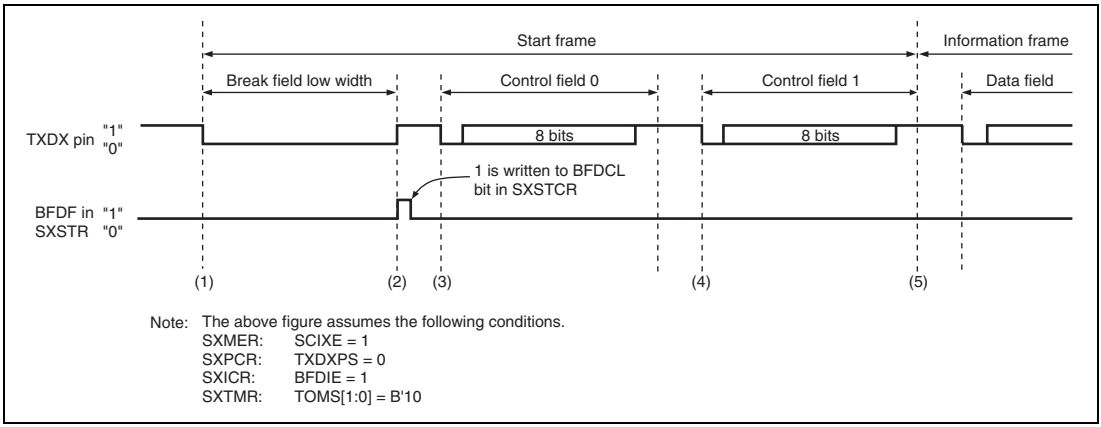


Figure 18.5 Output Compare Output Timing



Note: The above figure assumes the following conditions.
SXMER: SCIXE = 1
SXPCR: TXDXPS = 0
SXICR: BFDIE = 1
SXTMR: TOMS[1:0] = B'10

Figure 22.5 Start Frame Transmission Example

25.3.5 Operation in Clocked Synchronous Communication Mode

(1) Initialization in Clocked Synchronous Communication Mode

Figure 25.4 shows the initialization in clocked synchronous communication mode. Before transmitting and receiving data, the TE and RE bits in SSER should be cleared to 0, then the SSU should be initialized.

Note: When the operating mode, or transfer format, is changed for example, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not change the contents of the RDRF and ORER flags, or the contents of SSRDR.

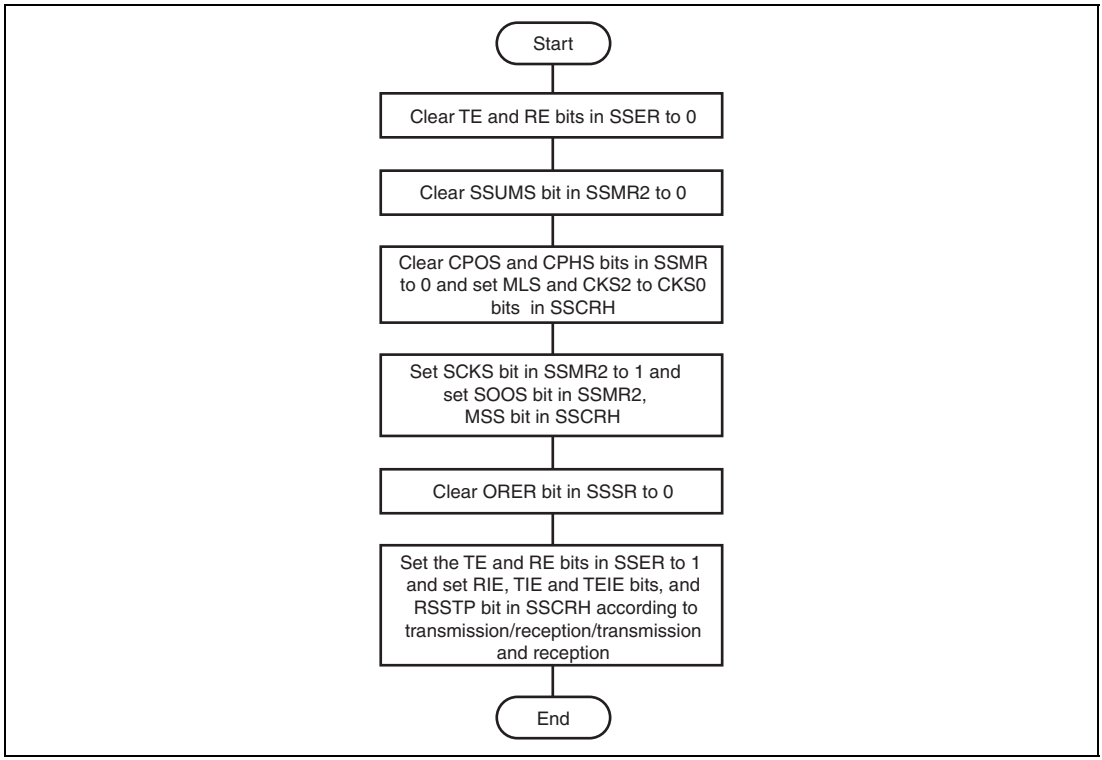


Figure 25.4 Initialization in Clocked Synchronous Communication Mode

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
PCR8	PCR87	PCR86	PCR85	PCR84*2	PCR83*2	PCR82*2	PCR81*2	PCR80*2	I/O port
PCR9*1	PCR97	PCR96	PCR95	—	—	—	—	—	
PCRA	PCRA7	PCRA6	PCRA5	PCRA4	PCRA3*1	PCRA2*1	PCRA1*1	PCRA0*1	
PCRB	PCRB7	PCRB6	PCRB5	PCRB4	PCRB3	PCRB2	PCRB1	PCRB0	
PCRJ	—	—	—	—	—	—	PCRJ1	PCRJ0	

Notes: 1. Not provided for the H8S/20103R and H8S/20115R Groups. These bits and addresses are reserved.
2. Provided only for the H8S/20323R and H8S/20335R Groups. These bits and addresses for the other groups are reserved.
3. Provided only for the H8S/20223R, H8S/20235R, H8S/20323R, and H8S/20335R Groups. These bits for the other groups are reserved.
4. Not provided for the H8S/20223R, H8S/20235R, H8S/20323R, and H8S/20335R Groups. These addresses are reserved.
5. Provided only for the H8S/20103R, H8S/20115R, H8S/20323R, and H8S/20335R Groups. These bits for the other groups are reserved.
6. Not provided for the H8S/20103R and H8S/20115R Groups. These bits are reserved.
7. Not provided for the H8S/20103R and H8S/20115R Groups. These addresses are reserved.
8. Provided only for the H8S/20223R, H8S/20235R, H8S/20323R, and H8S/20335R Groups. These addresses for the other groups are reserved.
9. Provided only for the H8S/20103R, H8S/20115R, H8S/20323R, and H8S/20335R Groups. These addresses for the other groups are reserved.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Sleep mode supply current	I_{SLEEP1}	V_{CC}	Sleep mode 1, ϕ_{OSC} = 20 MHz	—	7.5	11.0	mA	*
			Sleep mode 1, ϕ_{OSC} = 10 MHz	—	4.5	—	mA	Reference value*
	I_{SLEEP2}	V_{CC}	Sleep mode 2, ϕ_{OSC} = 20 MHz	—	2.0	3.5	mA	*
			Sleep mode 2, ϕ_{OSC} = 10 MHz	—	1.7	—	mA	Reference value*
	I_{SLEEP3}	V_{CC}	Sleep mode 3, ϕ_{OSC} = 20 MHz	—	1.8	3.2	mA	*
			Sleep mode 3, ϕ_{OSC} = 10 MHz	—	1.6	—	mA	Reference value*
	I_{SLEEP4}	V_{CC}	Sleep mode 4, ϕ_{sub} = 32 kHz	—	0.9	—	mA	Reference value*
	I_{SLEEP5}	V_{CC}	Sleep mode 5, ϕ_{sub} = 32 kHz	—	0.9	—	mA	Reference value*
	I_{SLEEP6}	V_{CC}	Sleep mode 6, ϕ_{loco} = 125 kHz	—	0.9	—	mA	Reference value*
Standby mode supply current	I_{STBY}	V_{CC}	Ta ≤ 50 °C when 32-kHz crystal resonator not used	—	10.0	30.0	µA	*
			Ta > 50 °C when 32-kHz crystal resonator not used	—	30.0	200.0	µA	*
RAM data retaining voltage	V_{RAM}	V_{CC}		2.0	—	—	V	
Main oscillator feedback resistor				—	0.3	—	MΩ	Reference value
Sub oscillator feedback resistor				—	8	—	MΩ	Reference value

Note: * Pin states during supply current measurement are given below (excluding current in the pull-up MOS transistors and output buffers).

Table 31.12 Electrical Characteristics for Low-Voltage Detection Circuit 1

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, VCC ≥ AVCC = AVref, Ta = –20 to +85 °C (N version)/ –40 to +85 °C (D version), unless otherwise indicated.

Item	Symbol	Test Conditions		Values Min.	Typ.	Max.	Unit	Notes
Voltage-detection level	V_{det1}	VD1LS[3:0] = 0111	Falling voltage	2.85	3.15	3.45	V	
			Rising voltage	3.05	3.35	3.65		
		VD1LS[3:0] = 1000	Falling voltage	3.00	3.30	3.60		
			Rising voltage	3.20	3.50	3.80		
		VD1LS[3:0] = 1001	Falling voltage	3.15	3.45	3.75		
			Rising voltage	3.35	3.65	3.95		
		VD1LS[3:0] = 1010	Falling voltage	3.30	3.60	3.90		
			Rising voltage	3.50	3.80	4.10		
		VD1LS[3:0] = 1011	Falling voltage	3.45	3.75	4.05		
			Rising voltage	3.65	3.95	4.25		
		VD1LS[3:0] = 1100	Falling voltage	3.60	3.90	4.20		
			Rising voltage	3.80	4.10	4.40		
		VD1LS[3:0] = 1101	Falling voltage	3.75	4.05	4.35		
			Rising voltage	3.95	4.25	4.55		
		VD1LS[3:0] = 1110	Falling voltage	3.90	4.20	4.50		
			Rising voltage	4.10	4.40	4.70		
		VD1LS[3:0] = 1111	Falling voltage	4.05	4.35	4.65		
			Rising voltage	4.25	4.55	4.85		
Voltage hysteresis between detection for rising and falling cases	$V_{LVD1HYS}$			—	0.22	—	V	Reference value
Low-voltage detection circuit 1 self supply current		Vcc = 5.0 V		—	2.0	—	µA	Reference value
Waiting time until low-voltage detection circuit 1 operation starts	$t_{d(E-A)}$			—	—	50.0	µs	
Detection minimum pulse width of low-voltage detection circuit 1	t_{WLVD1}			20.0	—	—	µs	