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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3665lti-199t

Table 2-2 shows the pinout for the 72-pin CSP package. Since there are four V_{DDIO} pins, the set of I/O pins associated with any V_{DDIO} may sink up to 100 mA total, same as for the 100-pin and 68-pin devices.

Table 2-2. CSP Pinout

Ball	Name	Ball	Name	Ball	Name
G6	P2[5]	F1	VDDD	A5	VDDA
E5	P2[6]	E1	VSSD	A6	VSSD
F5	P2[7]	E2	VCCD	B6	P12[2]
J7	P12[4]	C1	P15[0]	C6	P12[3]
H6	P12[5]	C2	P15[1]	A7	P0[0]
J6	VSSB	D2	P3[0]	B7	P0[1]
J5	Ind	D3	P3[1]	B5	P0[2]
H5	VBOOST	D4	P3[2]	C5	P0[3]
J4	VBAT	D5	P3[3]	A8	VIO0
H4	VSSD	B4	P3[4]	D6	P0[4]
J3	XRES_N	B3	P3[5]	D7	P0[5]
H3	P1[0]	A1	VIO3	C7	P0[6]
G3	P1[1]	B2	P3[6]	C8	P0[7]
H2	P1[2]	A2	P3[7]	E8	VCCD
J2	P1[3]	C3	P12[0]	F8	VSSD
G4	P1[4]	C4	P12[1]	G8	VDDD
G5	P1[5]	E3	P15[2]	E7	P15[4]
J1	VIO1	E4	P15[3]	F7	P15[5]
F4	P1[6]	B1 ^[12]	NC	G7	P2[0]
F3	P1[7]	B8 ^[12]	NC	H7	P2[1]
H1	P12[6]	D1 ^[12]	NC	H8	P2[2]
G1	P12[7]	D8 ^[12]	NC	F6	P2[3]
G2	P15[6]	A3	VCCA	E6	P2[4]
F2	P15[7]	A4	VSSA	J8	VIO2

Figure 2-7 and Figure 2-8 on page 12 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled Vccd must be connected together, with capacitance added, as shown in Figure 2-7 and Power System on page 31. The trace between the two Vccd pins should be as short as possible.
- The two pins labeled VSSD must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note [AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC[®] 3 and PSoC 5](#).

Notes

12. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
13. This feature on select devices only. See [Ordering Information](#) on page 120 for details.

6. System Integration

6.1 Clocking System

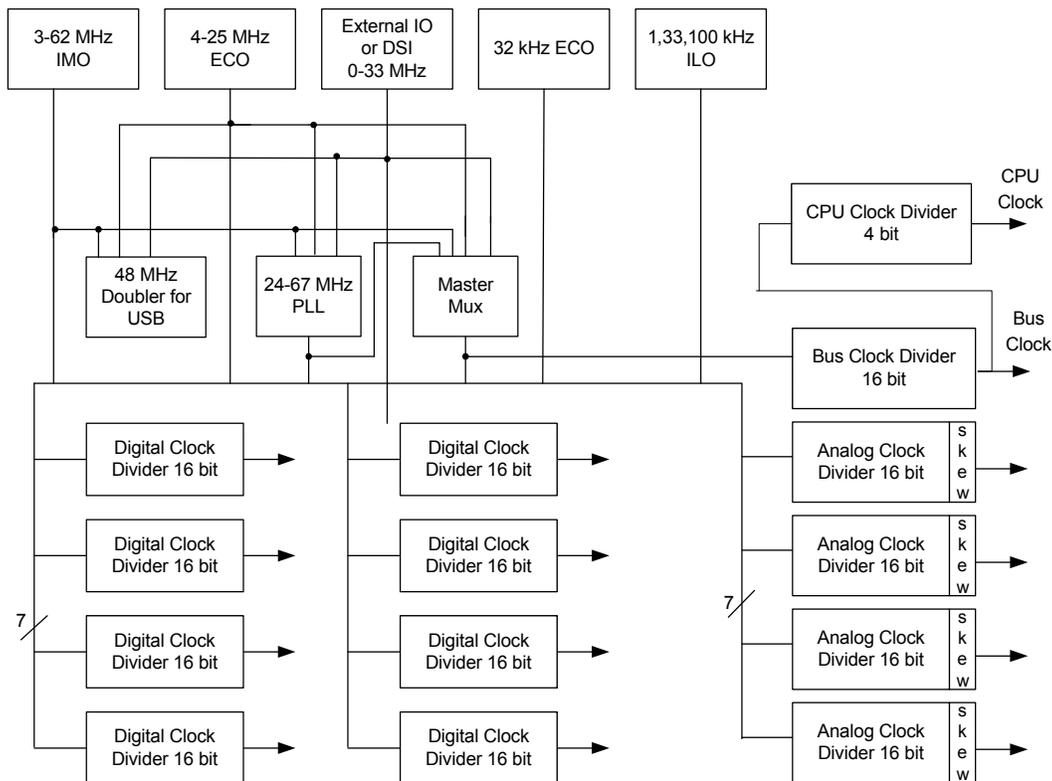
The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 66 MHz clock, accurate to $\pm 1\%$ over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. Any of the clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows you to build clocking systems with minimal input. You can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent in PSoC.

Key features of the clocking system include:

- Seven general purpose clock sources
 - 3- to 62-MHz IMO, $\pm 1\%$ at 3 MHz
 - 4- to 25-MHz external crystal oscillator (MHzECO)
 - Clock doubler provides a doubled clock frequency output for the USB block, see [USB Clock Domain](#) on page 30.
 - DSI signal from an external I/O pin or other logic
 - 24- to 67-MHz fractional PLL sourced from IMO, MHzECO, or DSI
 - 1-kHz, 33-kHz, 100-kHz ILO for WDT and sleep timer
 - 32.768-kHz external crystal oscillator (kHzECO) for RTC
- IMO has a USB mode that auto locks to the USB bus clock requiring no external crystal for USB. (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the bus clock
- Dedicated 4-bit divider for the CPU clock
- Automatic clock configuration in PSoC Creator

Figure 6-1. Clocking Subsystem

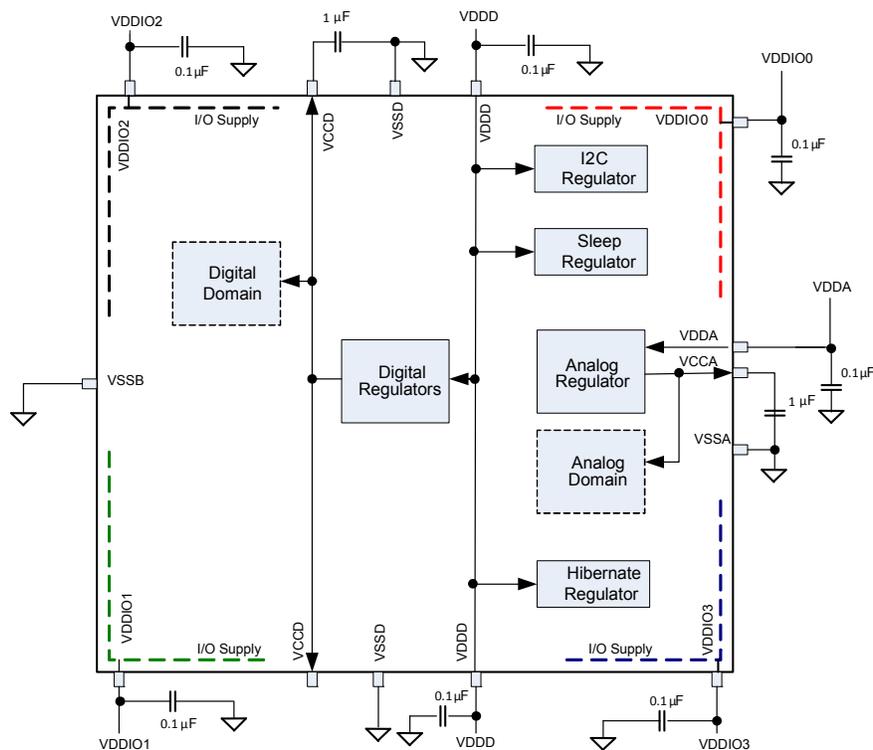


6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIO^x, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the

VDDIO pins must have capacitors connected as shown in Figure 6-4. The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a 1- μ F \pm 10% \times 5R capacitor. The power system also contains a sleep regulator, an I²C regulator, and a hibernate regulator.

Figure 6-4. PSoC Power System



Notes

- The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-8 on page 12.
- It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (VDDX or VCCX in Figure 6-4) is a significant percentage of the rated working voltage.
- You can power the device in internally regulated mode, where the voltage applied to the VDD^x pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the VCC^x pins, and do not tie the VDD^x pins to the VCC^x pins.**
- You can also power the device in externally regulated mode, that is, by directly powering the VCCD and VCCA pins. In this configuration, the VDDD pins should be shorted to the VCCD pins and the VDDA pin should be shorted to the VCCA pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.

6.2.1 Power Modes

PSoC 3 devices have four different power modes, as shown in Table 6-2 and Table 6-3. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low-power and portable devices.

PSoC 3 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and RTC functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. Figure 6-5 illustrates the allowable transitions between power modes. Sleep and hibernate modes should not be entered until all V_{DDIO} supplies are at valid voltage levels.

Table 6-2. Power Modes

Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I ² C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU	–	Only hibernate regulator active.

Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (Typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	1.2 mA ^[16]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<15 μ s	1 μ A	No	I ² C	Comparator	ILO/kHzECO	Comparator, PICU, I ² C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<100 μ s	200 nA	No	None	None	None	PICU	XRES

Note

¹⁶. Bus clock off. Execute from cache at 6 MHz. See Table 11-2 on page 72.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to “1” and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt.

While level sensitive interrupts are not directly supported; universal digital blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip’s analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in [Adjustable Output Level](#).

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders^[19]. See the “[CapSense](#)” section on page 63 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the “[LCD Direct Drive](#)” section on page 62 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO’s respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see [Figure 6-13](#)). The “[DAC](#)” section on page 64 has more details on VDAC use and reference routing to the SIO pins. Resistive pull-up and pull-down drive modes are not available with SIO in regulated output mode.

6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see [Figure 6-13](#)). Available input thresholds are:

- $0.5 \times VDDIO$
- $0.4 \times VDDIO$
- $0.5 \times V_{REF}$
- V_{REF}

Typically a voltage DAC (VDAC) generates the V_{REF} reference. “[DAC](#)” section on page 64 has more details on VDAC use and reference routing to the SIO pins.

Note

¹⁹. GPIOs with opamp outputs are not recommended for use with CapSense

6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

7. Digital Subsystem

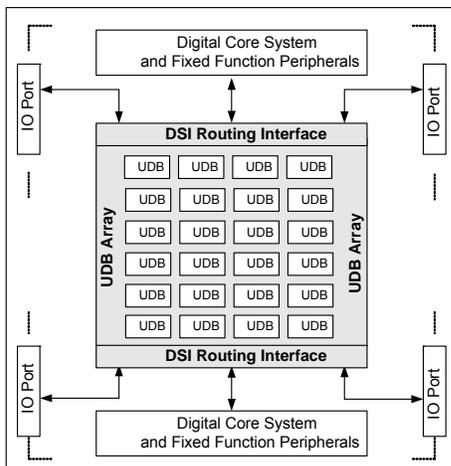
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- **Universal Digital Blocks (UDB)** – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- **Universal Digital Block Array** – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- **Digital System Interconnect (DSI)** – Digital signals from Universal Digital Blocks (UDBs), fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block Array.

Figure 7-1. CY8C36 Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C36 family's Universal Digital Blocks (UDBs) and Analog Blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the data sheet, and the list is always growing. An example of a component available for use in CY8C36 family, but, not explicitly called out in this data sheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **Communications**
 - I²C
 - UART
 - SPI
- **Functions**
 - EMIF
 - PWMs
 - Timers
 - Counters
- **Logic**
 - NOT
 - OR
 - XOR
 - AND

7.1.2 Example Analog Components

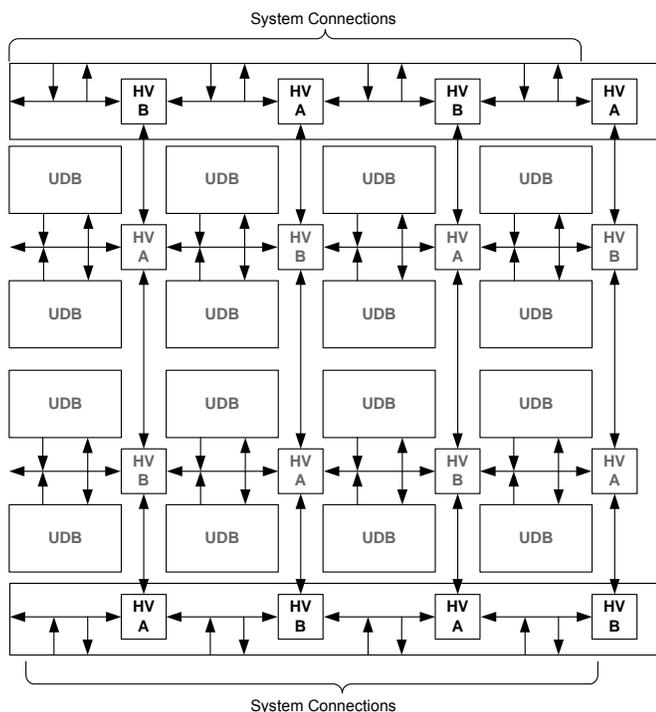
The following is a sample of the analog components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **Amplifiers**
 - TIA
 - PGA
 - opamp
- **ADC**
 - Delta-Sigma
- **DACs**
 - Current
 - Voltage
 - PWM
- **Comparators**
- **Mixers**

7.3 UDB Array Description

Figure 7-7 shows an example of a 16-UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoc Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-7. Digital System Interface Structure

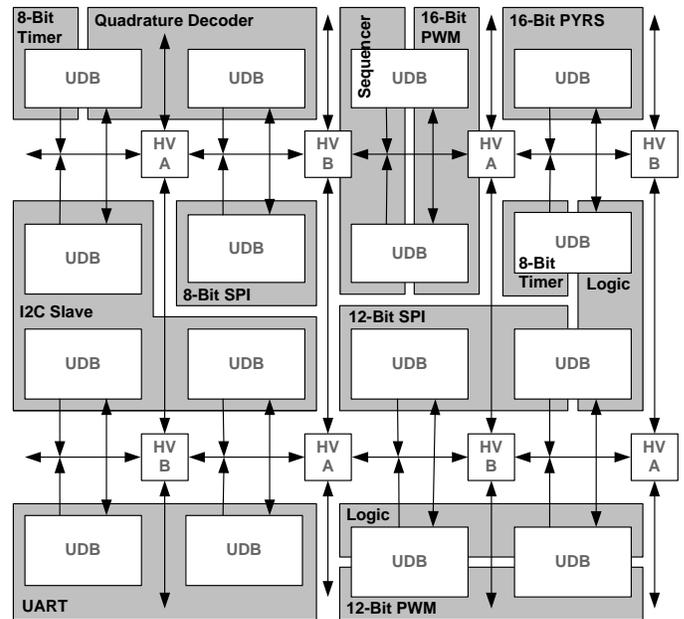


7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-8. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

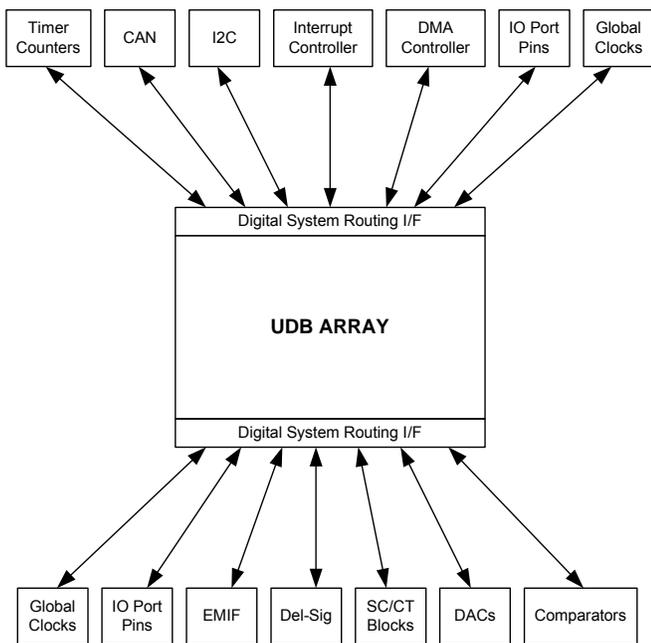
The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

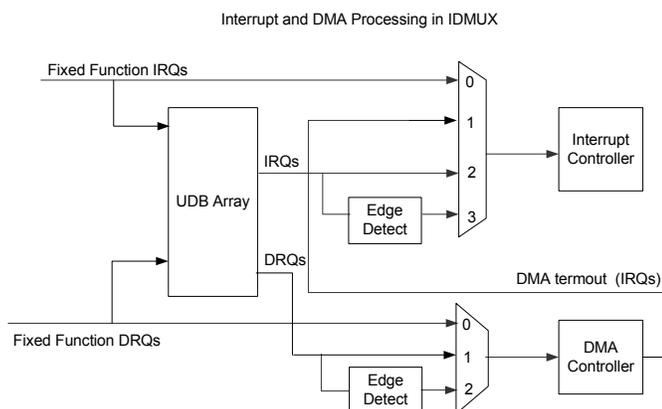
- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

Figure 7-9. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C36 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the master clock (see Figure 6-1 on page 28). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-11. I/O Pin Synchronization Routing

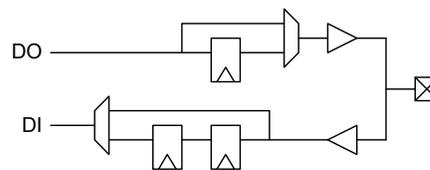
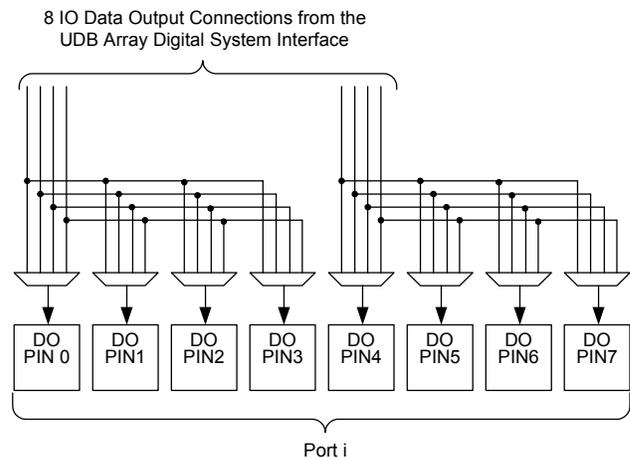


Figure 7-12. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in CY8C36, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

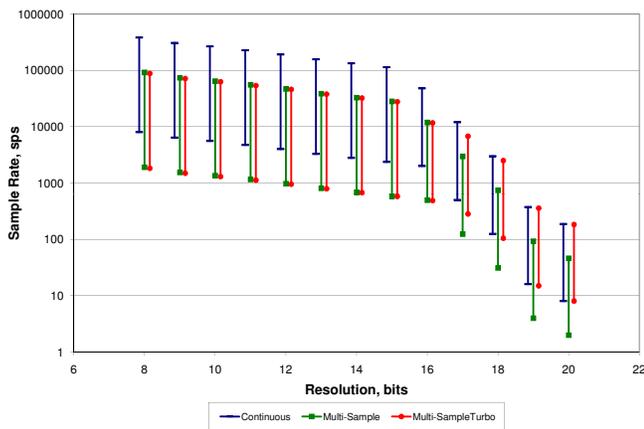
8.2 Delta-sigma ADC

The CY8C36 device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for measurement applications. The converter can be configured to output 12-bit resolution at data rates of up to 192 ksps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
12	192 k	66
8	384 k	43

Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V

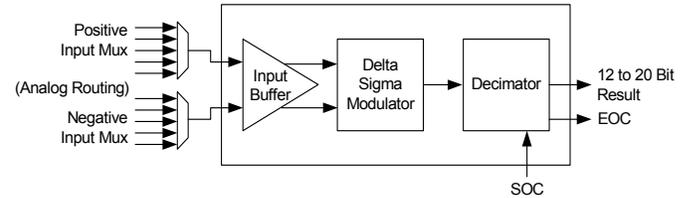


8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the

high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

More information on output formats is provided in the Technical Reference Manual.

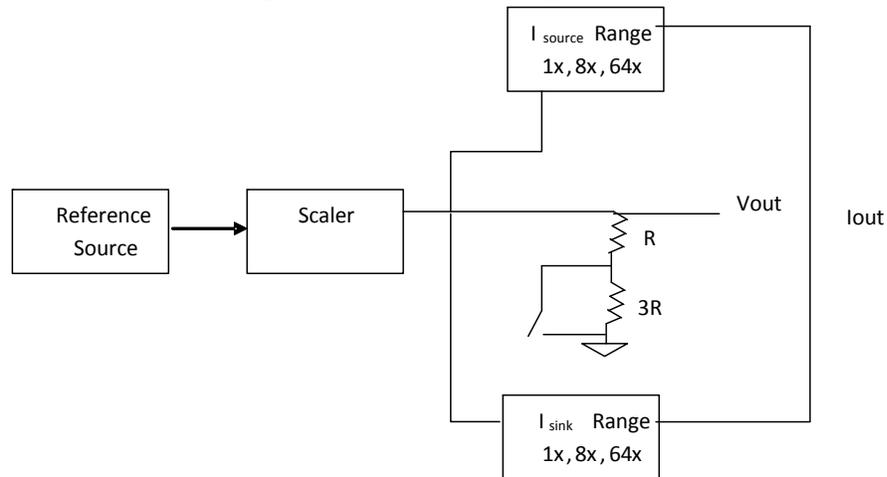
8.9 DAC

The CY8C36 parts contain up to four Digital to Analog Converters (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct $\pm 25\%$ of gain error

- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-11. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 μA , 0 to 255 μA , and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

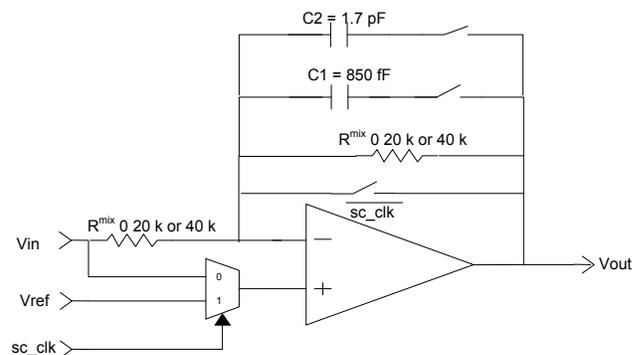
8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency ($F_{\text{clk}} + F_{\text{in}}$ and $F_{\text{clk}} - F_{\text{in}}$) and reduced-level frequency components at odd integer multiples of the local

oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-12. Mixer Configuration



9.8 CSP Package Bootloader

A factory-installed bootloader program is included in all devices with CSP packages. The bootloader is compatible with PSoC Creator 3.0 bootloadable project files and has the following features:

- I²C-based
- SCLK and SDAT available at P1[6] and P1[7], respectively
- External pull-up resistors required
- I²C slave, address 4, data rate = 100 kbps
- Single application
- Wait two seconds for bootload command
- Other bootloader options are as set by the PSoC Creator 3.0 Bootloader Component default
- Occupies the bottom 9K of flash

For more information on this bootloader, see the following Cypress application notes:

- [AN89611](#) – PSoC® 3 AND PSoC 5LP - Getting Started With Chip Scale Packages (CSP)
- [AN73854](#) – PSoC 3 and PSoC 5 LP Introduction to Bootloaders
- [AN60317](#) – PSoC 3 and PSoC 5 LP I²C Bootloader

Note that a PSoC Creator bootloadable project must be associated with .hex and .elf files for a bootloader project that is configured for the target device. Bootloader .hex and .elf files can be found at www.cypress.com/go/PSoC3datasheet.

The factory-installed bootloader can be overwritten using JTAG or SWD programming.

Table 11-7. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L _{BOOST}	Boost inductor	4.7 μH nominal	3.7	4.7	5.7	μH
		10 μH nominal	8.0	10.0	12.0	μH
		22 μH nominal	17.0	22.0	27.0	μH
C _{BOOST}	Total capacitance sum of V _{DD} , V _D DA, V _{DDIO} ^[41]		17.0	26.0	31.0	μF
C _{BAT}	Battery filter capacitor		17.0	22.0	27.0	μF
I _F	Schottky diode average forward current		1.0	–	–	A
V _R	Schottky reverse voltage		20.0	–	–	V

Figure 11-8. T_A range over V_{BAT} and V_{OUT}

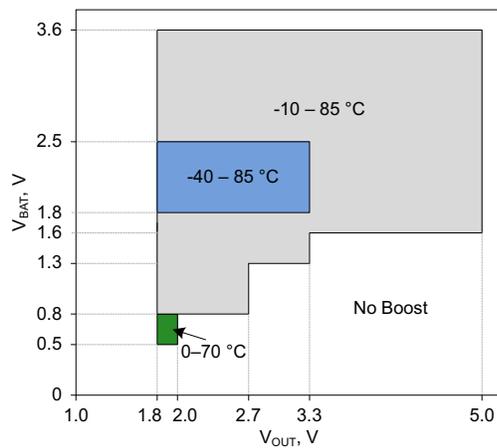


Figure 11-9. I_{OUT} range over V_{BAT} and V_{OUT}

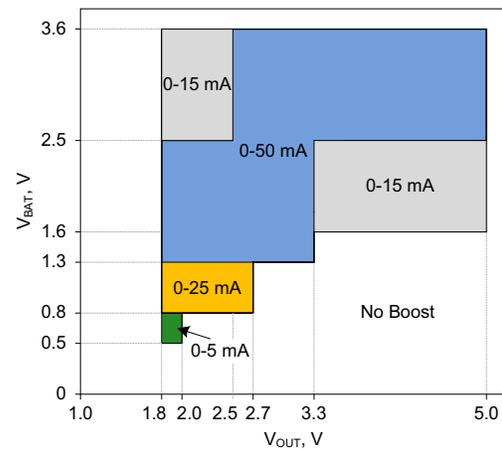
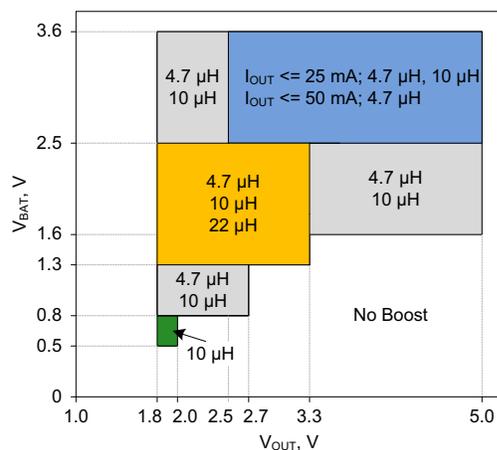


Figure 11-10. L_{BOOST} values over V_{BAT} and V_{OUT}



Note

41. Based on device characterization (Not production tested).

11.4 Inputs and Outputs

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

When the power supplies ramp up, there are low-impedance connections between each GPIO pin and its V_{DDIO} supply. This causes the pin voltages to track V_{DDIO} until both V_{DDIO} and V_{DDA} reach the IPOR voltage, which can be as high as 1.45 V. At that point, the low-impedance connections no longer exist and the pins change to their normal NVL settings.

11.4.1 GPIO

Table 11-9. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	CMOS Input, PRT[*]CTL = 0	$0.7 \times V_{DDIO}$	–	–	V
V_{IL}	Input voltage low threshold	CMOS Input, PRT[*]CTL = 0	–	–	$0.3 \times V_{DDIO}$	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[*]CTL = 1, $V_{DDIO} < 2.7\text{ V}$	$0.7 \times V_{DDIO}$	–	–	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[*]CTL = 1, $V_{DDIO} \geq 2.7\text{ V}$	2.0	–	–	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[*]CTL = 1, $V_{DDIO} < 2.7\text{ V}$	–	–	$0.3 \times V_{DDIO}$	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[*]CTL = 1, $V_{DDIO} \geq 2.7\text{ V}$	–	–	0.8	V
V_{OH}	Output voltage high	$I_{OH} = 4\text{ mA}$ at 3.3 V_{DDIO}	$V_{DDIO} - 0.6$	–	–	V
		$I_{OH} = 1\text{ mA}$ at 1.8 V_{DDIO}	$V_{DDIO} - 0.5$	–	–	V
V_{OL}	Output voltage low	$I_{OL} = 8\text{ mA}$ at 3.3 V_{DDIO}	–	–	0.6	V
		$I_{OL} = 4\text{ mA}$ at 1.8 V_{DDIO}	–	–	0.6	V
		$I_{OL} = 3\text{ mA}$ at 3.3 V_{DDIO}	–	–	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	k Ω
Rpulldown	Pull-down resistor		3.5	5.6	8.5	k Ω
I_{IL}	Input leakage current (absolute value) ^[43]	25 $^{\circ}\text{C}$, $V_{DDIO} = 3.0\text{ V}$	–	–	2	nA
C_{IN}	Input capacitance ^[43]	GPIOs not shared with opamp outputs, MHz ECO or kHzECO	–	4	7	pF
		GPIOs shared with MHz ECO or kHzECO ^[44]	–	5	7	pF
		GPIOs shared with opamp outputs	–	–	18	pF
V_H	Input voltage hysteresis (Schmitt-Trigger) ^[43]		–	40	–	mV
I _{diode}	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	μA
R _{global}	Resistance pin to analog global bus	25 $^{\circ}\text{C}$, $V_{DDIO} = 3.0\text{ V}$	–	320	–	Ω
R _{mux}	Resistance pin to analog mux bus	25 $^{\circ}\text{C}$, $V_{DDIO} = 3.0\text{ V}$	–	220	–	Ω

Notes

43. Based on device characterization (Not production tested).

44. For information on designing with PSoC oscillators, refer to the application note, [AN54439 - PSoC® 3 and PSoC 5 External Oscillator](#).

Figure 11-36. IDAC INL vs Input Code, Range = 255 μ A, Source Mode

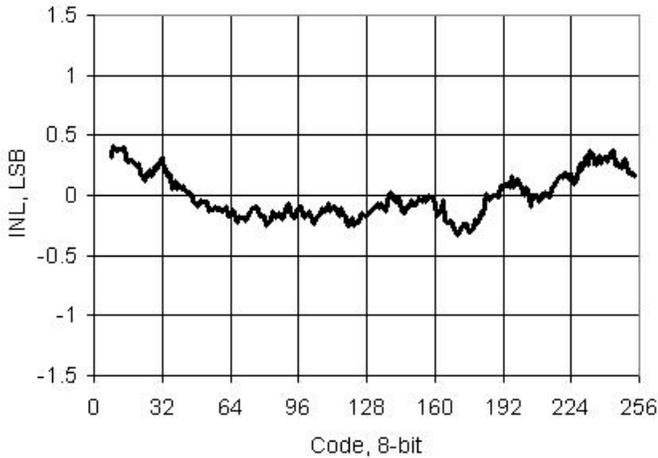


Figure 11-37. IDAC INL vs Input Code, Range = 255 μ A, Sink Mode

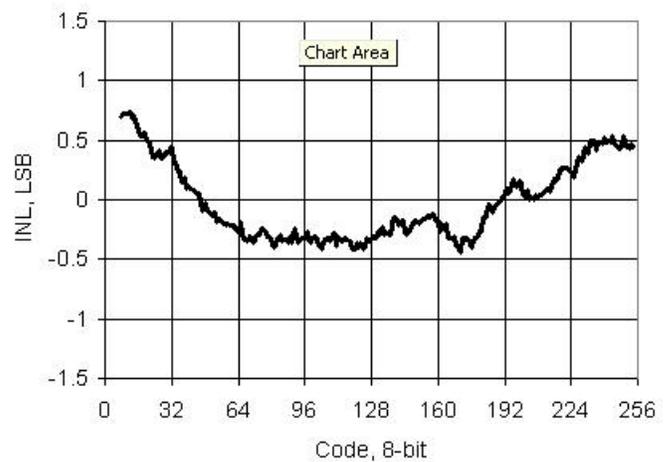


Figure 11-38. IDAC DNL vs Input Code, Range = 255 μ A, Source Mode

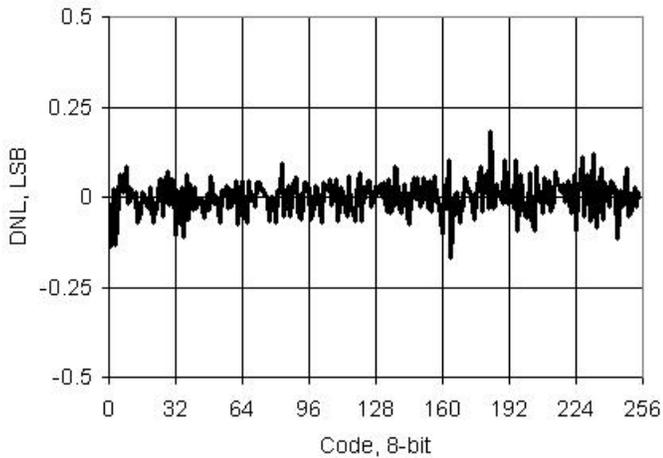


Figure 11-39. IDAC DNL vs Input Code, Range = 255 μ A, Sink Mode

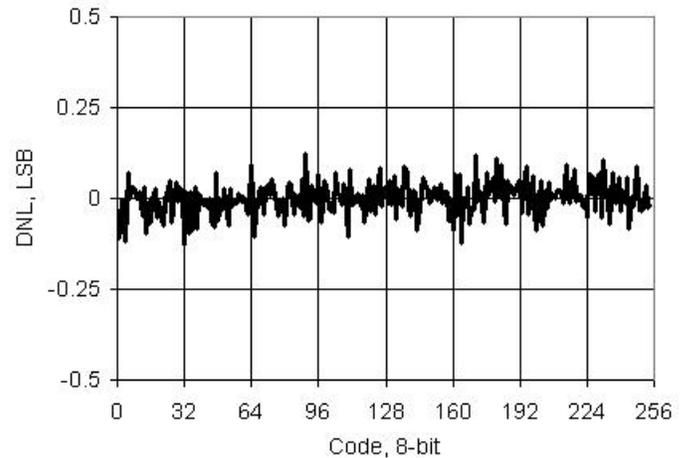


Figure 11-40. IDAC INL vs Temperature, Range = 255 μ A, High speed mode

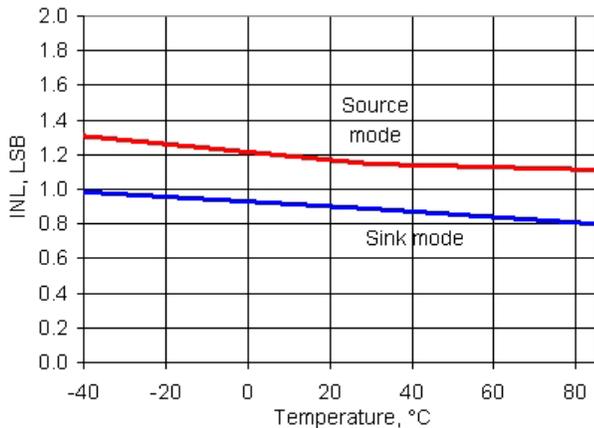


Figure 11-41. IDAC DNL vs Temperature, Range = 255 μ A, High speed mode

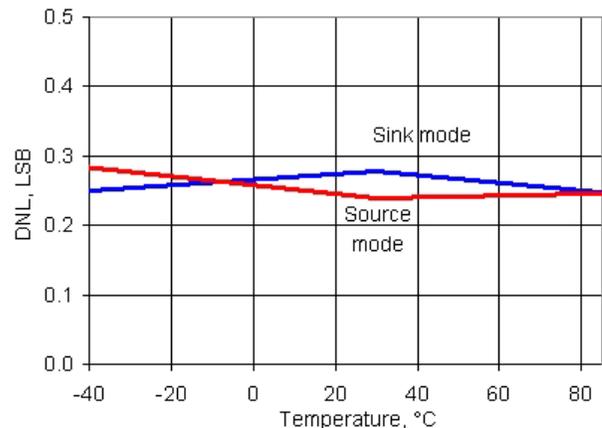


Figure 11-52. VDAC INL vs Temperature, 1 V Mode

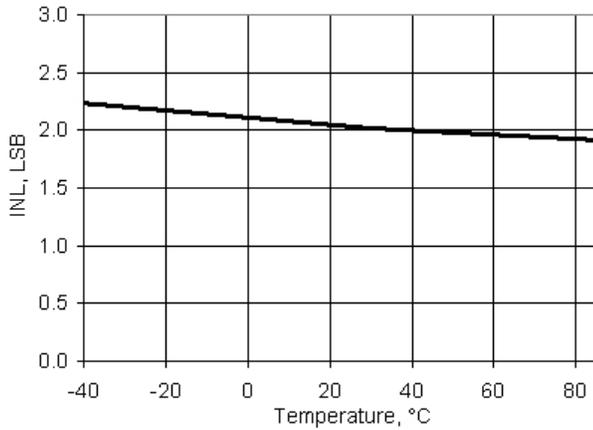


Figure 11-53. VDAC DNL vs Temperature, 1 V Mode

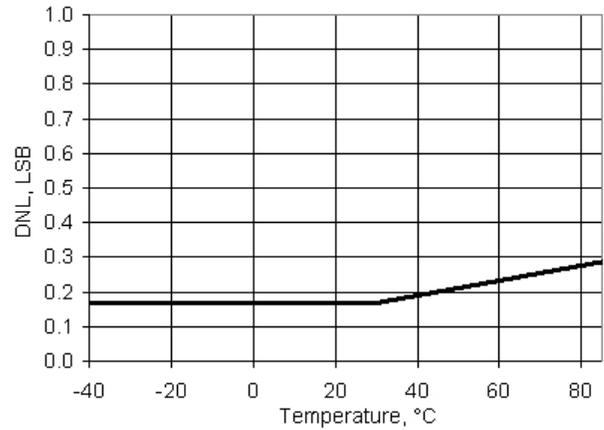


Figure 11-54. VDAC Full Scale Error vs Temperature, 1 V Mode

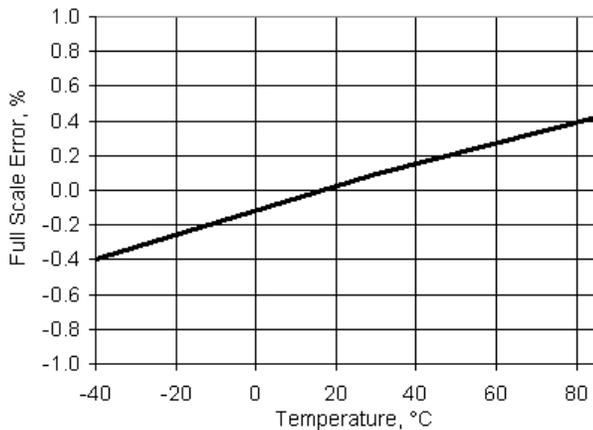


Figure 11-55. VDAC Full Scale Error vs Temperature, 4 V Mode

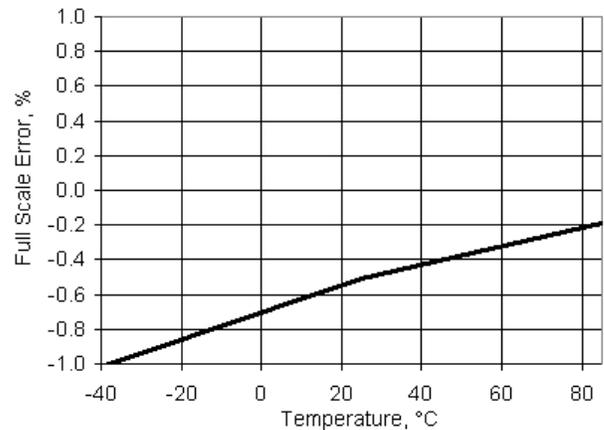


Figure 11-56. VDAC Operating Current vs Temperature, 1V Mode, Low speed mode

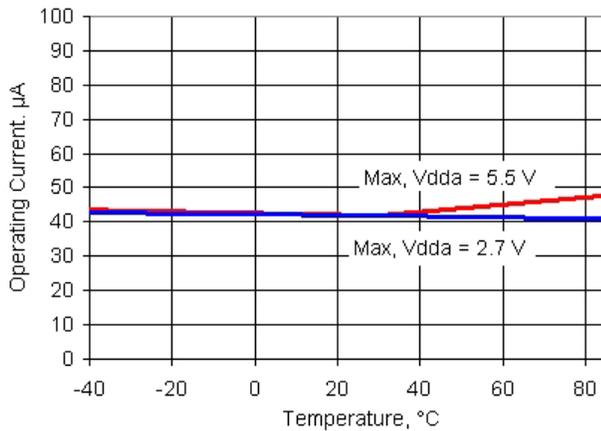


Figure 11-57. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode

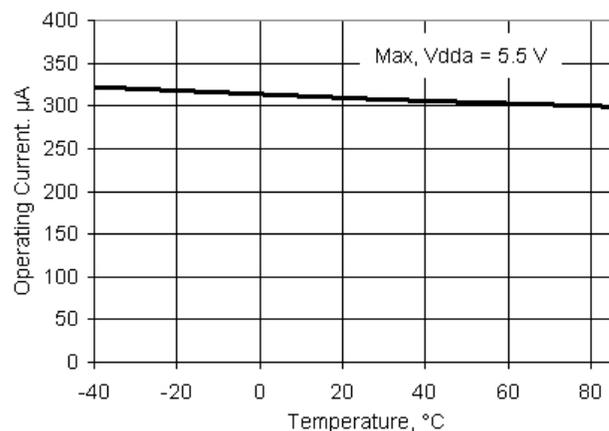


Table 11-37. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	-3 dB bandwidth	Power mode = high, gain = 1, input = 100 mV peak-to-peak	6.7	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/μs
e _n	Input noise density	Power mode = high, V _{DDA} = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

Figure 11-63. Bandwidth vs. Temperature, at Different Gain Settings, Power Mode = High

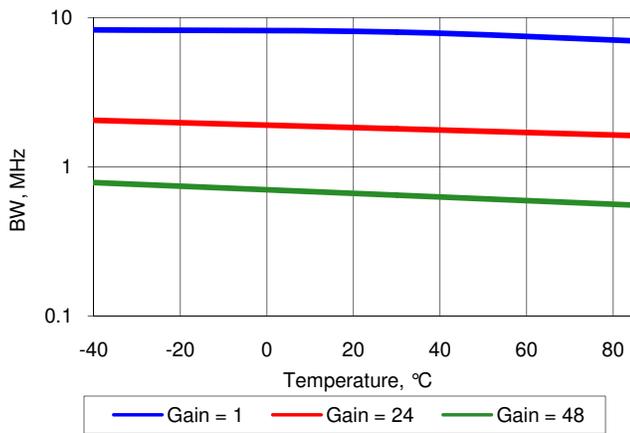
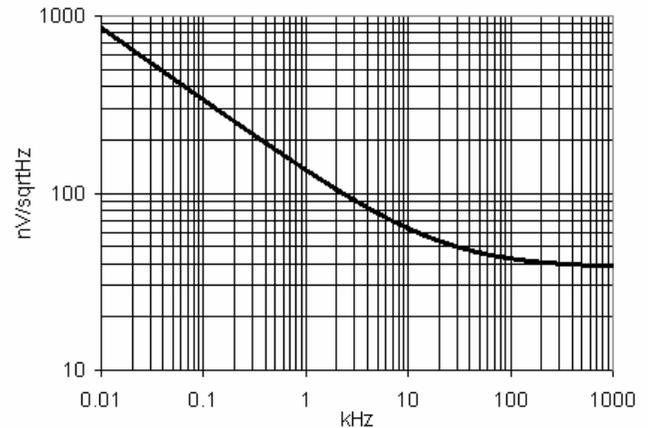


Figure 11-64. Noise vs. Frequency, V_{DDA} = 5 V, Power Mode = High



11.5.11 Temperature Sensor

Table 11-38. Temperature Sensor Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Temp sensor accuracy	Range: -40 °C to +85 °C	–	±5	–	°C

11.5.12 LCD Direct Drive

Table 11-39. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I _{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 MHz, V _{DDIO} = V _{DDA} = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	μA
I _{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	μA
V _{BIAS}	LCD bias range (V _{BIAS} refers to the main output voltage(V _O) of LCD DAC)	V _{DDA} ≥ 3 V and V _{DDA} ≥ V _{BIAS}	2	–	5	V
	LCD bias step size	V _{DDA} ≥ 3 V and V _{DDA} ≥ V _{BIAS}	–	9.1 × V _{DDA}	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I _{OUT}	Output drive current per segment driver)	V _{DDIO} = 5.5V, strong drive mode	355	–	710	μA

Table 11-40. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f _{LCD}	LCD frame rate		10	50	150	Hz

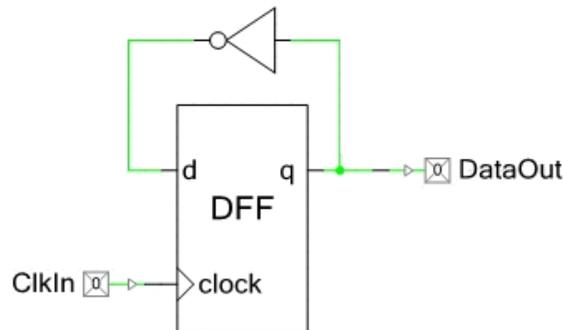
11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-54. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F _{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F _{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F _{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F _{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-65 .	25 °C, V _{DD} ≥ 2.7 V	–	20	25	ns
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-65 .	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-65. Clock to Output Performance



11.7.3 Nonvolatile Latches (NVL)

Table 11-59. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V _{DDD} pin	1.71	–	5.5	V

Table 11-60. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1K	–	–	program/erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	program/erase cycles
	NVL data retention time	Average ambient temp. T _A ≤ 55 °C	20	–	–	years
		Average ambient temp. T _A ≤ 85 °C	10	–	–	years

11.7.4 SRAM

Table 11-61. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-62. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{SRAM}	SRAM operating frequency		DC	–	67.01	MHz

11.7.5 External Memory Interface

Figure 11-66. Asynchronous Write and Read Cycle Timing, No Wait States

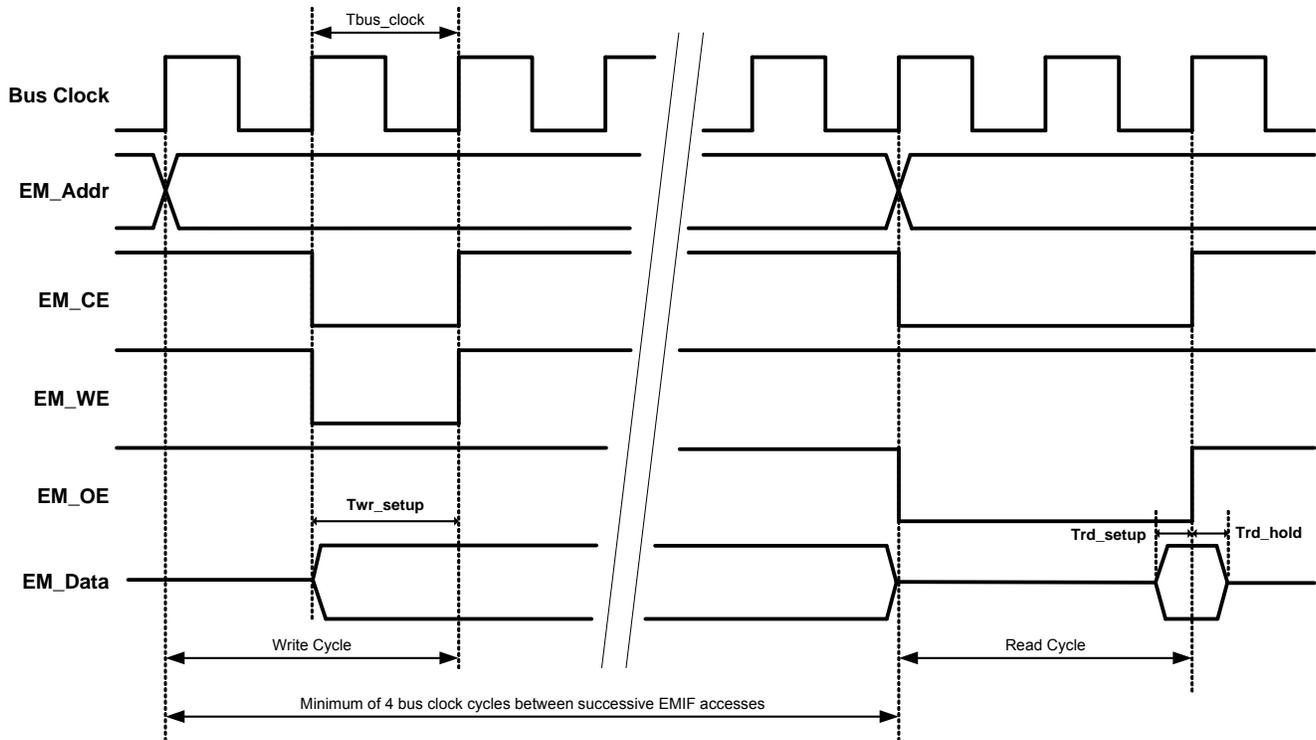


Table 11-63. Asynchronous Write and Read Timing Specifications^[68]

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency ^[69]		–	–	33	MHz
Tbus_clock	Bus clock period ^[70]		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_WE and EM_CE		$T_{bus_clock} - 10$	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

Notes

68. Based on device characterization (Not production tested).

69. EMIF signal timings are limited by GPIO frequency limitations. See “GPIO” section on page 80.

70. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) (continued) Document Number: 001-53413				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
*T	4188568	11/14/2013	MKEA	Added SIO Comparator Specifications. Corrected typo in the V_{REF} parameter in the Voltage Reference Specifications. Added CSP information in Packaging and Ordering Information sections. Updated delta-sigma V_{OS} spec conditions.
*U	4385782	05/21/2014	MKEA	Updated General Description and Features . Added More Information and PSoC Creator sections. Updated 100-pin TQFP package diagram.
*V	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in VDAC DC Specifications . Updated Figure 6-11 . Added second note after Figure 6-4 . Added a reference to Fig 6-1 in Section 6.1.1 and Section 6.1.2 . Updated Section 6.2.2 . Added Section 7.8.1 . Updated Boost specifications.
*W	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of TWRITE from 2 to 10 in EEPROM AC specs table. Changed "Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Section 11.7.5. Updated Delta-sigma ADC DC Specifications
*X	4932879	09/24/2015	MKEA	Changed the Regulator Output Capacitor min and max from "-" to 0.9 and 1.1, respectively. Added reference to AN54439 in Section 11.9.3. Added MHz ECO DC specs table. Removed references to IPOR rearm issues in Section 6.3.1.1. Table 6-1: Changed DSI Fmax to 33 MHz. Figure 6-1: Changed External I/O or DSI to 0-33 MHz. Table 11-10: Changed Fgpiopin Max to 33 MHz. Table 11-12: Changed Fsiopin Max to 33 MHz.
*Y	5322536	06/27/2016	MKEA	Updated More Information . Corrected typos in External Electrical Connections . Added links to CAD Libraries in Section 2.