



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3666axi-037t">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3666axi-037t</a>

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521](#), [How to Design with PSoC 3](#), [PSoC 4](#), and [PSoC 5LP](#). Following is an abbreviated list for PSoC 3:

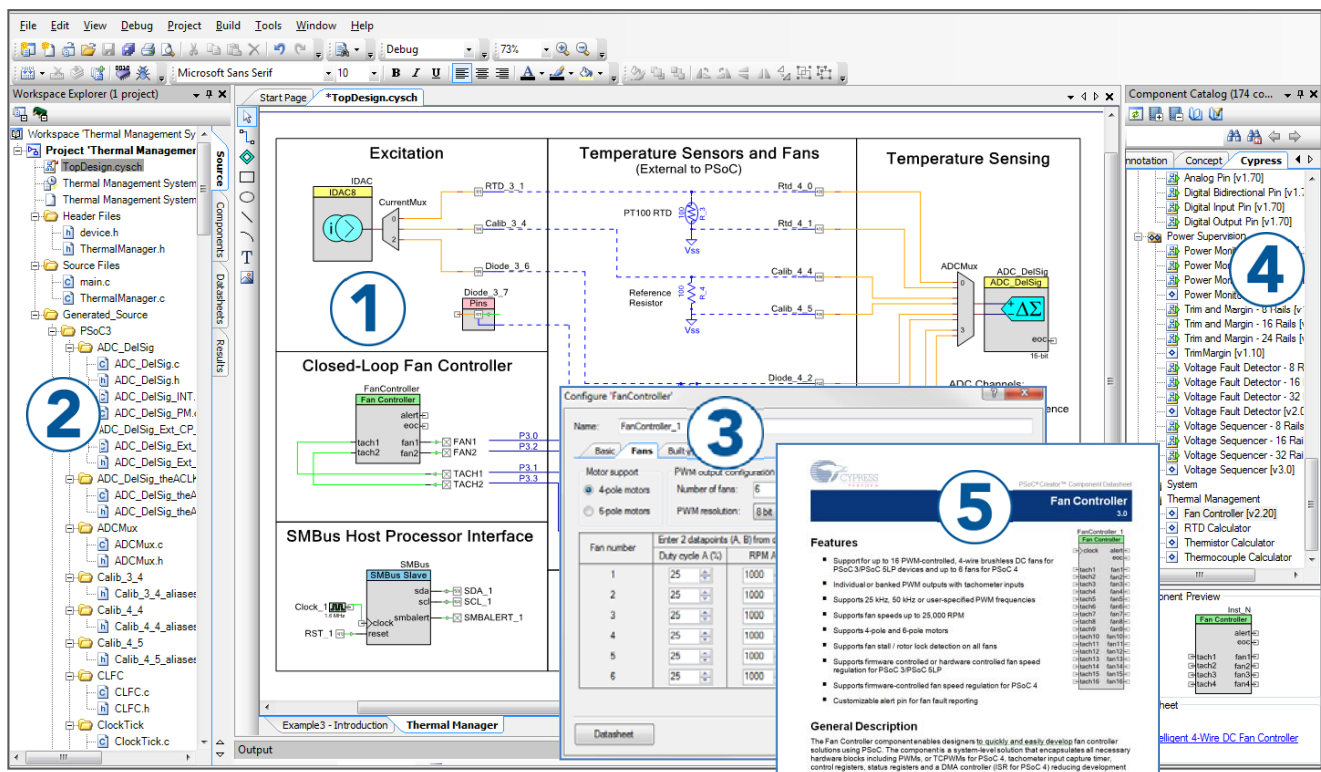
- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)  
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes and [code examples](#) covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 3 are:
  - [AN54181](#): Getting Started With PSoC 3
  - [AN61290](#): Hardware Design Considerations
  - [AN57821](#): Mixed Signal Circuit Board Layout
  - [AN58304](#): Pin Selection for Analog Designs
  - [AN81623](#): Digital Design Best Practices
  - [AN73854](#): Introduction To Bootloaders
- Development Kits:
  - [CY8CKIT-030](#) is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
  - [CY8CKIT-001](#) provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
  - The [MiniProg3](#) device provides an interface for flash programming and debug.
- Technical Reference Manuals (TRM)
  - [Architecture TRM](#)
  - [Registers TRM](#)
  - [Programming Specification](#)

## PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

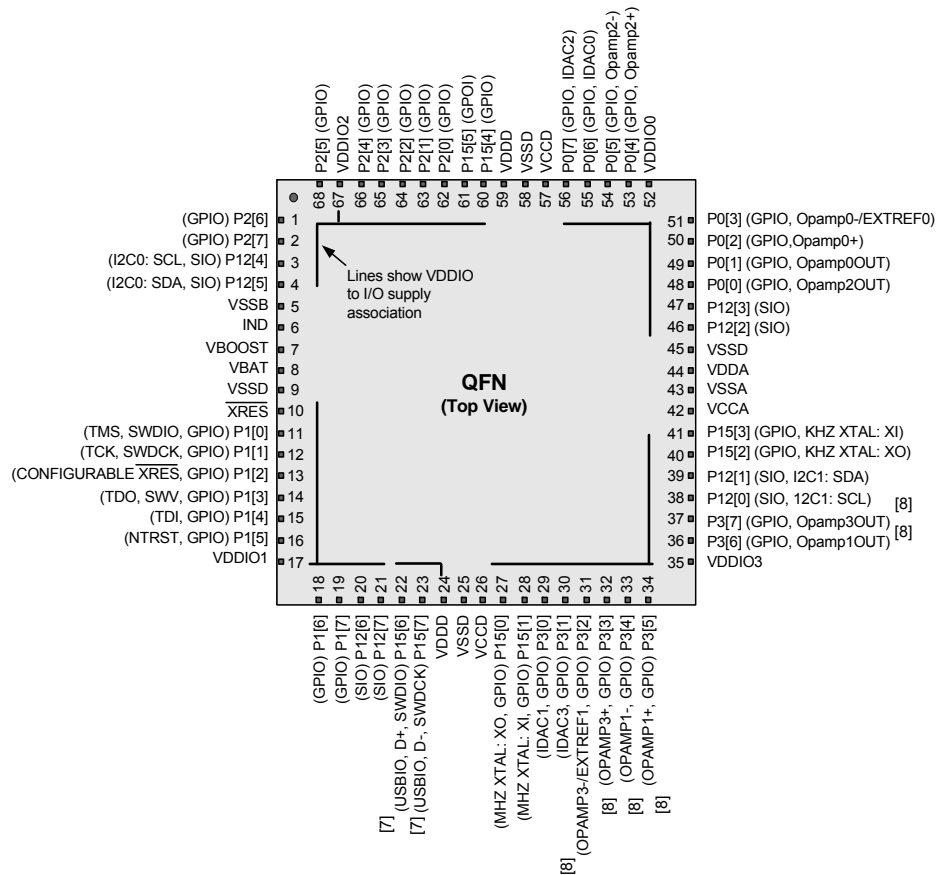
**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



## Contents

<b>1. Architectural Overview .....</b>	<b>4</b>	<b>9. Programming, Debug Interfaces, Resources .....</b>	<b>65</b>
<b>2. Pinouts .....</b>	<b>6</b>	9.1 JTAG Interface .....	66
<b>3. Pin Descriptions .....</b>	<b>12</b>	9.2 Serial Wire Debug Interface .....	67
<b>4. CPU .....</b>	<b>13</b>	9.3 Debug Features .....	68
4.1 8051 CPU .....	13	9.4 Trace Features .....	68
4.2 Addressing Modes .....	14	9.5 Single Wire Viewer Interface .....	68
4.3 Instruction Set .....	14	9.6 Programming Features .....	68
4.4 DMA and PHUB .....	18	9.7 Device Security .....	68
4.5 Interrupt Controller .....	20	9.8 CSP Package Bootloader .....	69
<b>5. Memory .....</b>	<b>23</b>	<b>10. Development Support .....</b>	<b>70</b>
5.1 Static RAM .....	23	10.1 Documentation .....	70
5.2 Flash Program Memory .....	23	10.2 Online .....	70
5.3 Flash Security .....	23	10.3 Tools .....	70
5.4 EEPROM .....	24	<b>11. Electrical Specifications .....</b>	<b>71</b>
5.5 Nonvolatile Latches (NVLs) .....	24	11.1 Absolute Maximum Ratings .....	71
5.6 External Memory Interface .....	25	11.2 Device Level Specifications .....	72
5.7 Memory Map .....	26	11.3 Power Regulators .....	76
<b>6. System Integration .....</b>	<b>28</b>	11.4 Inputs and Outputs .....	80
6.1 Clocking System .....	28	11.5 Analog Peripherals .....	88
6.2 Power System .....	31	11.6 Digital Peripherals .....	105
6.3 Reset .....	35	11.7 Memory .....	109
6.4 I/O System and Routing .....	37	11.8 PSoC System Resources .....	113
<b>7. Digital Subsystem .....</b>	<b>44</b>	11.9 Clocking .....	116
7.1 Example Peripherals .....	44	<b>12. Ordering Information .....</b>	<b>120</b>
7.2 Universal Digital Block .....	46	12.1 Part Numbering Conventions .....	121
7.3 UDB Array Description .....	49	<b>13. Packaging .....</b>	<b>122</b>
7.4 DSI Routing Interface Description .....	49	<b>14. Acronyms .....</b>	<b>126</b>
7.5 CAN .....	51	<b>15. Reference Documents .....</b>	<b>127</b>
7.6 USB .....	53	<b>16. Document Conventions .....</b>	<b>128</b>
7.7 Timers, Counters, and PWMs .....	53	16.1 Units of Measure .....	128
7.8 I <sup>2</sup> C .....	54	<b>17. Revision History .....</b>	<b>129</b>
7.9 Digital Filter Block .....	56	<b>18. Sales, Solutions, and Legal Information .....</b>	<b>137</b>
<b>8. Analog Subsystem .....</b>	<b>56</b>	Worldwide Sales and Design Support.....	137
8.1 Analog Routing .....	57	Products .....	137
8.2 Delta-sigma ADC .....	59	PSoC® Solutions .....	137
8.3 Comparators .....	60	Cypress Developer Community.....	137
8.4 Opamps .....	61	Technical Support .....	137
8.5 Programmable SC/CT Blocks .....	61		
8.6 LCD Direct Drive .....	62		
8.7 CapSense .....	63		
8.8 Temp Sensor .....	63		
8.9 DAC .....	64		
8.10 Up/Down Mixer .....	64		
8.11 Sample and Hold .....	65		

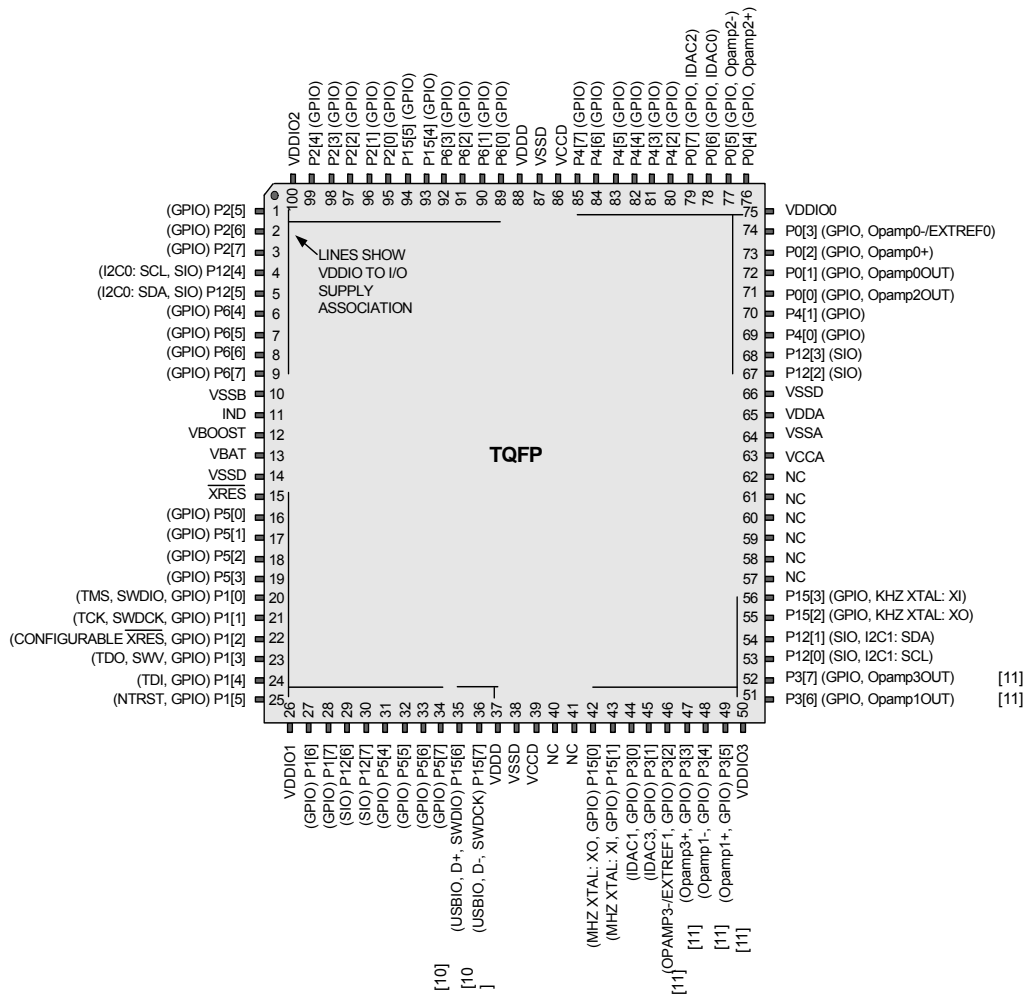
Figure 2-5. 68-pin QFN Part Pinout<sup>[9]</sup>



## Notes

- Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- This feature on select devices only. See [Ordering Information](#) on page 120 for details.
- The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.

**Figure 2-6. 100-pin TQFP Part Pinout**



**Table 2-1. VDDIO and Port Pin Associations**

VDDIO	Port Pins
VDDIO0	P0[7:0], P4[7:0], P12[3:2]
VDDIO1	P1[7:0], P5[7:0], P12[7:6]
VDDIO2	P2[7:0], P6[7:0], P12[5:4], P15[5:4]
VDDIO3	P3[7:0], P12[1:0], P15[3:0]
VDDD	P15[7:6] (USB D+, D-)

**Notes**

- 10. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- 11. This feature on select devices only. See [Ordering Information](#) on page 120 for details.

#### 4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. [Table 4-5](#) shows the list of jump instructions.

**Table 4-5. Jump Instructions**

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A, Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn, rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

#### 4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

##### 4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access

- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

**Table 4-6. PHUB Spokes and Peripherals**

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, CAN, I <sup>2</sup> C, Timers, Counters, and PWMs
5	DFB
6	UDBs group 1
7	UDBs group 2

## 4.4.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TD) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64 KB
- TDs may be nested and/or chained for complex transactions

## 4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100% of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

**Table 4-7. Priority Levels**

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

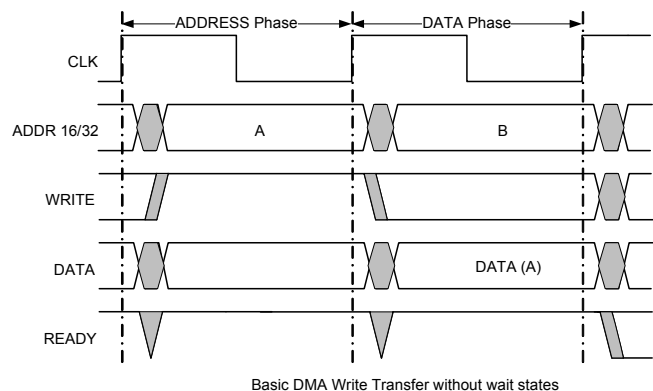
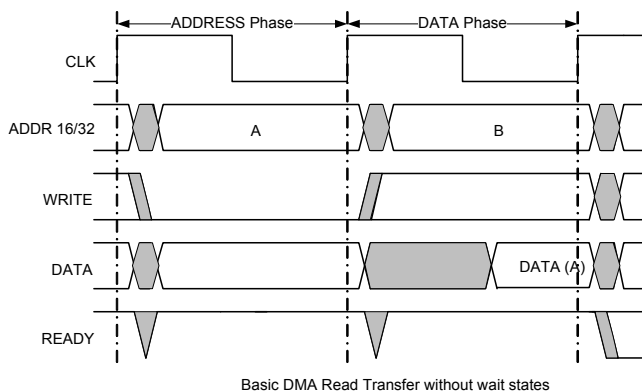
## 4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

### 4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles shown in Figure 4-1. For more description on other transfer modes, refer to the Technical Reference Manual.

**Figure 4-1. DMA Timing Diagram**



### 4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

### 4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the

data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

### 4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

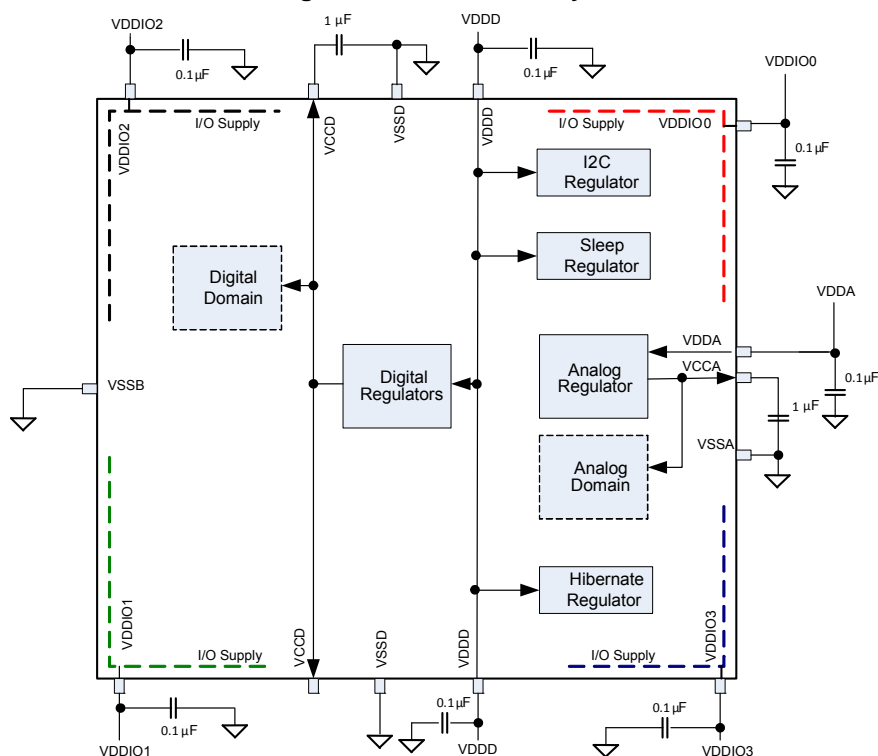


## 6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOx, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the

VDDIO pins must have capacitors connected as shown in [Figure 6-4](#). The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a  $1\text{-}\mu\text{F} \pm 10\% \times 5\text{R}$  capacitor. The power system also contains a sleep regulator, an I<sup>2</sup>C regulator, and a hibernate regulator.

**Figure 6-4. PSoC Power System**

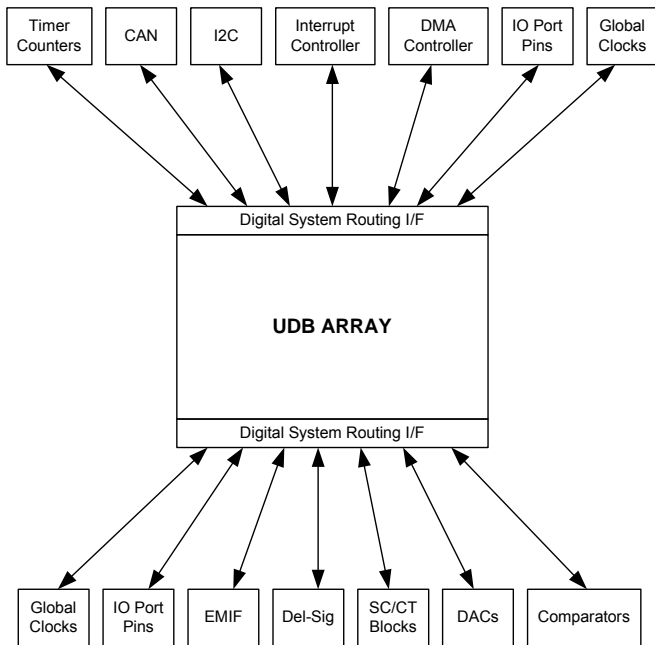


### Notes

- The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in [Figure 2-8](#) on page 12.
- It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (VDDx or VCCx in [Figure 6-4](#)) is a significant percentage of the rated working voltage.
- You can power the device in internally regulated mode, where the voltage applied to the VDDx pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the VCCx pins, and do not tie the VDDx pins to the VCCx pins.**
- You can also power the device in externally regulated mode, that is, by directly powering the VCCD and VCCA pins. In this configuration, the VDDD pins should be shorted to the VCCD pins and the VDDA pin should be shorted to the VCCA pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.

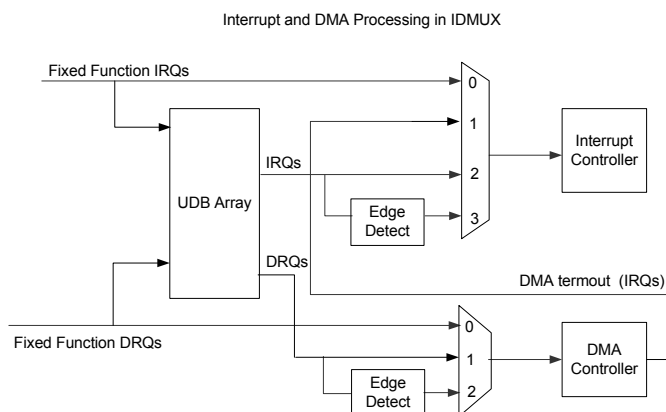


**Figure 7-9. Digital System Interconnect**



Interrupt and DMA routing is very flexible in the CY8C36 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

**Figure 7-10. Interrupt and DMA Processing in the IDMUX**

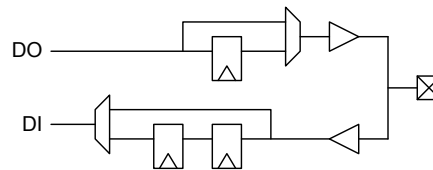


## 7.4.1 I/O Port Routing

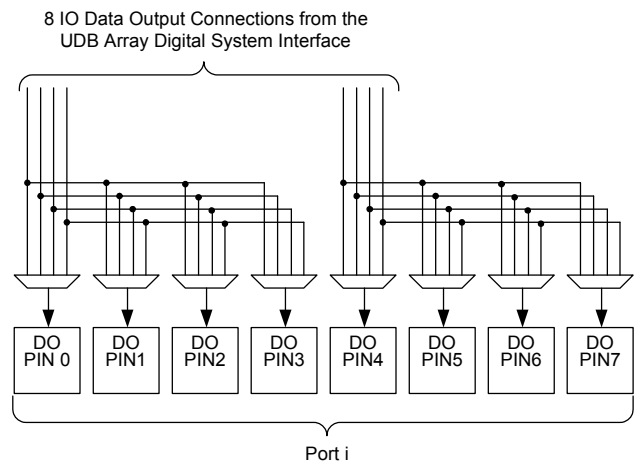
There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the master clock (see Figure 6-1 on page 28). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

**Figure 7-11. I/O Pin Synchronization Routing**



**Figure 7-12. I/O Pin Output Connectivity**



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

## 7.9 Digital Filter Block

Some devices in the CY8C36 family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one bus clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes MCU bandwidth.

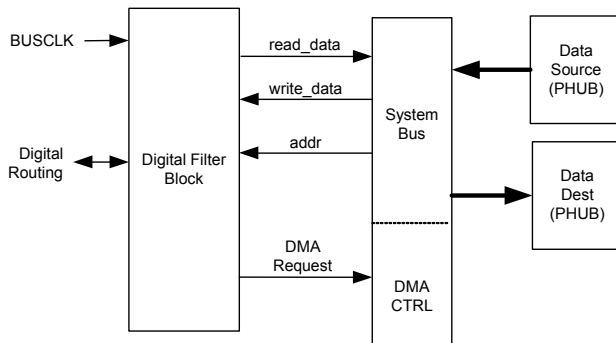
The heart of the DFB is a datapath (DP), which is the numerical calculation unit of the DFB. The DP is a 24-bit fixed-point numerical processor containing a 48-bit multiply and accumulate function (MAC), a multi-function ALU, sample and coefficient data RAMs as well as data routing, shifting, holding and rounding functions.

In the MAC, two 24-bit values can be multiplied and the result added to the 48-bit accumulator in each bus clock cycle. The MAC is the only portion of the DP that is wider than 24 bits. All results from the MAC are passed on to the ALU as 24-bit values representing the high-order 24 bits in the accumulator shifted by one (bits 46:23). The MAC assumes an implied binary point after the most significant bit.

The DP also contains an optimized ALU that supports add, subtract, comparison, threshold, absolute value, squelch, saturation, and other functions. The DP unit is controlled by seven control fields totaling 18 bits coming from the DFB Controller. For more information see the TRM.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

**Figure 7-20. DFB Application Diagram (pwr/gnd not shown)**



The typical use model is for data to be supplied to the DFB over the system bus from another on-chip system data source such as an ADC. The data typically passes through main memory or is directly transferred from another chip resource through DMA. The DFB processes this data and passes the result to another on-chip resource such as a DAC or main memory through DMA on the system bus.

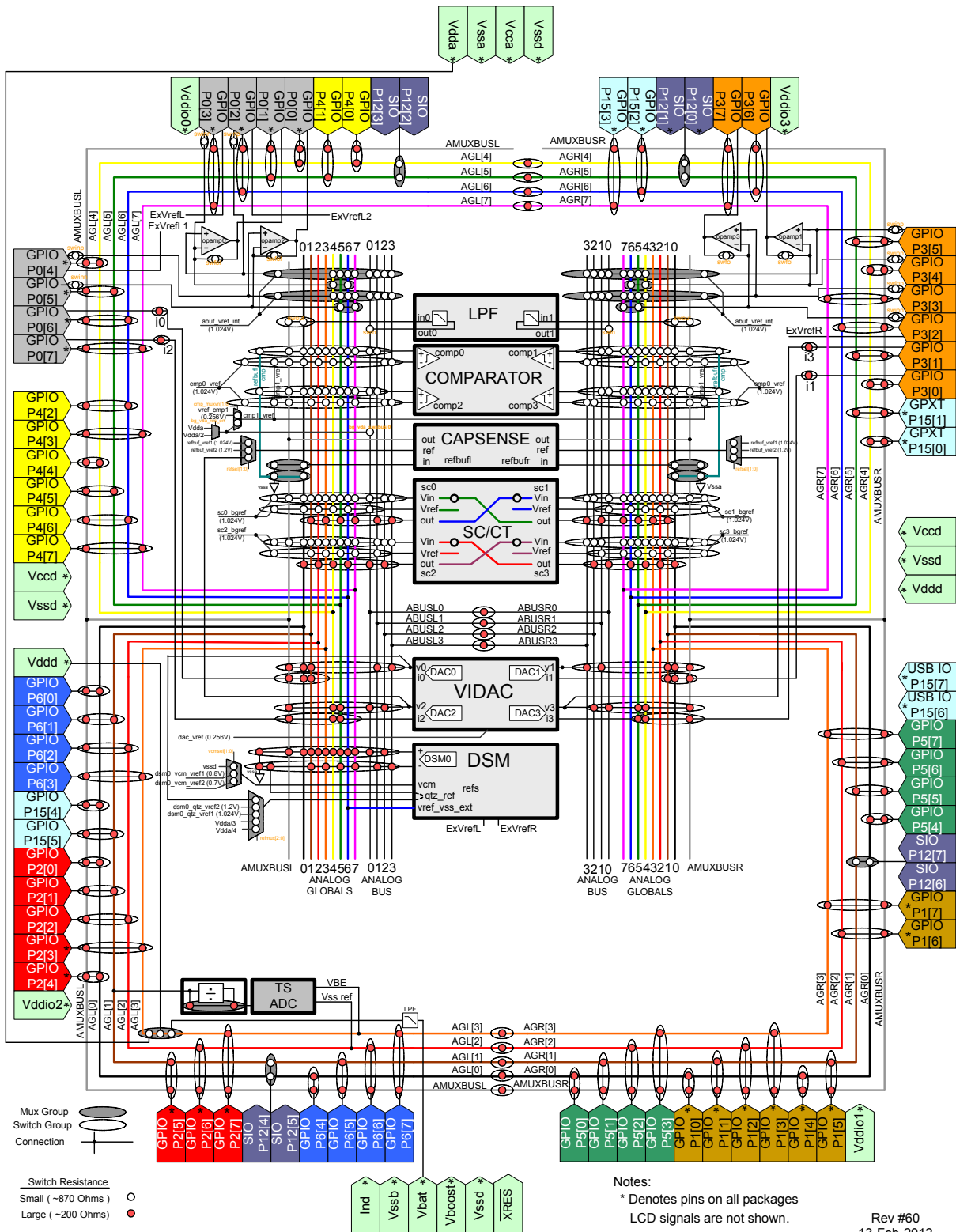
Data movement in or out of the DFB is typically controlled by the system DMA controller but can be moved directly by the MCU.

## 8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution Delta-Sigma ADC.
- Up to four 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.
- Up to four configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer.
- Up to four opamps for internal use and connection to GPIO that can be used as high current output buffers.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

**Figure 8-2. CY8C36 Analog Interconnect**



To preserve detail of this figure, this figure is best viewed with a PDF display program or printed on a 11" × 17" paper.

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in CY8C36, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

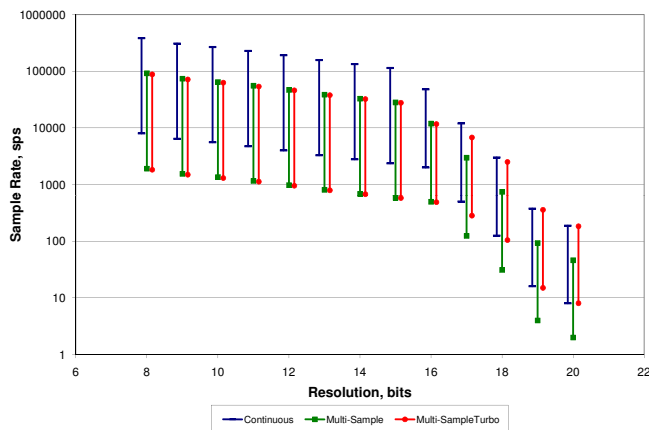
## 8.2 Delta-sigma ADC

The CY8C36 device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for measurement applications. The converter can be configured to output 12-bit resolution at data rates of up to 192 ksp/s. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

**Table 8-1. Delta-sigma ADC Performance**

Bits	Maximum Sample Rate (sps)	SINAD (dB)
12	192 k	66
8	384 k	43

**Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V**

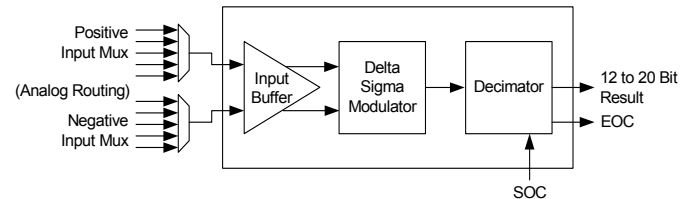


### 8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the

high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is  $[(\sin x)/x]^4$ .

**Figure 8-4. Delta-sigma ADC Block Diagram**



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

### 8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

#### 8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

#### 8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

#### 8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

More information on output formats is provided in the Technical Reference Manual.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- Programmable gain amplifier (PGA) – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

## 8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650  $\mu$ A. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 k $\Omega$ .

## 8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

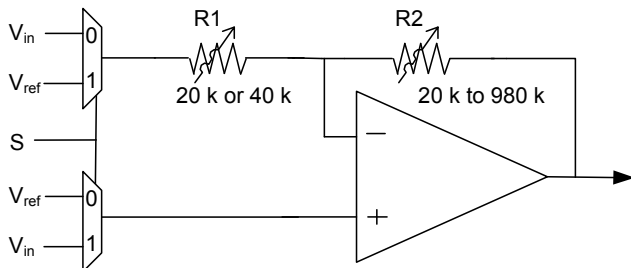
## 8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8 on page 62. The schematic in Figure 8-8 on page 62 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

**Table 8-3. Bandwidth**

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

**Figure 8-8. PGA Resistor Settings**



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

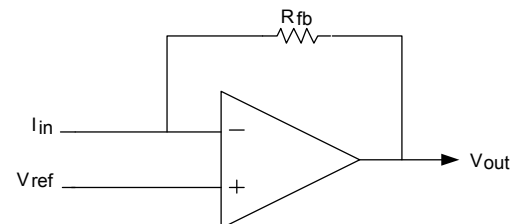
## 8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current  $I_{in}$ , the output voltage is  $V_{REF} - I_{in} \times R_{fb}$ , where  $V_{REF}$  is the value placed on the non inverting input. The feedback resistor  $R_{fb}$  is programmable between 20 K $\Omega$  and 1 M $\Omega$  through a configuration register. Table 8-4 shows the possible values of  $R_{fb}$  and associated configuration settings.

**Table 8-4. Feedback Resistor Settings**

Configuration Word	Nominal $R_{fb}$ (K $\Omega$ )
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

**Figure 8-9. Continuous Time TIA Schematic**



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the  $V_{REF}$  TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

## 8.6 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C36 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

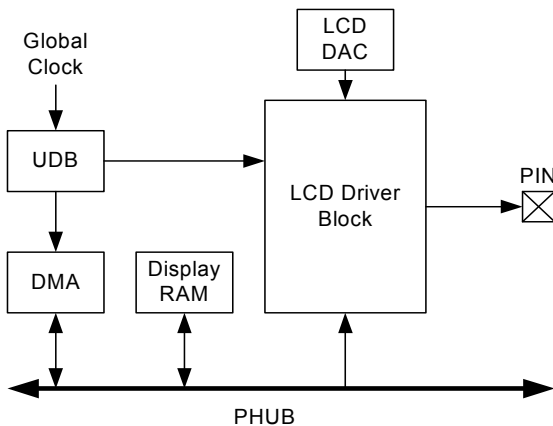


PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

**Figure 8-10. LCD System**



### 8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

### 8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through DMA.

### 8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

### 8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

## 8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, and proximity detection. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator. A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

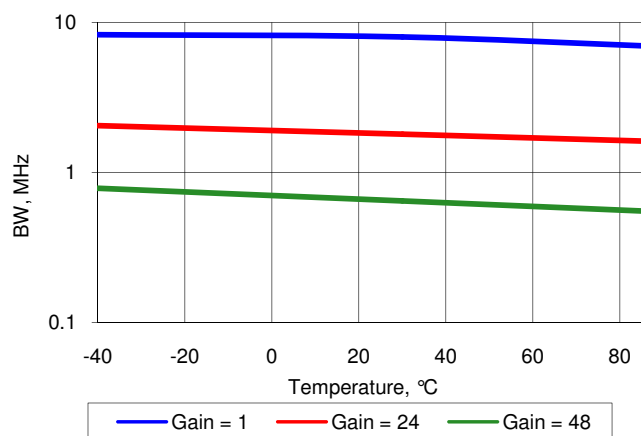
## 8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

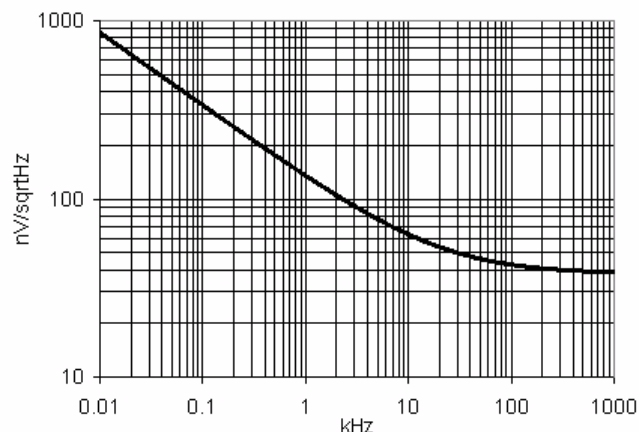
**Table 11-37. PGA AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, input = 100 mV peak-to-peak	6.7	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/μs
e <sub>n</sub>	Input noise density	Power mode = high, V <sub>DDA</sub> = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

**Figure 11-63. Bandwidth vs. Temperature, at Different Gain Settings, Power Mode = High**



**Figure 11-64. Noise vs. Frequency, V<sub>DDA</sub> = 5 V, Power Mode = High**



#### 11.5.11 Temperature Sensor

**Table 11-38. Temperature Sensor Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Temp sensor accuracy	Range: –40 °C to +85 °C	–	±5	–	°C

#### 11.5.12 LCD Direct Drive

**Table 11-39. LCD Direct Drive DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
I <sub>CC</sub>	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 MHz, V <sub>DDIO</sub> = V <sub>DDA</sub> = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	μA
I <sub>CC SEG</sub>	Current per segment driver	Strong drive mode	–	260	–	μA
V <sub>BIAS</sub>	LCD bias range (V <sub>BIAS</sub> refers to the main output voltage(V0) of LCD DAC)	V <sub>DDA</sub> ≥ 3 V and V <sub>DDA</sub> ≥ V <sub>BIAS</sub>	2	–	5	V
	LCD bias step size	V <sub>DDA</sub> ≥ 3 V and V <sub>DDA</sub> ≥ V <sub>BIAS</sub>	–	9.1 × V <sub>DDA</sub>	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I <sub>OUT</sub>	Output drive current per segment driver)	V <sub>DDIO</sub> = 5.5V, strong drive mode	355	–	710	μA

**Table 11-40. LCD Direct Drive AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
f <sub>LCD</sub>	LCD frame rate		10	50	150	Hz



### 11.9.2 Internal Low Speed Oscillator

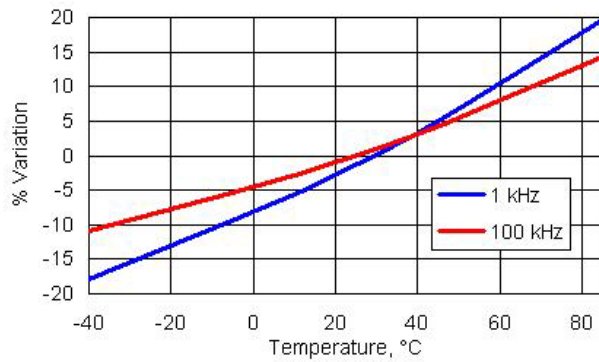
**Table 11-75. ILO DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$I_{CC}$	Operating current <sup>[82]</sup>	$F_{OUT} = 1 \text{ kHz}$	–	–	1.7	$\mu\text{A}$
		$F_{OUT} = 33 \text{ kHz}$	–	–	2.6	$\mu\text{A}$
		$F_{OUT} = 100 \text{ kHz}$	–	–	2.6	$\mu\text{A}$
	Leakage current <sup>[82]</sup>	Power down mode	–	–	15	nA

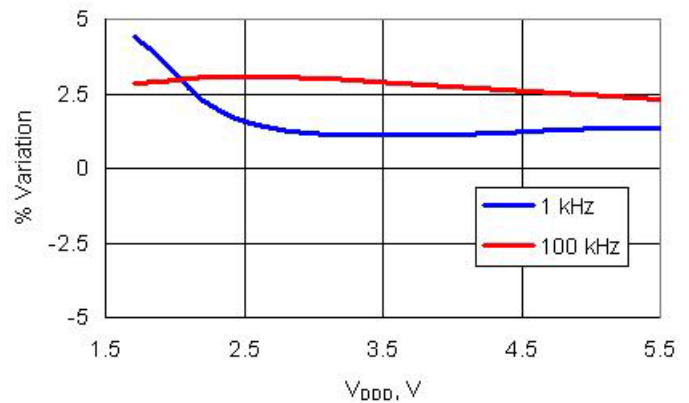
**Table 11-76. ILO AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time, all frequencies	Turbo mode	–	–	2	ms
$F_{ILO}$	ILO frequencies					
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz

**Figure 11-73. ILO Frequency Variation vs. Temperature**



**Figure 11-74. ILO Frequency Variation vs.  $V_{DD}$**



**Note**

82. This value is calculated, not measured.

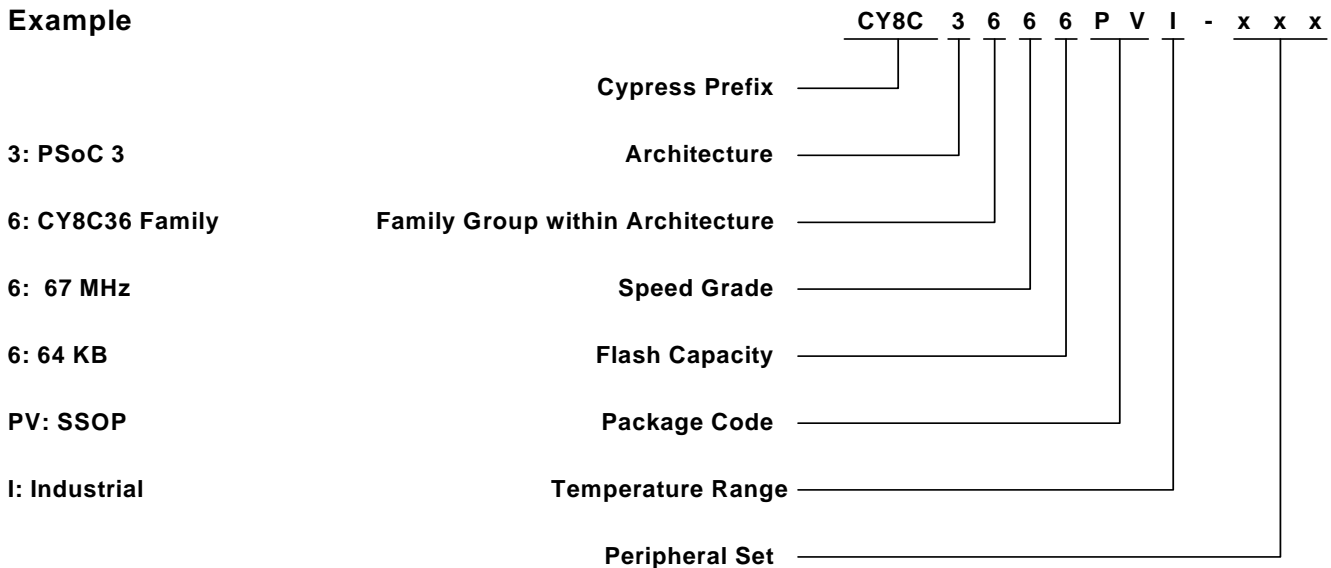
## 12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, ..., 9, A, B, ..., Z) unless stated otherwise.

CY8Cabcdefg-xxx

- **a:** Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- **b:** Family group within architecture
  - 4: CY8C34 family
  - 6: CY8C36 family
  - 8: CY8C38 family
- **c:** Speed grade
  - 4: 48 MHz
  - 6: 67 MHz
- **d:** Flash capacity
  - 4: 16 KB
  - 5: 32 KB
  - 6: 64 KB
- **ef:** Package code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
  - PV: SSOP
  - FN: CSP
- **g:** Temperature range
  - C: commercial
  - I: industrial
  - A: automotive
- **xxx:** Peripheral set
  - Three character numeric
  - No meaning is associated with these three characters.

### Example



Tape and reel versions of these devices are available and are marked with a "T" at the end of the part number.

All devices in the PSoC 3 CY8C36 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration data sheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other "end of life" requirements.

## 13. Packaging

**Table 13-1. Package Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Operating ambient temperature		−40	25.00	85	°C
T <sub>J</sub>	Operating junction temperature		−40	–	100	°C
T <sub>JA</sub>	Package θ <sub>JA</sub> (48-pin SSOP)		–	49	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (48-pin QFN)		–	14	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (68-pin QFN)		–	15	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (100-pin TQFP)		–	34	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (48-pin SSOP)		–	24	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (48-pin QFN)		–	15	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (68-pin QFN)		–	13	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (100-pin TQFP)		–	10	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (72-pin CSP)		–	18	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (72-pin CSP)		–	0.13	–	°C/Watt

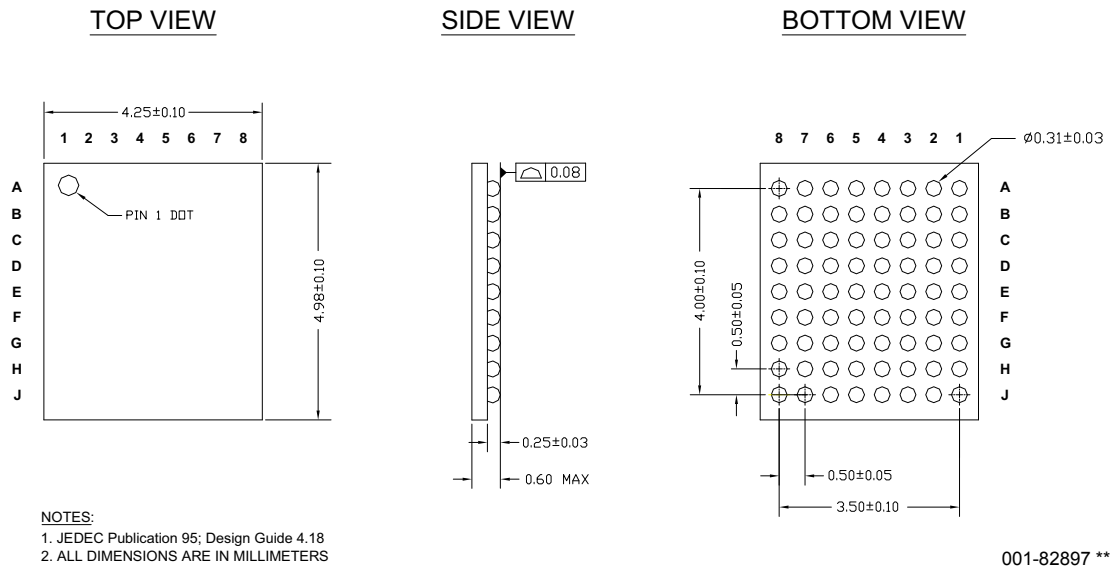
**Table 13-2. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
72-pin CSP	260 °C	30 seconds

**Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
72-pin CSP	MSL 1

**Figure 13-5. WLCSP Package (4.25 × 4.98 × 0.60 mm)**



**Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)**  
**Document Number: 001-53413**

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*P	3732521	09/03/2012	MKEA	<p>Replaced I<sub>DDDR</sub> and I<sub>DDAR</sub> specs in <a href="#">Table 11-2, "DC Specifications,"</a> on page 72 that were dropped out in *N revision.</p> <p>Updated <a href="#">Table 11-32, "Mixer DC Specifications,"</a> on page 102, V<sub>OS</sub> Max value from 10 to 15.</p> <p>Updated <a href="#">Table 11-21, "12-bit Delta-sigma ADC DC Specifications,"</a> on page 91, I<sub>DD 12</sub> Max value from 1.4 to 1.95 mA</p> <p>Replaced PSoC® 3 Programming AN62391 with TRM in footnote #67 and <a href="#">"Programming, Debug Interfaces, Resources"</a> section on page 65</p> <p>Removed Figure 11-8 (Efficiency vs Vout)</p> <p>Updated <a href="#">Table 11-19, "Opamp DC Specifications,"</a> on page 88, I<sub>DD</sub> Quiescent current row values from 200 and 270 to 250 and 400 respectively.</p> <p>Updated conditions for Storage Temperature in <a href="#">Table 11-1, "Absolute Maximum Ratings DC Specifications[22],"</a> on page 71.</p> <p>Updated conditions and min values for NVL data retention time in <a href="#">Table 11-60, "NVL AC Specifications,"</a> on page 110.</p> <p>Updated <a href="#">Table 11-75, "ILO DC Specifications,"</a> on page 118.</p> <p>Removed the following pruned parts from the ordering information table. CY8C3665AXI-010 CY8C3665AXI-016 CY8C3665LTI-044 CY8C3665LTI-006 CY8C3665PVI-007 CY8C3665PVI-080</p> <p>Updated PSoC 3 boost circuit value throughout the document.</p> <p>Removed 100 kHz sub row in <a href="#">Table 11-51, "DFB DC Specifications,"</a> on page 107.</p> <p>Updated package diagram 51-85061 to *F revision.</p>
*Q	3922905	03/25/2013	MKEA	<p>Updated I<sub>DD XX</sub> parameters under <a href="#">Table 11-21, "12-bit Delta-sigma ADC DC Specifications,"</a> on page 91.</p> <p>Updated Temperature Drift specification in <a href="#">Voltage Reference Specifications.</a></p> <p>Added CY8C3665AXI-198, CY8C3665LTI-044, CY8C3665LTI-199, CY8C3666AXI-200, CY8C3666LTI-201, CY8C3666AXI-202, and CY8C3666LTI-203 part numbers in <a href="#">Ordering Information.</a></p> <p>Updated I<sup>2</sup>C section and GPIO and SIO DC specifications tables.</p> <p>Corrected Hibernate max limit.</p> <p>Changed INL max value from ±1.5 to ±1.6 in <a href="#">IDAC DC Specifications.</a></p> <p>Updated ECCEN default setting in <a href="#">Fields and Factory Default Settings.</a></p>
*R	4064707	07/18/2013	MKEA	<p>Added USB test ID in <a href="#">Features.</a></p> <p>Updated schematic in <a href="#">Section 2..</a></p> <p>Added paragraph for device reset warning in <a href="#">Section 5.4.</a></p> <p>Added NVL bit for DEBUG_EN in <a href="#">Section 5.5.</a></p> <p>Updated UDB PLD array diagram in <a href="#">Section 7.2.1.</a></p> <p>Changed Tstartup specs in <a href="#">Section 11.2.1.</a></p> <p>Changed GPIO rise and fall time specs in <a href="#">Section 11.4.</a></p> <p>Added Opamp I<sub>B</sub> spec in <a href="#">Section 11.5.1.</a></p> <p>Added VREF spec condition: pre-assembly and added "box method" to VREF temperature drift spec conditions in <a href="#">Section 11.5.3.</a></p> <p>Added IMO spec condition: pre-assembly in <a href="#">Section 11.9.1.</a></p> <p>Added Appendix for CSP package (preliminary)</p>
*S	4118845	09/10/2013	MKEA	<p>Removed T<sub>STG</sub> spec and added note clarifying maximum storage temperature range in <a href="#">Table 11-1.</a></p> <p>Updated Vos spec conditions and TCvos in <a href="#">Table 11-21.</a></p> <p>Updated F<sub>IMO</sub> spec (3 MHz).</p> <p>Updated 100-TQFP package diagram.</p>

**Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)**  
**Document Number: 001-53413**

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*T	4188568	11/14/2013	MKEA	Added SIO Comparator Specifications. Corrected typo in the $V_{REF}$ parameter in the Voltage Reference Specifications. Added CSP information in Packaging and Ordering Information sections. Updated delta-sigma $V_{OS}$ spec conditions.
*U	4385782	05/21/2014	MKEA	Updated <a href="#">General Description</a> and <a href="#">Features</a> . Added <a href="#">More Information</a> and <a href="#">PSoC Creator</a> sections. Updated 100-pin TQFP package diagram.
*V	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in <a href="#">VDAC DC Specifications</a> . Updated <a href="#">Figure 6-11</a> . Added second note after <a href="#">Figure 6-4</a> . Added a reference to Fig 6-1 in <a href="#">Section 6.1.1</a> and <a href="#">Section 6.1.2</a> . Updated <a href="#">Section 6.2.2</a> . Added <a href="#">Section 7.8.1</a> . Updated Boost specifications.
*W	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of TWRITE from 2 to 10 in EEPROM AC specs table. Changed "Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated <a href="#">Section 11.7.5</a> . Updated Delta-sigma ADC DC Specifications
*X	4932879	09/24/2015	MKEA	Changed the Regulator Output Capacitor min and max from "-" to 0.9 and 1.1, respectively. Added reference to AN54439 in <a href="#">Section 11.9.3</a> . Added MHz ECO DC specs table. Removed references to IPOR rearm issues in <a href="#">Section 6.3.1.1</a> . <a href="#">Table 6-1</a> : Changed DSI Fmax to 33 MHz. <a href="#">Figure 6-1</a> : Changed External I/O or DSI to 0-33 MHz. <a href="#">Table 11-10</a> : Changed Fgpioin Max to 33 MHz. <a href="#">Table 11-12</a> : Changed Fsiopin Max to 33 MHz.
*Y	5322536	06/27/2016	MKEA	Updated <a href="#">More Information</a> . Corrected typos in <a href="#">External Electrical Connections</a> . Added links to CAD Libraries in <a href="#">Section 2</a> .