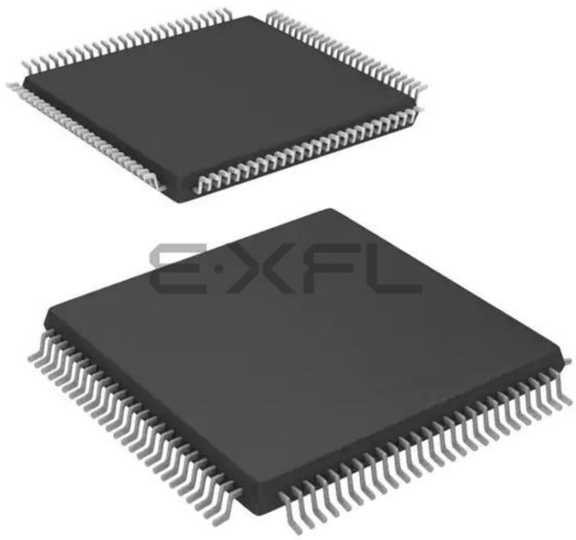


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3666axi-200

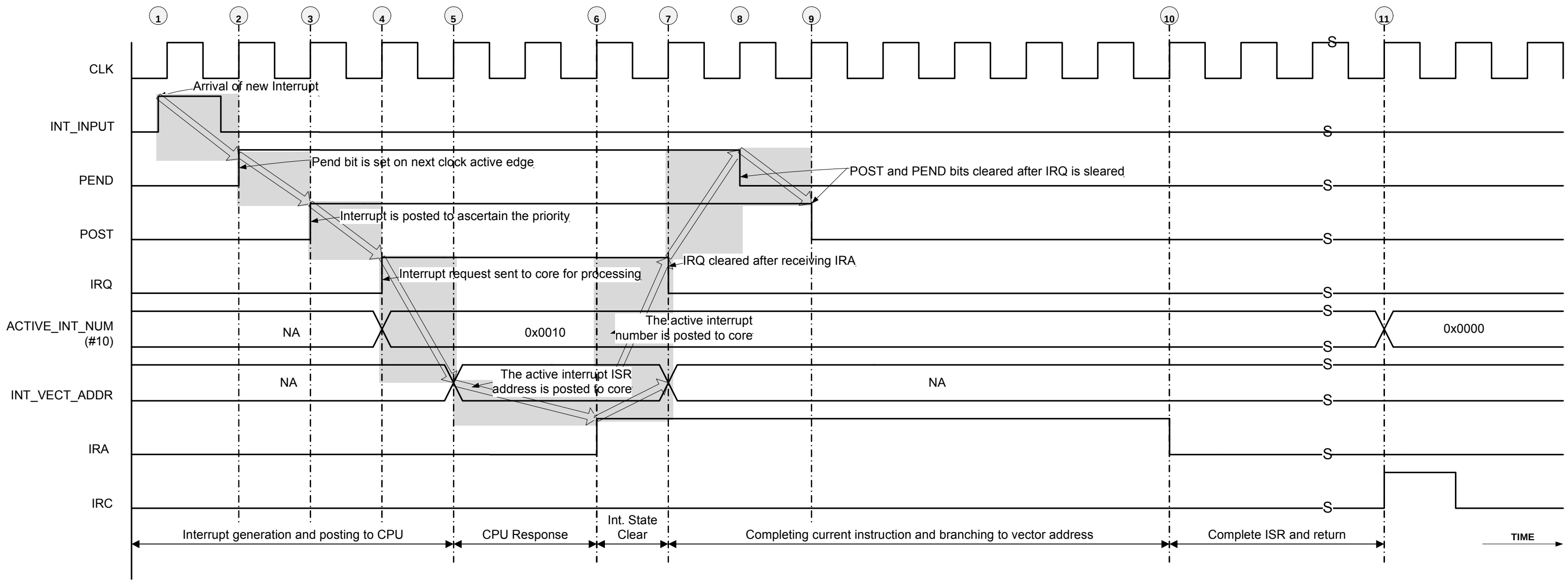
Table 4-3. Data Transfer Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
MOV @Ri, Direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR, #data16	Load data pointer with 16 bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	1	5
MOVC A, @A + PC	Move code byte relative to PC to accumulator	1	4
MOVX A,@Ri	Move external RAM (8-bit) to accumulator	1	4
MOVX A, @DPTR	Move external RAM (16-bit) to accumulator	1	3
MOVX @Ri, A	Move accumulator to external RAM (8-bit)	1	5
MOVX @DPTR, A	Move accumulator to external RAM (16-bit)	1	4
PUSH Direct	Push direct byte onto stack	2	3
POP Direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, Direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low order indirect digit RAM with accumulator	1	3

Table 4-4. Boolean Instructions

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	3
ANL C, bit	AND direct bit to carry	2	2
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

Figure 4-2. Interrupt Processing Timing Diagram



Notes

1: Interrupt triggered asynchronous to the clock

2: The PEND bit is set on next active clock edge to indicate the interrupt arrival

3: POST bit is set following the PEND bit

4: Interrupt request and the interrupt number sent to CPU core after evaluation priority (Takes 3 clocks)

5: ISR address is posted to CPU core for branching

6: CPU acknowledges the interrupt request

7: ISR address is read by CPU for branching

8, 9: PEND and POST bits are cleared respectively after receiving the IRA from core

10: IRA bit is cleared after completing the current instruction and starting the instruction execution from ISR location (Takes 7 cycles)

11: IRC is set to indicate the completion of ISR, Active int. status is restored with previous status

The total interrupt latency (ISR execution)

= POST + PEND + IRQ + IRA + Completing current instruction and branching

= 1+1+1+2+7 cycles

= 12 cycles

Figure 4-3. Interrupt Structure

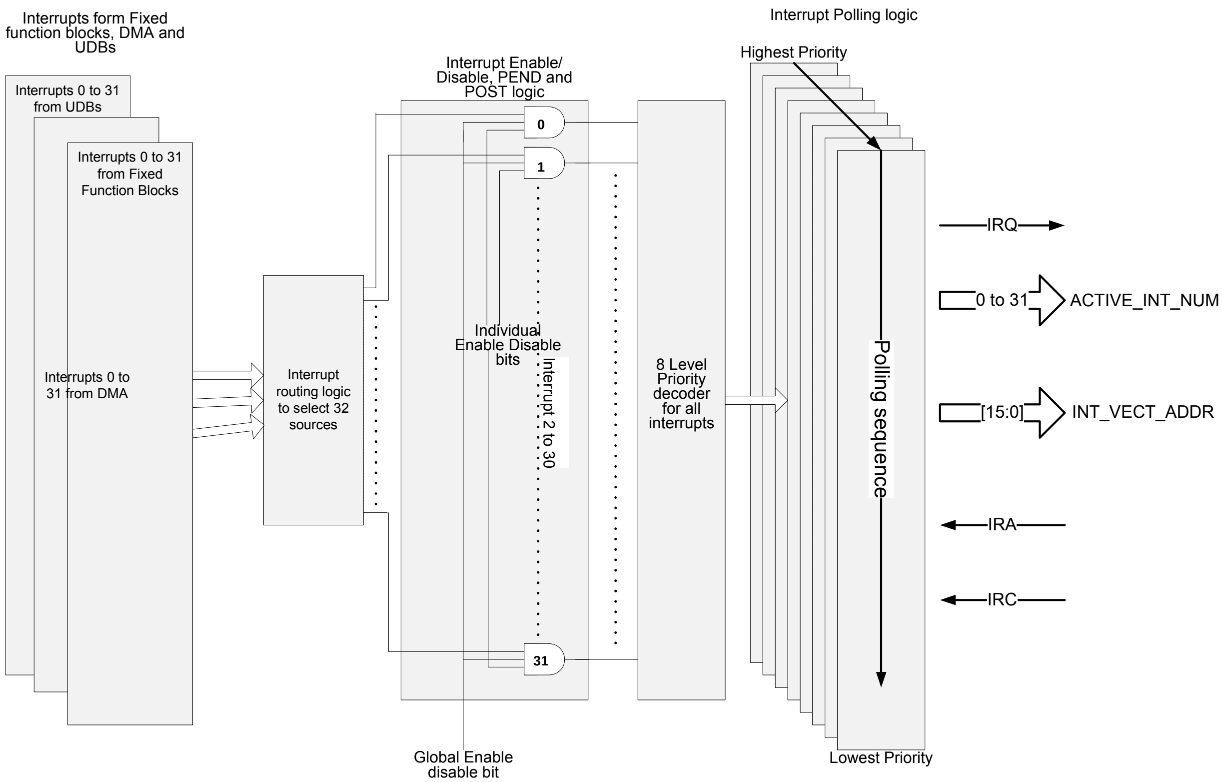


Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^{2}C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]

5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C36 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The factory default values of all EEPROM bytes are 0.

Because the EEPROM is mapped to the 8051 xdata space, the CPU cannot execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

It can take as much as 20 milliseconds to write to EEPROM or flash. During this time the device should not be reset, or unexpected changes may be made to portions of EEPROM or flash. Reset sources (see *Section 6.3.1*) include XRES pin, software reset, and watchdog; care should be taken to make sure that these are not inadvertently activated. In addition, the low voltage detect circuits should be configured to generate an interrupt instead of a reset.

5.5 Nonvolatile Latches (NVLs)

PSoC has a 4-byte array of nonvolatile latches (NVLs) that are used to configure the device at reset. The NVL register map is shown in Table 5-2.

Table 5-2. Device Configuration NVL Register Map

Register Address	7	6	5	4	3	2	1	0
0x00	PRT3RDM[1:0]		PRT2RDM[1:0]		PRT1RDM[1:0]		PRT0RDM[1:0]	
0x01	PRT12RDM[1:0]		PRT6RDM[1:0]		PRT5RDM[1:0]		PRT4RDM[1:0]	
0x02	XRESMEN	DBGEN					PRT15RDM[1:0]	
0x03	DIG_PHS_DLY[3:0]				ECCEN	DPS[1:0]		CFGSPEED

The details for individual fields and their factory default settings are shown in Table 5-3.

Table 5-3. Fields and Factory Default Settings

Field	Description	Settings
PRTxRDM[1:0]	Controls reset drive mode of the corresponding IO port. See "Reset Configuration" on page 43. All pins of the port are set to the same mode.	00b (default) - high impedance analog 01b - high impedance digital 10b - resistive pull up 11b - resistive pull down
XRESMEN	Controls whether pin P1[2] is used as a GPIO or as an external reset. See "Pin Descriptions" on page 12, XRES description.	0 (default for 68-pin 72-pin, and 100-pin parts) - GPIO 1 (default for 48-pin parts) - external reset
DBGEN	Debug Enable allows access to the debug system, for third-party programmers.	0 - access disabled 1 (default) - access enabled
CFGSPEED	Controls the speed of the IMO-based clock during the device boot process, for faster boot or low-power operation	0 (default) - 12 MHz IMO 1 - 48 MHz IMO
DPS[1:0]	Controls the usage of various P1 pins as a debug port. See "Programming, Debug Interfaces, Resources" on page 65.	00b - 5-wire JTAG 01b (default) - 4-wire JTAG 10b - SWD 11b - debug ports disabled
ECCEN	Controls whether ECC flash is used for ECC or for general configuration and data storage. See "Flash Program Memory" on page 23.	0 - ECC disabled 1 (default) - ECC enabled
DIG_PHS_DLY[3:0]	Selects the digital clock phase delay.	See the TRM for details.

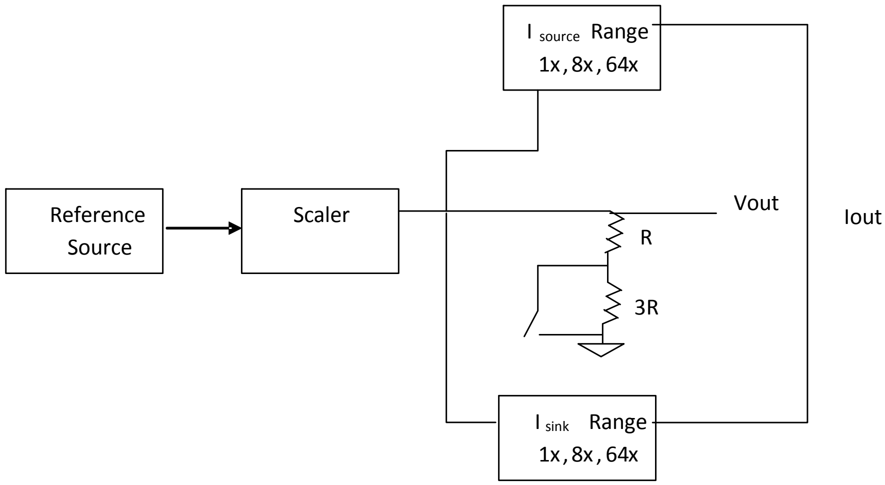
Although PSoC Creator provides support for modifying the device configuration NVLs, the number of NVL erase / write cycles is limited – see "Nonvolatile Latches (NVL))" on page 110.

8.9 DAC

The CY8C36 parts contain up to four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25% of gain error
- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-11. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

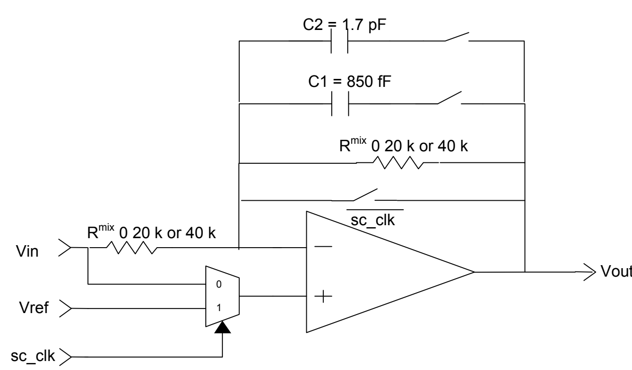
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk – Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-12. Mixer Configuration



9.3 Debug Features

Using the JTAG or SWD interface, the CY8C36 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C36 compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The CY8C36 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0×50536F43) to a Write Once Latch (WOL).

The WOL is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0×50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0×50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 23). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out through the SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

9.8 CSP Package Bootloader

A factory-installed bootloader program is included in all devices with CSP packages. The bootloader is compatible with PSoC Creator 3.0 bootloadable project files and has the following features:

- I^2C-based
- SCLK and SDAT available at P1[6] and P1[7], respectively
- External pull-up resistors required
- I^2C slave, address 4, data rate = 100 kbps
- Single application
- Wait two seconds for bootload command
- Other bootloader options are as set by the PSoC Creator 3.0 Bootloader Component default
- Occupies the bottom 9K of flash

For more information on this bootloader, see the following Cypress application notes:

- AN89611 – PSoC® 3 AND PSoC 5LP - Getting Started With Chip Scale Packages (CSP)
- AN73854 – PSoC 3 and PSoC 5 LP Introduction to Bootloaders
- AN60317 – PSoC 3 and PSoC 5 LP I^2C Bootloader

Note that a PSOC Creator bootloadable project must be associated with .hex and .elf files for a bootloader project that is configured for the target device. Bootloader .hex and .elf files can be found at www.cypress.com/go/PSoC3datasheet.

The factory-installed bootloader can be overwritten using JTAG or SWD programming.

Table 11-7. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor	4.7 µH nominal	3.7	4.7	5.7	µH
		10 µH nominal	8.0	10.0	12.0	µH
		22 µH nominal	17.0	22.0	27.0	µH
C_{BOOST}	Total capacitance sum of V_{DDD}, V_{DDA}, V_{DDIO}[41]		17.0	26.0	31.0	µF
C_{BAT}	Battery filter capacitor		17.0	22.0	27.0	µF
I_F	Schottky diode average forward current		1.0	–	–	A
V_R	Schottky reverse voltage		20.0	–	–	V

Figure 11-8. T_A range over V_{BAT} and V_{OUT}

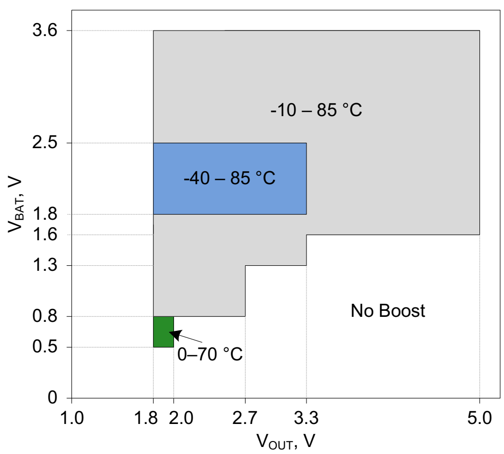


Figure 11-9. I_{OUT} range over V_{BAT} and V_{OUT}

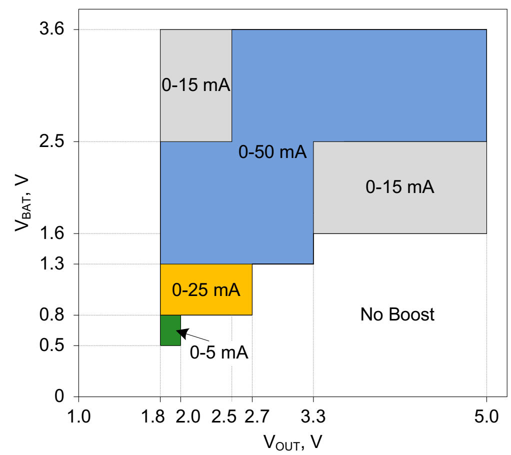
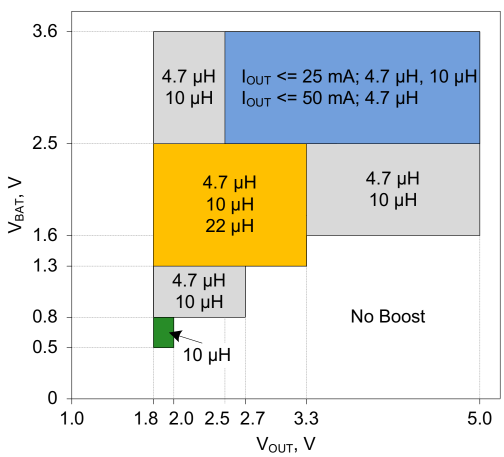


Figure 11-10. L_{BOOST} values over V_{BAT} and V_{OUT}



Note

41. Based on device characterization (Not production tested).

Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode

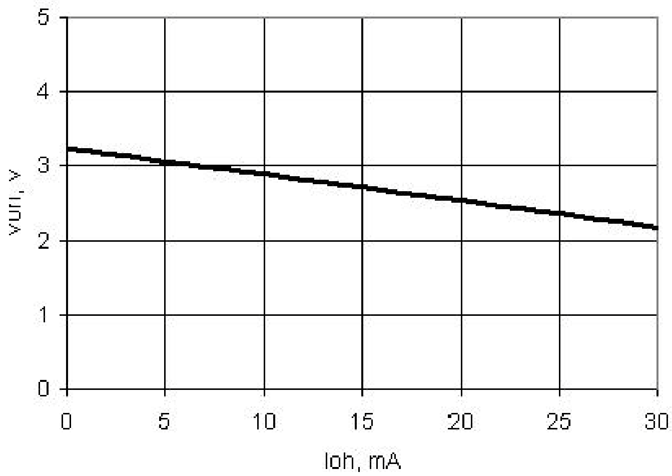


Figure 11-23. USBIO Output Low Voltage and Current, GPIO Mode

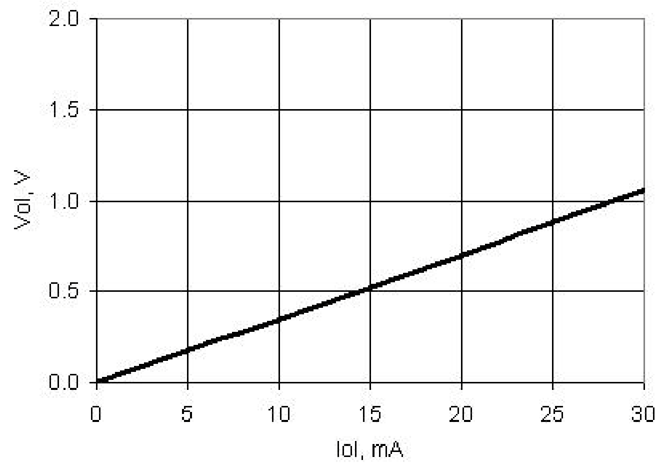


Table 11-15. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	3 V ≤ V_{DDD} ≤ 5.5 V	–	–	20	MHz
		V_{DDD} = 1.71 V	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 1.71 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 1.71 V, 25 pF load	–	–	40	ns

11.5.5 Comparator

Table 11-26. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, V_{DDA} > 2.7 V, Vin ≥ 0.5 V	–		10	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		9	mV
	Input offset voltage in fast mode[60]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[60]	Custom trim	–	–	4	mV
	Input offset voltage in ultra low-power mode	V_{DDA} ≤ 4.6 V	–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA}	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode V_{DDA} ≤ 4.6 V	V_{SSA}	–	V_{DDA} – 1.15	V
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[61]		–	–	400	µA
	Low current mode/slow mode[61]		–	–	100	µA
	Ultra low-power mode[61]	V_{DDA} ≤ 4.6 V	–	6	–	µA

Table 11-27. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode[61]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[61]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low-power mode[61]	50 mV overdrive, measured pin-to-pin, V_{DDA} ≤ 4.6 V	–	55	–	µs

11.5.6 Current Digital-to-analog Converter (IDAC)

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 12 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-28. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I_{OUT}	Output current at code = 255	Range = 2.04 mA, code = 255, V_{DDA} ≥ 2.7 V, Rload = 600 Ω	–	2.04	–	mA
		Range = 2.04 mA, high speed mode, code = 255, V_{DDA} ≤ 2.7 V, Rload = 300 Ω	–	2.04	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	

Notes

60. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.
61. Based on device characterization (Not production tested).

Figure 11-52. VDAC INL vs Temperature, 1 V Mode

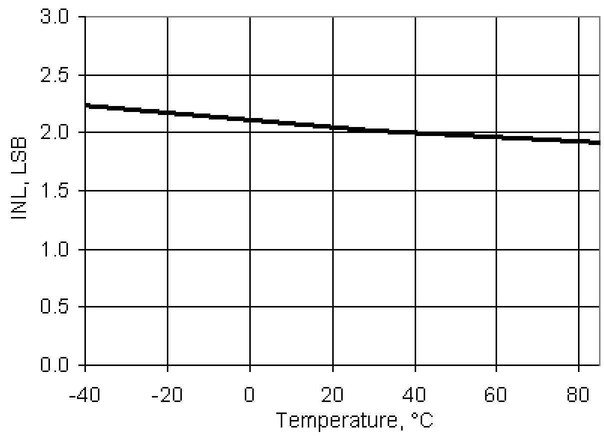


Figure 11-53. VDAC DNL vs Temperature, 1 V Mode

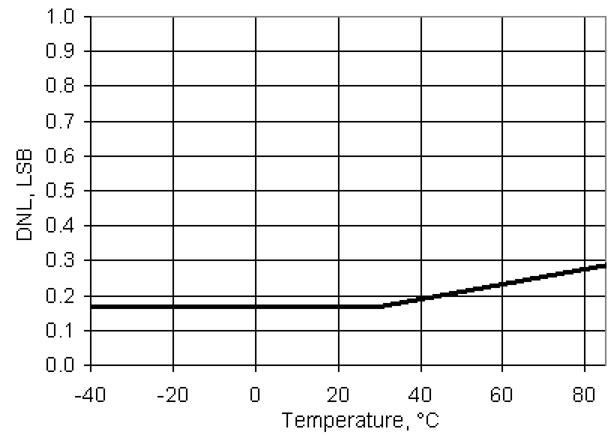


Figure 11-54. VDAC Full Scale Error vs Temperature, 1 V Mode

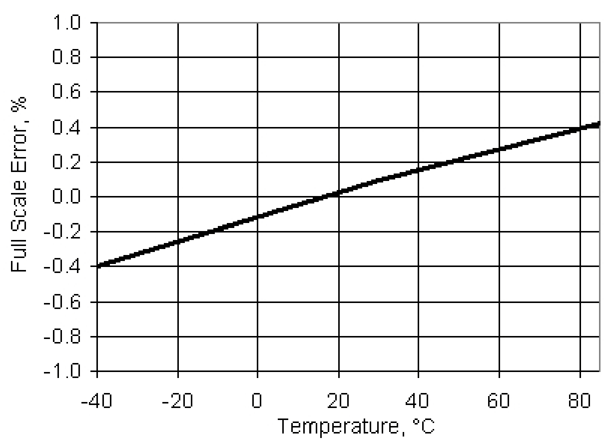


Figure 11-55. VDAC Full Scale Error vs Temperature, 4 V Mode

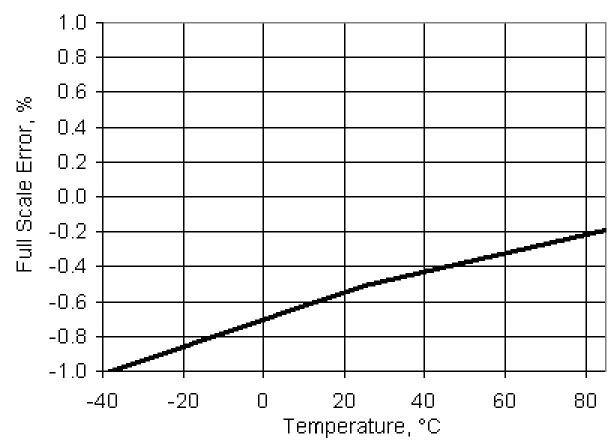


Figure 11-56. VDAC Operating Current vs Temperature, 1V Mode, Low speed mode

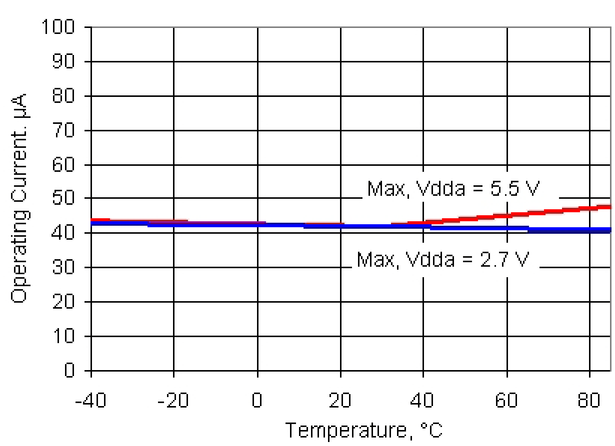


Figure 11-57. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode

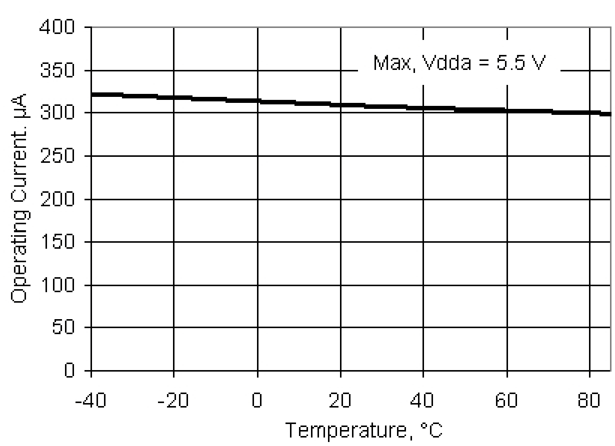


Table 11-31. VDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate	1 V scale	–	–	1000	ksps
		4 V scale	–	–	250	ksps
TsettleP	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.8	3.2	µs
TsettleN	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.7	3	µs
	Voltage noise	Range = 1 V, High speed mode, V_{DDA} = 5 V, 10 kHz	–	750	–	nV/sqrtHz

Figure 11-58. VDAC Step Response, Codes 0x40 - 0xC0, 1 V Mode, High speed mode, V_{DDA} = 5 V

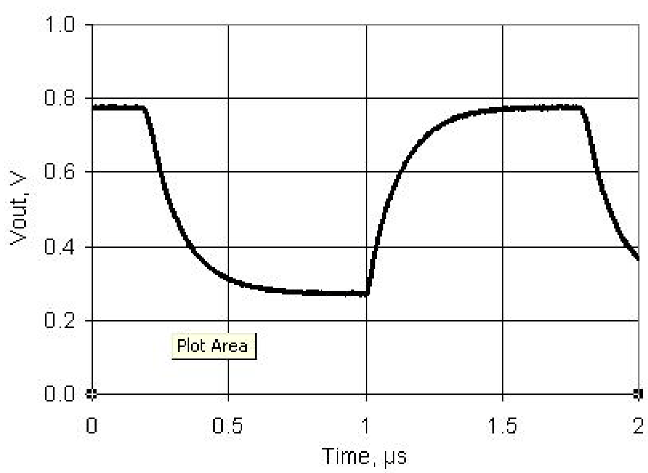


Figure 11-59. VDAC Glitch Response, Codes 0x7F - 0x80, 1 V Mode, High speed mode, V_{DDA} = 5 V

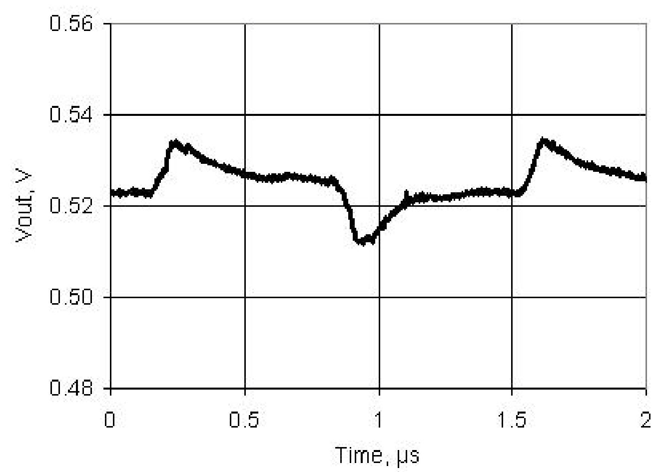


Figure 11-60. VDAC PSRR vs Frequency

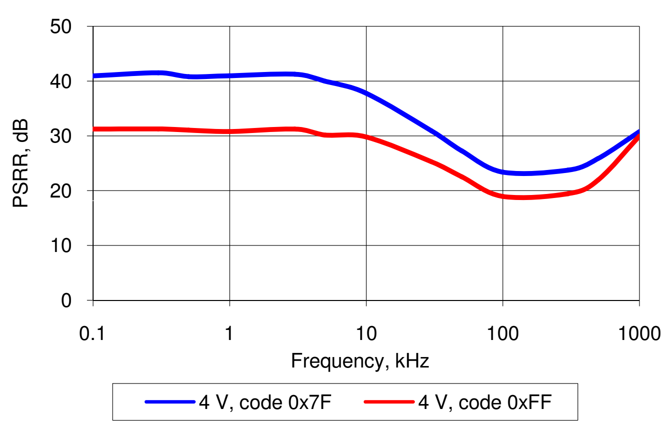
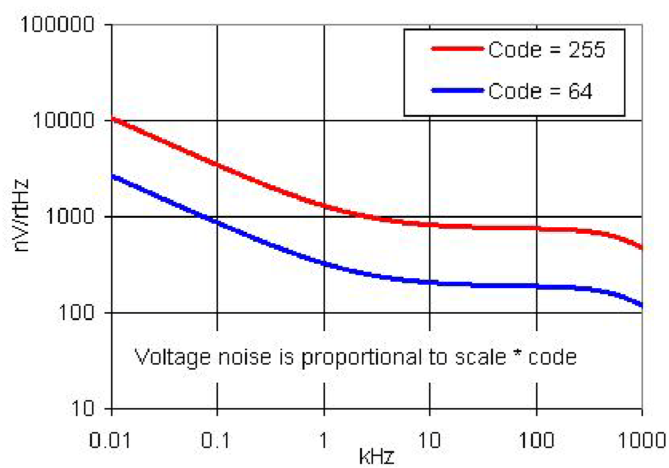


Figure 11-61. VDAC Voltage Noise, 1 V Mode, High speed mode, V_{DDA} = 5 V



11.6.6 Digital Filter Block

Table 11-51. DFB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	DFB operating current	64-tap FIR at F_{DFB}				
		500 kHz (6.7 ksps)	–	0.16	0.27	mA
		1 MHz (13.4 ksps)	–	0.33	0.53	mA
		10 MHz (134 ksps)	–	3.3	5.3	mA
		48 MHz (644 ksps)	–	15.7	25.5	mA
		67 MHz (900 ksps)	–	21.8	35.6	mA

Table 11-52. DFB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DFB}	DFB operating frequency		DC	–	67.01	MHz

11.6.7 USB

Table 11-53. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[66]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

Note

66. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 87.

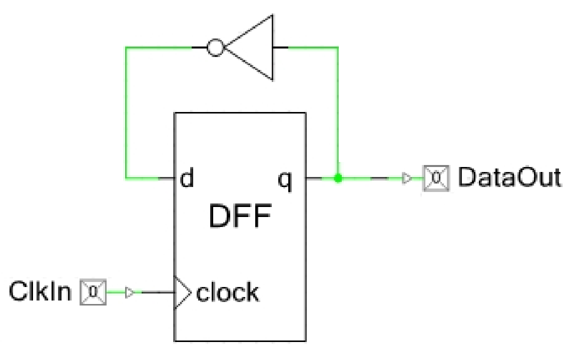
11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-54. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-65.	25 °C, $V_{DDD} \geq 2.7$ V	–	20	25	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-65.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-65. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-55. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-56. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	15	20	ms
T_{ERASE}	Row erase time		–	10	13	ms
	Row program time		–	5	7	ms
T_{BULK}	Bulk erase time (16 KB to 64 KB)		–	–	35	ms
	Sector erase time (8 KB to 16 KB)		–	–	15	ms
T_{PROG}	Total device programming time	No overhead[67]	–	1.5	2	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Average ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	

11.7.2 EEPROM

Table 11-57. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

Table 11-58. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	10	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, T_A ≤ 25 °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	
		Average ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	

Note

67. See PSoC® 3 Device Programming Specifications for a low-overhead method of programming PSoC 3 flash.

11.8 PSoC System Resources

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, V_{DDD} and V_{DDA} must be ≥ 2.0 V. Brown out detect is not available in externally regulated mode.

Table 11-65. Precise Low-Voltage Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

Table 11-66. Power On Reset (POR) with Brown Out AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR	Response time		–	–	0.5	µs
	V_{DDD}/V_{DDA} droop rate	Sleep mode	–	5	–	V/sec

11.8.2 Voltage Monitors

Table 11-67. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage		–	–	–	–
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-68. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Response time[74]		–	–	1	µs

Note
74. Based on device characterization (Not production tested).

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (48-pin SSOP)		–	49	–	°C/Watt
T_{JA}	Package θ_{JA} (48-pin QFN)		–	14	–	°C/Watt
T_{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T_{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin SSOP)		–	24	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin QFN)		–	15	–	°C/Watt
T_{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T_{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt
T_{JA}	Package θ_{JA} (72-pin CSP)		–	18	–	°C/Watt
T_{JC}	Package θ_{JC} (72-pin CSP)		–	0.13	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
72-pin CSP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
72-pin CSP	MSL 1

Figure 13-1. 48-pin (300 mil) SSOP Package Outline

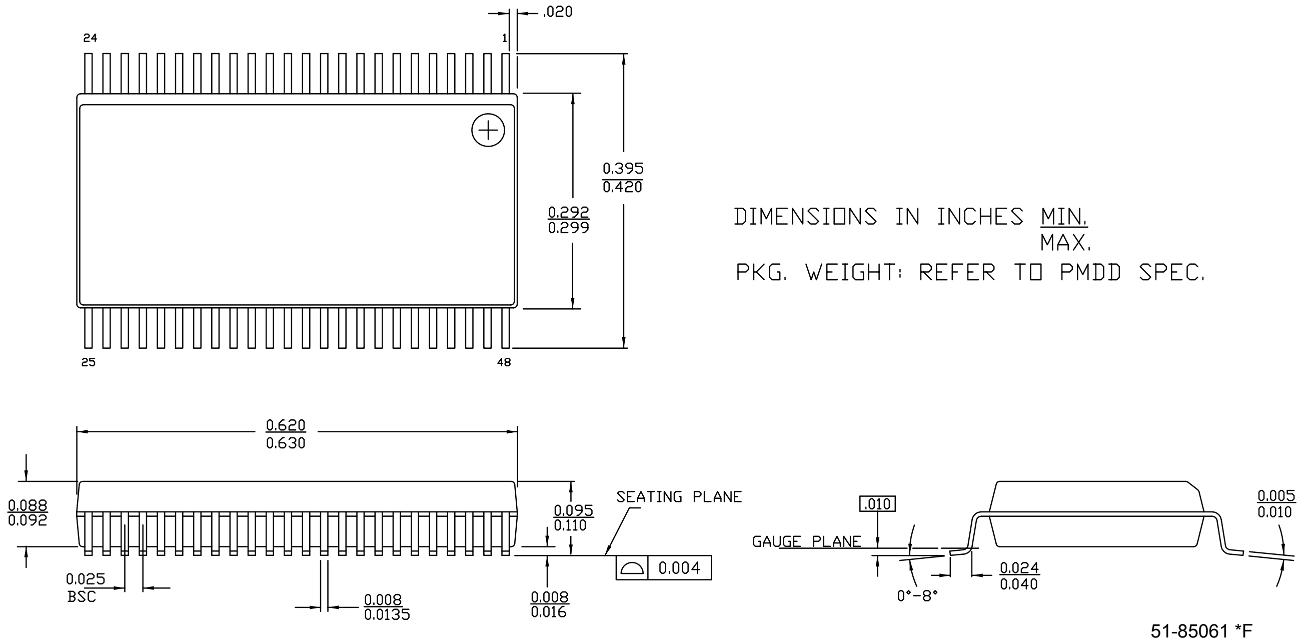
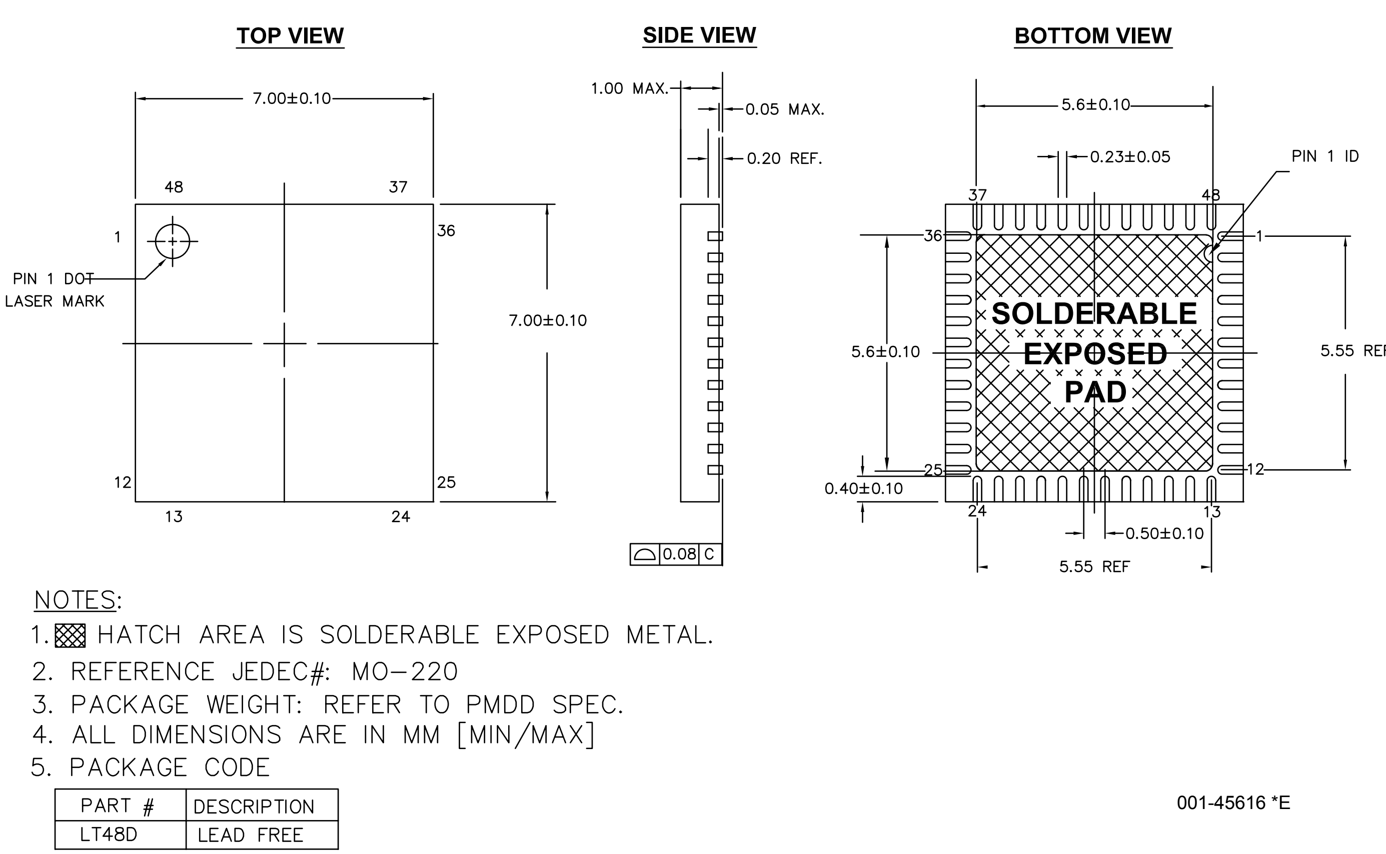


Figure 13-2. 48-pin QFN Package Outline



Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-53413				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*E	2938381	05/27/10	MKEA	Replaced V_{DDIO} with V_{DDD} in USBIO diagram and specification tables, added text in USBIO section of Electrical Specifications. Added Table 13-2 (Package MSL) Modified Tstorag condition and changed max spec to 100 Added bullet (Pass) under ALU (section 7.2.2.2) Added figures for kHzECO and MHzECO in the External Oscillator section Updated Figure 6-1(Clocking Subsystem diagram) Removed CPUCLK_DIV in table 5-2, Deleted Clock Divider SFR subsection Updated PSoC Creator Framework image Updated SIO DC Specifications (V_{IH} and V_{IL} parameters) Updated bullets in Clocking System and Clocking Distribution sections Updated Figure 8-2 Updated PCB Layout and Schematic, updated as per MTRB review comments Updated Table 6-3 (power changed to current) In 32kHZ EC DC Specifications table, changed I_{CC} Max to 0.25 In IMO DC Specifications table, updated Supply Current values Updated GPIO DC Specs table
*F	2958674	06/22/10	SHEA	Minor ECN to post data sheet to external website
*G	2989685	08/04/10	MKEA	Added USBIO 22 ohm DP and DM resistors to Simplified Block Diagram Added to Table 6-6 a footnote and references to same. Added sentences to the resistive pull-up and pull-down description bullets. Added sentence to Section 6.4.11, Adjustable Output Level. Updated section 5.5 External Memory Interface Updated Table 11-73 JTAG Interface AC Specifications Updated Table 11-74 SWD Interface AC Specifications Updated style changes as per the new template.
*H	3078568	11/04/10	MKEA	Updated "Current Digital-to-analog Converter (IDAC)" on page 94 Updated "Voltage Digital to Analog Converter (VDAC)" on page 99 Updated "DC Specifications" on page 72 Updated "Voltage Reference Specifications" on page 93
*I	3107314	12/10/2010	MKEA	Updated delta-sigma tables and graphs. Updated Flash AC specs Formatted table 11.2. Updated interrupt controller table Updated transimpedance amplifier section Updated SIO DC specs table Updated Voltage Monitors DC Specifications table Updated LCD Direct Drive DC specs table Replaced the Discrete Time Mixer and Continuous Time Mixer tables with Mixer DC and AC specs tables Updated ESD_{HBM} value. Updated IDAC and VDAC sections Removed ESO parts from ordering information Changed USBIO pins from NC to DNU and removed redundant USBIO pin description notes Updated POR with brown out DC and AC specs Updated PGA AC specs Updated 32 kHz External Crystal DC Specifications Updated opamp AC specs Updated XRES IO specs Updated Inductive boost regulator section Delta sigma ADC spec updates Updated comparator section Removed buzz mode from Power Mode Transition diagram Updated opamp DC and AC spec tables Updated PGA DC table

Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-53413				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*N	3645908	06/14/2012	MKEA	Added paragraph clarifying that to achieve low hibernate current, you must limit the frequency of IO input signals. Revised description of IPOR and clarified PRES term. Changed footnote to state that all GPIO input voltages - not just analog voltages - must be less than Vddio. Updated 100-TQFP package drawing Clarified description of opamp Iout spec Changed "compliant with I2C" to "compatible with I2C" Updated 48-QFN package drawing Changed reset status register description text to clarify that not all reset sources are in the register Updated example PCB layout figure Removed text stating that FTW is a wakeup source Changed supply ramp rate spec from 1 V/ns to 0.066 V/µs Added "based on char" footnote to voltage monitors response time spec Changed analog global spec descriptions and values Added spec for ESD_{HBM} for when Vssa and Vssd are separate Added a statement about support for JTAG programmers and file formats Changed comparator specs and conditions Added text describing flash cache, and updated related text Changed text and added figures describing Vddio source and sink Added a statement about support for JTAG programmers and file formats. Changed comparator specs and conditions Added text on adjustability of buzz frequency Updated terminology for "master" and "system" clock Deleted the text "debug operations are possible while the device is reset" Deleted and updated text regarding SIO performance under certain power ramp conditions Removed from boost mention of 22 µH inductors. This included deleting some graph figures. Changed DAC high and low speed/power mode descriptions and conditions Changed IMO startup time spec Added text on XRES and PRES re-arm times Added text about usage in externally regulated mode Updated package diagram spec 001-45616 to *D revision. Changed supply ramp rate spec from 1 V/ns to 0.066 V/µs Changed text describing SIO modes for overvoltage tolerance Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions Updated Vref temperature drift specs. Added Vref graphs and footnote. Updated DFB description text Changed load cap conditions in opamp specs Updated del-sig ADC spec tables, to replace three the instances of "16 bit" with "12 bit" Updated package diagram spec 001-45616 to *D revision
*O	3648803	06/18/2012	WKA/ MKEA	No changes. EROS update.