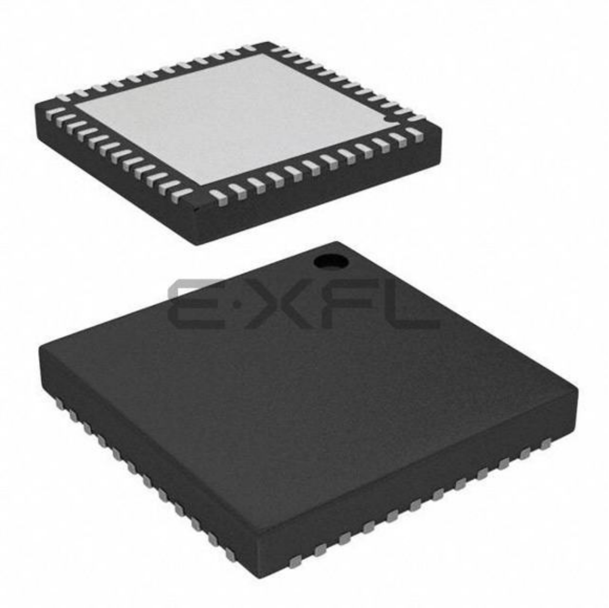
Infineon Technologies - CY8C3666LTI-050 Datasheet



Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3666lti-050

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C36 family these blocks can include four 16-bit timers, counters, and PWM blocks; I^2C slave, master, and multi-master; FS USB; and Full CAN 2.0b.

For more details on the peripherals see the “Example Peripherals” section on page 44 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the “Digital Subsystem” section on page 44 of this data sheet.

PSoC’s analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- ADC
- DACs
- DFB

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100 µV offset
- A gain error of 0.2 percent
- INL less than ±1 LSB
- DNL less than ±1 LSB
- SINAD better than 66 dB

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors.

The output of the ADC can optionally feed the programmable DFB through the DMA without CPU intervention. You can configure the DFB to perform IIR and FIR digital filters and several user-defined custom functions. The DFB can implement filters with up to 64 taps. It can perform a 48-bit multiply-accumulate (MAC) operation in one clock cycle.

Four high-speed voltage or current DACs support 8-bit output signals at an update rate of up to 8 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a PWM DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC, DACs, and DFB, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the “Analog Subsystem” section on page 56 of this data sheet for more details.

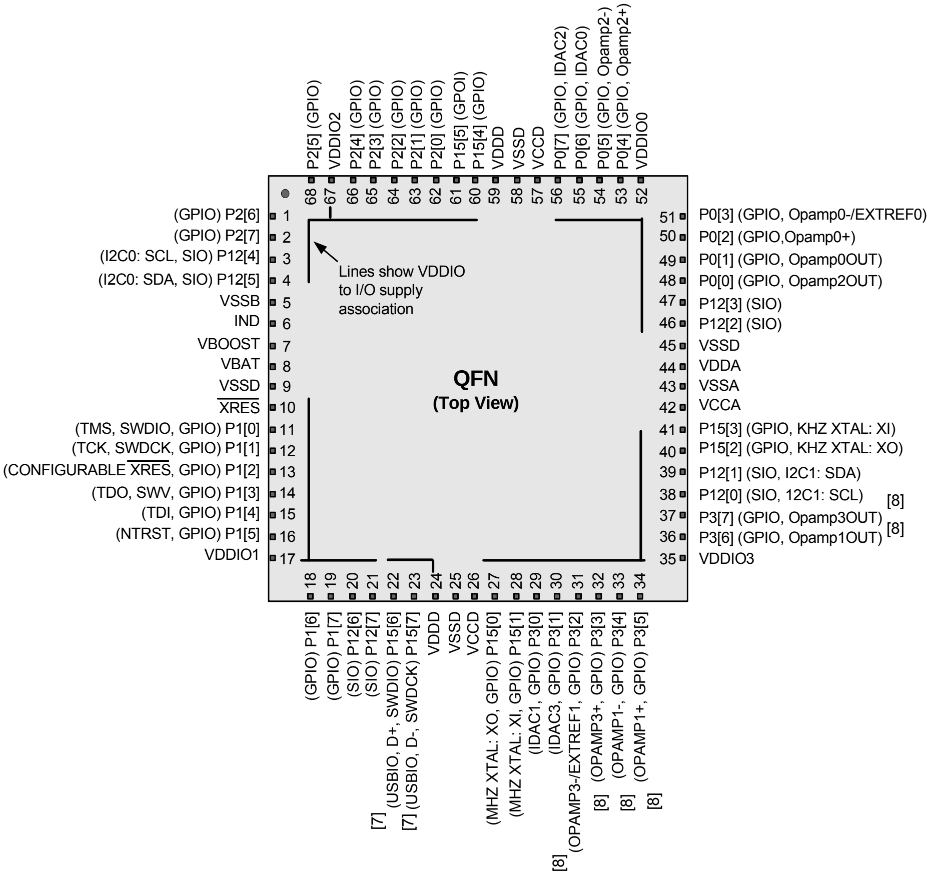
PSoC’s 8051 CPU subsystem is built around a single-cycle pipelined 8051 8-bit processor running at up to 67 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC’s nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC’s nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an ECC for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive[3], CapSense[4], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of V_{DDIO} when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with FS USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the “I/O System and Routing” section on page 37 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The internal main oscillator (IMO) is the clock base for the system, and has 1-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 62 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low-power internal low speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in RTC applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

Figure 2-5. 68-pin QFN Part Pinout[9]



Notes

7. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
8. This feature on select devices only. See Ordering Information on page 120 for details.
9. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see AN72845, Design Guidelines for QFN Devices.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Figure 4-2 on page 21 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 22 shows the interrupt structure and priority polling.

5.7 Memory Map

The CY8C36 8051 memory map is very similar to the MCS-51 memory map.

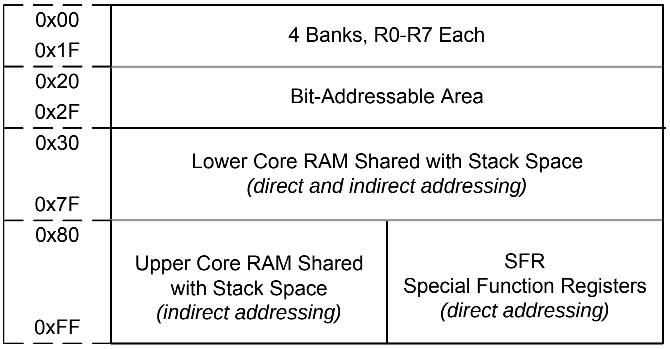
5.7.1 Code Space

The CY8C36 8051 code space is 64 KB. Only main flash exists in this space. See the “Flash Program Memory” section on page 23.

5.7.2 Internal Data Space

The CY8C36 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in “Static RAM” on page 23) and a 128-byte space for Special Function Registers (SFRs). See Figure 5-2. The lowest 32 bytes are used for four banks of registers R0-R7. The next 16 bytes are bit-addressable.

Figure 5-2. 8051 Internal Data Space



In addition to the register or bit address modes used with the lower 48 bytes, the lower 128 bytes can be accessed with direct or indirect addressing. With direct addressing mode, the upper 128 bytes map to the SFRs. With indirect addressing mode, the upper 128 bytes map to RAM. Stack operations use indirect addressing; the 8051 stack space is 256 bytes. See the “Addressing Modes” section on page 14.

5.7.3 SFRs

The special function register (SFR) space provides access to frequently accessed registers. The memory map for the SFR memory space is shown in Table 5-4.

Table 5-4. SFR Map

Address	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0×F8	SFRPRT15DR	SFRPRT15PS	SFRPRT15SEL	–	–	–	–	–
0×F0	B	–	SFRPRT12SEL	–	–	–	–	–
0×E8	SFRPRT12DR	SFRPRT12PS	MXAX	–	–	–	–	–
0×E0	ACC	–	–	–	–	–	–	–
0×D8	SFRPRT6DR	SFRPRT6PS	SFRPRT6SEL	–	–	–	–	–
0×D0	PSW	–	–	–	–	–	–	–
0×C8	SFRPRT5DR	SFRPRT5PS	SFRPRT5SEL	–	–	–	–	–
0×C0	SFRPRT4DR	SFRPRT4PS	SFRPRT4SEL	–	–	–	–	–
0×B8	–	–	–	–	–	–	–	–
0×B0	SFRPRT3DR	SFRPRT3PS	SFRPRT3SEL	–	–	–	–	–
0×A8	IE	–	–	–	–	–	–	–
0×A0	P2AX	–	SFRPRT1SEL	–	–	–	–	–
0×98	SFRPRT2DR	SFRPRT2PS	SFRPRT2SEL	–	–	–	–	–
0×90	SFRPRT1DR	SFRPRT1PS	–	DPX0	–	DPX1	–	–
0×88	–	SFRPRT0PS	SFRPRT0SEL	–	–	–	–	–
0×80	SFRPRT0DR	SP	DPL0	DPH0	DPL1	DPH1	DPS	–

The CY8C36 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C36 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C36 family.

6. System Integration

6.1 Clocking System

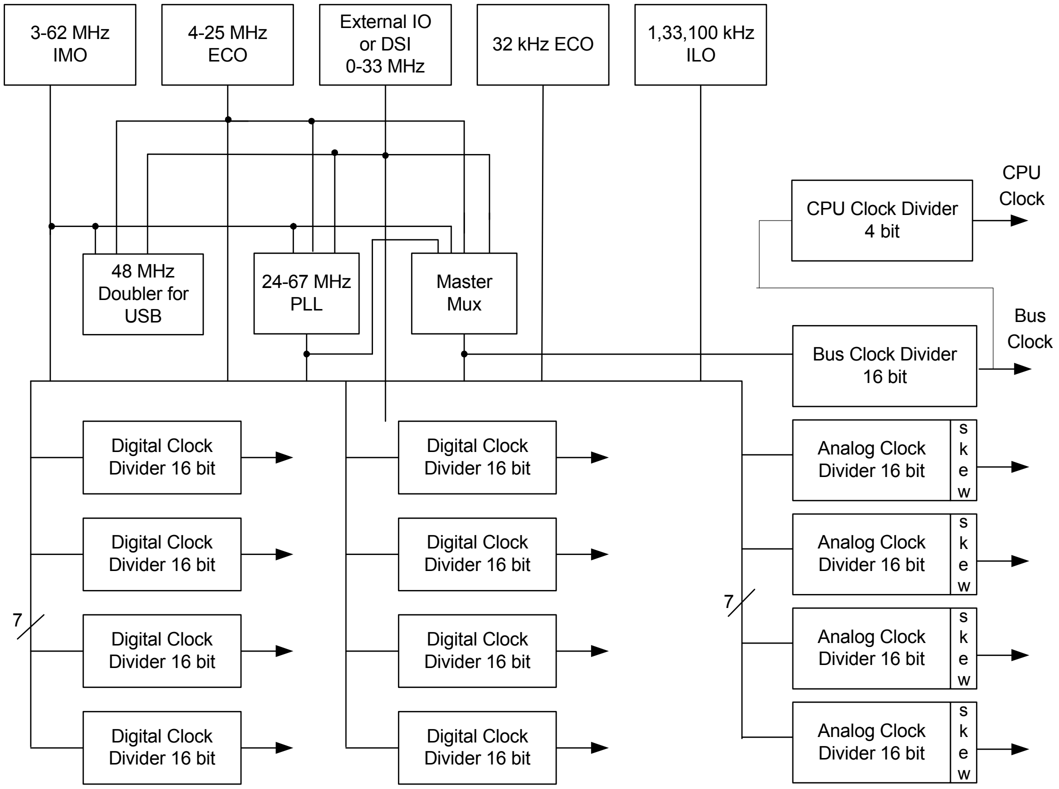
The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 66 MHz clock, accurate to ±1% over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. Any of the clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows you to build clocking systems with minimal input. You can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent in PSoC.

Key features of the clocking system include:

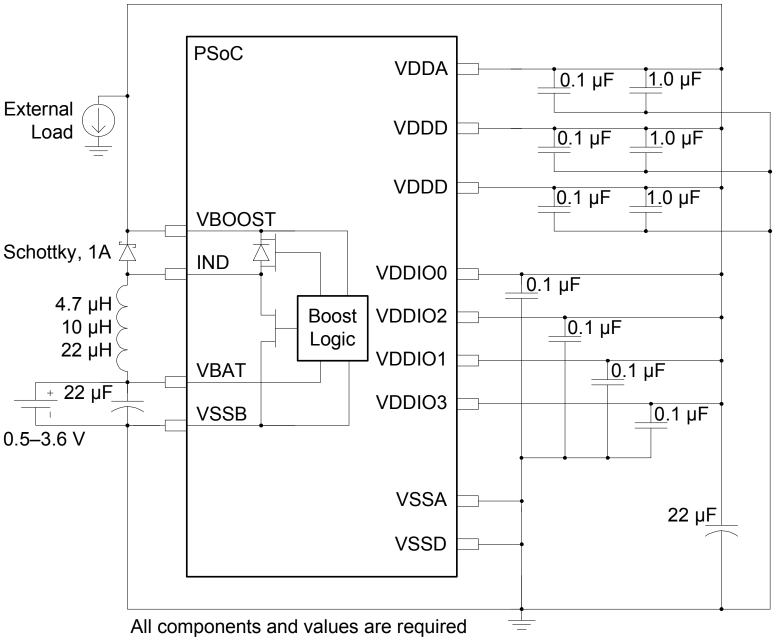
- Seven general purpose clock sources
  - 3- to 62-MHz IMO, ±1% at 3 MHz
  - 4- to 25-MHz external crystal oscillator (MHzECO)
  - Clock doubler provides a doubled clock frequency output for the USB block, see USB Clock Domain on page 30.
  - DSI signal from an external I/O pin or other logic
  - 24- to 67-MHz fractional PLL sourced from IMO, MHzECO, or DSI
  - 1-kHz, 33-kHz, 100-kHz ILO for WDT and sleep timer
  - 32.768-kHz external crystal oscillator (kHzECO) for RTC
- IMO has a USB mode that auto locks to the USB bus clock requiring no external crystal for USB. (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the bus clock
- Dedicated 4-bit divider for the CPU clock
- Automatic clock configuration in PSoC Creator

Figure 6-1. Clocking Subsystem



must be rated for a minimum of 10 V to minimize capacitive losses due to voltage de-rating.

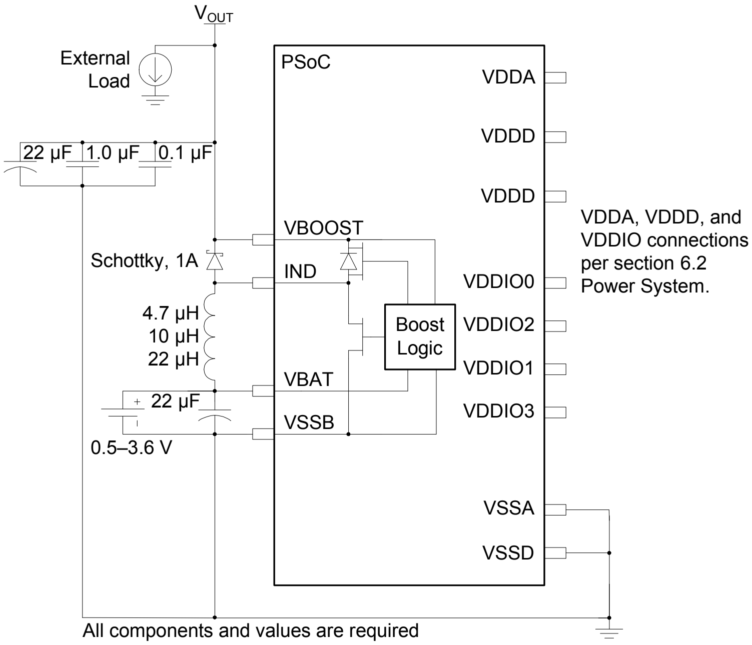
Figure 6-6. Application of Boost Converter powering PSoC device



All components and values are required

The boost converter may also generate a supply that is not used directly by the PSoC device. An example of this use case is boosting a 1.8 V supply to 4.0 V to drive a white LED. If the boost converter is not supplying the PSoC devices V_{DDA}, V_{DDD}, and V_{DDIO} it must comply with the same design rules as supplying the PSoC device, but with a change to the bulk capacitor requirements. A parallel arrangement 22 µF, 1.0 µF, and 0.1 µF capacitors are all required on the Vout supply and must be placed within 1 cm of the VBOOST pin to ensure regulator stability.

Figure 6-7. Application of Boost Converter not powering PSoC device



All components and values are required

The USBIO pins (P15[7] and P15[6]), when enabled for I/O mode, have limited drive mode control. The drive mode is set using the PRT15.DM0[7, 6] register. A resistive pull option is also available at the USBIO pins, which can be enabled using the PRT15.DM1[7, 6] register. When enabled for USB mode, the drive mode control has no impact on the configuration of the USB pins. Unlike the GPIO and SIO configurations, the port wide configuration registers do not configure the USB drive mode bits. Table 6-4 shows the drive mode configuration for the USBIO pins.

Table 6-4. USBIO Drive Modes (P15[7] and P15[6])

PRT15.DM1[7,6] Pull up enable	PRT15.DM0[7,6] Drive Mode enable	PRT15.DR[7,6] = 1	PRT15.DR[7,6] = 0	Description
0	0	High Z	Strong Low	Open Drain, Strong Low
0	1	Strong High	Strong Low	Strong Outputs
1	0	Res High (5k)	Strong Low	Resistive Pull Up, Strong Low
1	1	Strong High	Strong Low	Strong Outputs

- High Impedance Analog

  The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

  To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

- High Impedance Digital

  The input buffer is enabled for digital signal input. This is the standard high impedance (HiZ) state recommended for digital inputs.

- Resistive pull-up or resistive pull-down

  Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

- Open Drain, Drives High and Open Drain, Drives Low

  Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I^{2}C bus signal lines.

- Strong Drive

  Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

- Resistive pull-up and pull-down

  Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRT×SLW registers.

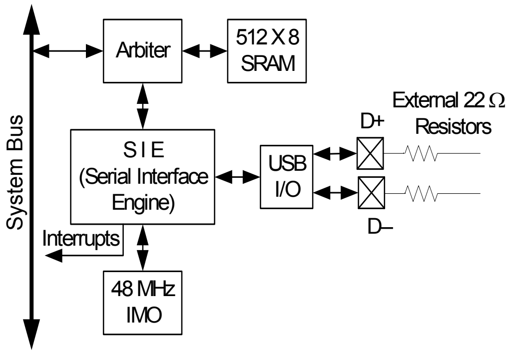
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the “I/O System and Routing” section on page 37.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
  - Automatic Memory Management with Automatic DMA Access
- Internal 3.3-V regulator for transceiver
- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-16. USB



7.7 Timers, Counters, and PWMs

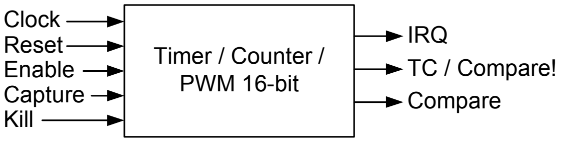
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-17. Timer/Counter/PWM

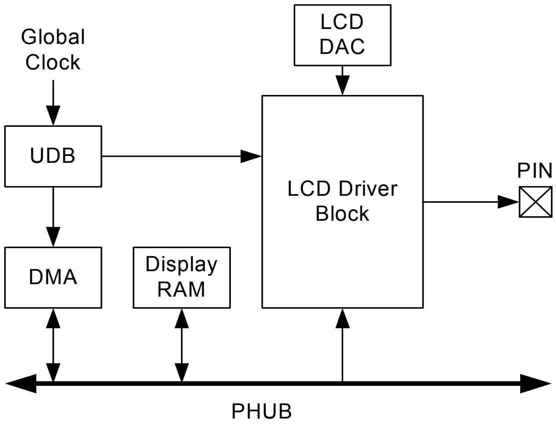


PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-10. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, and proximity detection. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator. A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

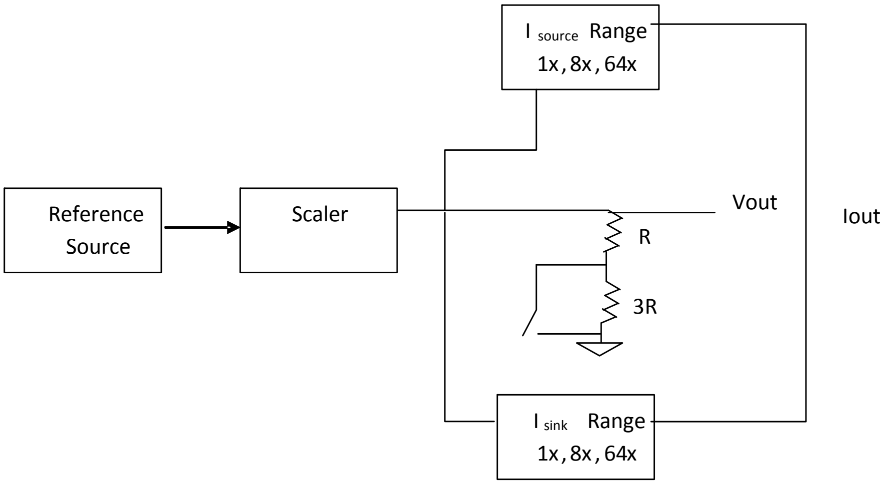
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.9 DAC

The CY8C36 parts contain up to four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25% of gain error
- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-11. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

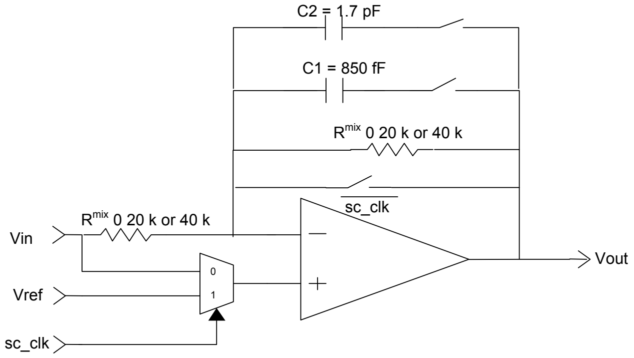
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk – Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-12. Mixer Configuration



11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	± 10%, ×5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 31	0.9	1	1.1	µF

Figure 11-5. Regulators V_{CC} vs V_{DD}

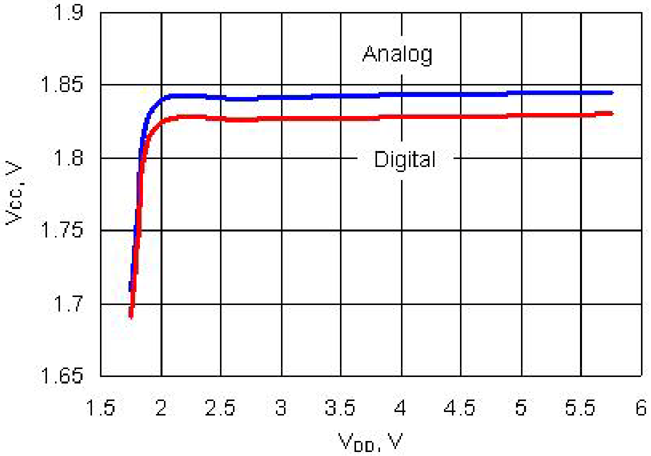
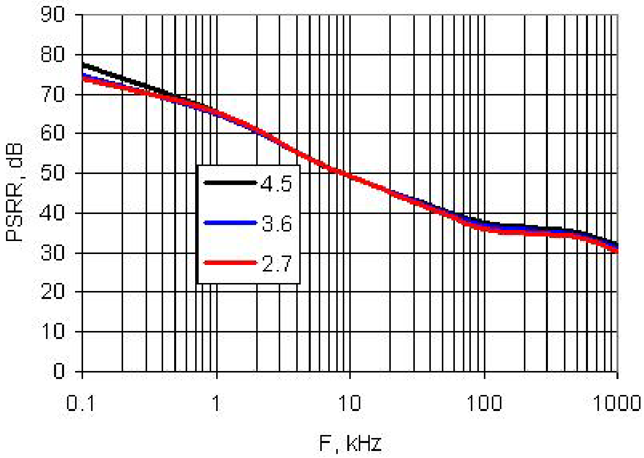


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}

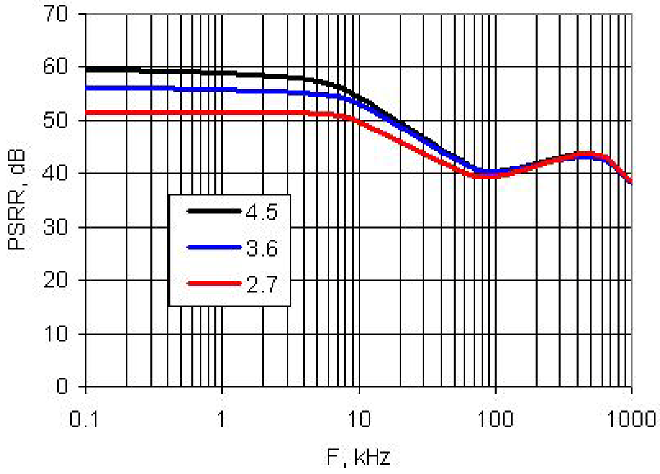


11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, ×5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}



11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: V_{BAT} = 0.5 V–3.6 V, V_{OUT} = 1.8 V–5.0 V, I_{OUT} = 0 mA–50 mA, L_{BOOST} = 4.7 µH–22 µH, C_{BOOST} = 22 µF || 3 × 1.0 µF || 3 × 0.1 µF, C_{BAT} = 22 µF, I_F = 1.0 A. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Boost output voltage[38]	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V_{BAT}	Input voltage to boost[39]	I_{OUT} = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T_A = 0 °C–70 °C	0.5	–	0.8	V
		I_{OUT} = 0 mA–15 mA	vsel = 1.8 V–5.0 V[40], T_A = –10 °C–85 °C	1.6	–	3.6	V
		I_{OUT} = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T_A = –10 °C–85 °C	0.8	–	1.6	V
		I_{OUT} = 0 mA–50 mA	vsel = 1.8 V–3.3 V[40], T_A = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V[40], T_A = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V[40], T_A = –10 °C–85 °C	2.5	–	3.6	V
I_{OUT}	Output current	T_A = 0 °C–70 °C	V_{BAT} = 0.5 V–0.8 V	0	–	5	mA
		T_A = –10 °C–85 °C	V_{BAT} = 1.6 V–3.6 V	0	–	15	mA
			V_{BAT} = 0.8 V–1.6 V	0	–	25	mA
			V_{BAT} = 1.3 V–2.5 V	0	–	50	mA
			V_{BAT} = 2.5 V–3.6 V	0	–	50	mA
		T_A = –40 °C–85 °C	V_{BAT} = 1.8 V–2.5 V	0	–	50	mA
I_{LPK}	Inductor peak current			–	–	700	mA
I_Q	Quiescent current	Boost active mode		–	250	–	µA
		Boost sleep mode, I_{OUT} < 1 µA		–	25	–	µA
Reg_{LOAD}	Load regulation			–	–	10	%
Reg_{LINE}	Line regulation			–	–	10	%

Notes

38. Listed vsel options are characterized. Additional vsel options are valid and guaranteed by design.
39. The boost will start at all valid V_{BAT} conditions including down to V_{BAT} = 0.5 V.
40. If V_{BAT} is greater than or equal to V_{OUT} boost setting, then V_{OUT} will be less than V_{BAT} due to resistive losses in the boost circuit.

Figure 11-36. IDAC INL vs Input Code, Range = 255 µA, Source Mode

Figure 11-37. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

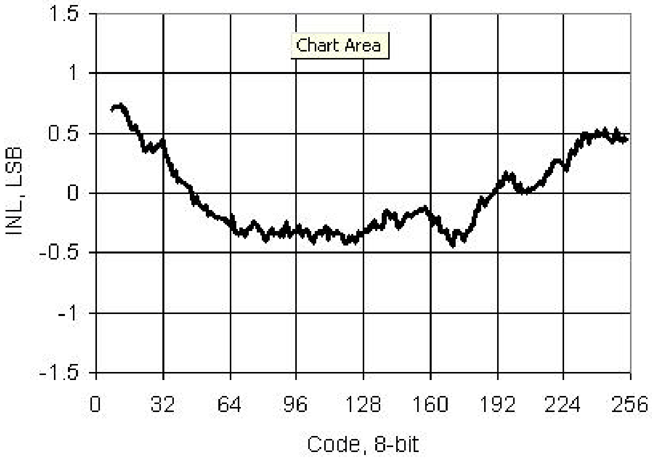


Figure 11-38. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

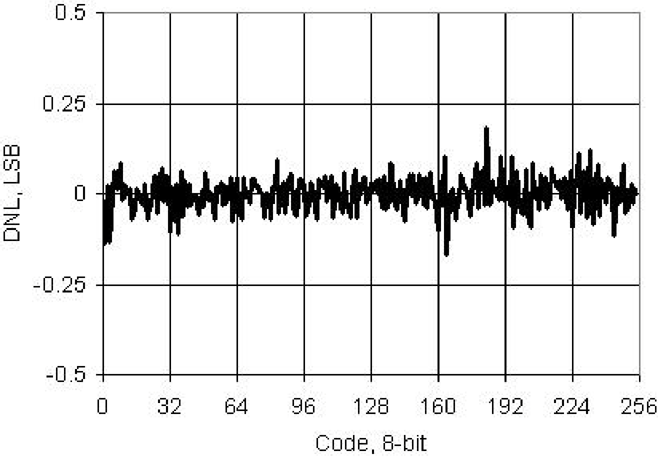


Figure 11-39. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

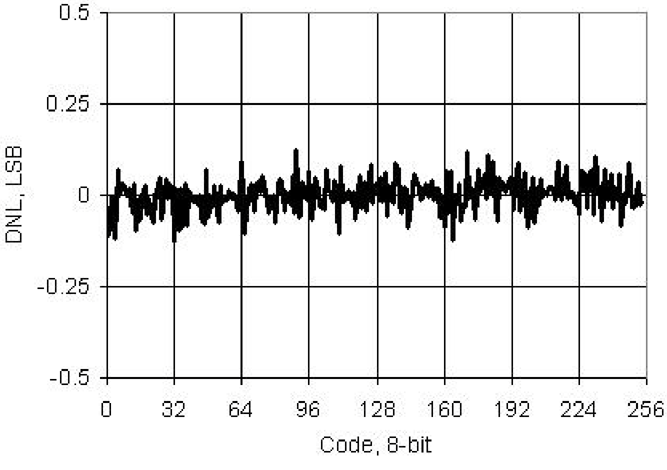


Figure 11-40. IDAC INL vs Temperature, Range = 255 µA, High speed mode

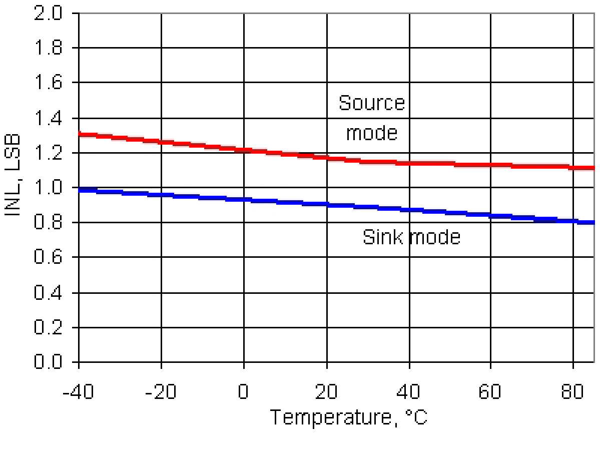
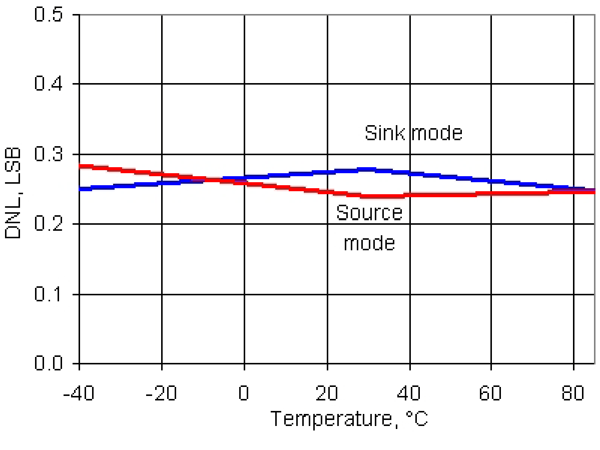


Figure 11-41. IDAC DNL vs Temperature, Range = 255 µA, High speed mode



11.5.7 Voltage Digital to Analog Converter (VDAC)

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-30. VDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	8	–	bits
INL1	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
INL4	Integral nonlinearity[62]	4 V scale	–	±2.1	±2.5	LSB
DNL1	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
DNL4	Differential nonlinearity[62]	4 V scale	–	±0.3	±1	LSB
Rout	Output resistance	1 V scale	–	4	–	kΩ
		4 V scale	–	16	–	kΩ
V_{OUT}	Output voltage range, code = 255	1 V scale	–	1.02	–	V
		4 V scale, V_{DDA} = 5 V	–	4.08	–	V
	Monotonicity		–	–	Yes	–
V_{OS}	Zero scale error		–	0	±0.9	LSB
Eg	Gain error	1 V scale	–	–	±2.5	%
		4 V scale	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale	–	–	0.03	%FSR / °C
		4 V scale	–	–	0.03	%FSR / °C
I_{DD}	Operating current	Low speed mode	–	–	100	µA
		High speed mode	–	–	500	µA

Figure 11-50. VDAC INL vs Input Code, 1 V Mode

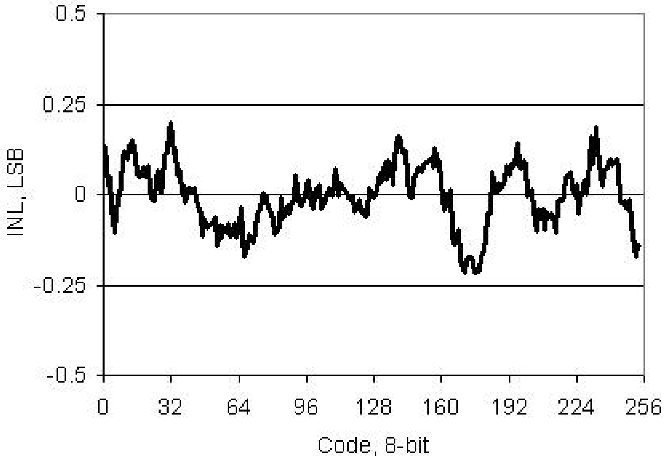
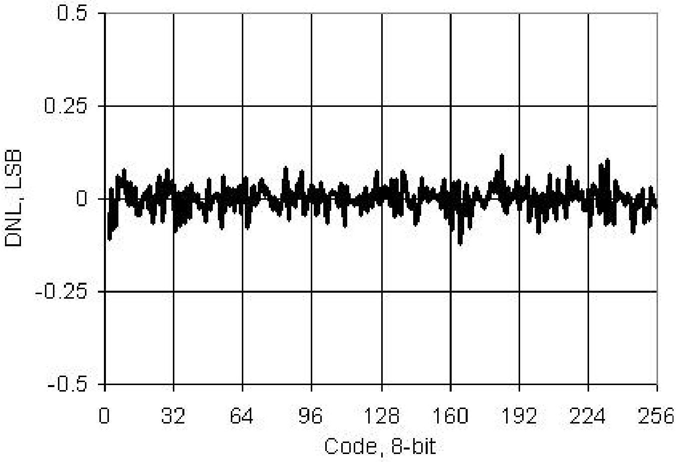


Figure 11-51. VDAC DNL vs Input Code, 1 V Mode



Note

[62] Based on device characterization (Not production tested).

11.5.8 Mixer

The mixer is created using a SC/CT analog block; see the Mixer component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-32. Mixer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage		–	–	15	mV
	Quiescent current		–	0.9	2	mA
G	Gain		–	0	–	dB

Table 11-33. Mixer AC Specifications[63]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LO}	Local oscillator frequency	Down mixer mode	–	–	4	MHz
f_{in}	Input signal frequency	Down mixer mode	–	–	14	MHz
f_{LO}	Local oscillator frequency	Up mixer mode	–	–	1	MHz
f_{in}	Input signal frequency	Up mixer mode	–	–	1	MHz
SR	Slew rate		3	–	–	V/µs

11.5.9 Transimpedance Amplifier

The TIA is created using a SC/CT analog block; see the TIA component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-34. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IOFF}	Input offset voltage		–	–	10	mV
Rconv	Conversion resistance[64]	R = 20K; 40 pF load	–25	–	+35	%
		R = 30K; 40 pF load	–25	–	+35	%
		R = 40K; 40 pF load	–25	–	+35	%
		R = 80K; 40 pF load	–25	–	+35	%
		R = 120K; 40 pF load	–25	–	+35	%
		R = 250K; 40 pF load	–25	–	+35	%
		R= 500K; 40 pF load	–25	–	+35	%
		R = 1M; 40 pF load	–25	–	+35	%
	Quiescent current		–	1.1	2	mA

Table 11-35. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW	Input bandwidth (–3 dB)	R = 20K; –40 pF load	1500	–	–	kHz
		R = 120K; –40 pF load	240	–	–	kHz
		R = 1M; –40 pF load	25	–	–	kHz

Notes

[63] Based on device characterization (Not production tested).

[64] Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component data sheets. External precision resistors can also be used.

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.9.1 *Internal Main Oscillator*

Table 11-73. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	62.6 MHz		–	–	600	µA
	48 MHz		–	–	500	µA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Figure 11-70. IMO Current vs. Frequency

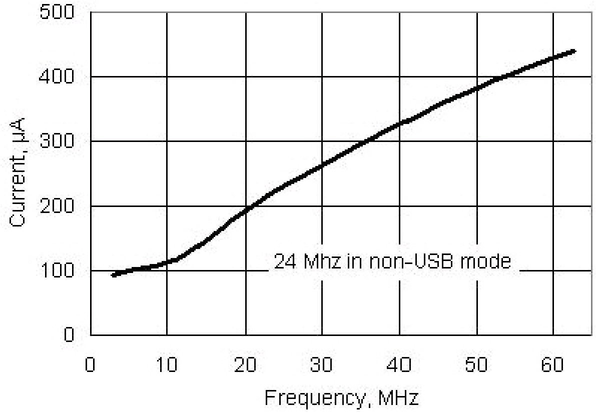


Table 11-74. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}[79]	IMO frequency stability (with factory trim)					
	62.6 MHz		–7	–	7	%
	48 MHz		–5	–	5	%
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz	0 °C to 70 °C	–1	–	1	%
		–40 °C to 85 °C	–1.5	–	1.5	%
	3 MHz frequency stability after typical PCB assembly post-reflow.	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.	–	±2	–	%
	Startup time[80]	From enable (during normal system operation)	–	–	13	µs

---

Notes

[79] F_{IMO} is measured after packaging, and thus accounts for substrate and die attach stresses.

[80] Based on device characterization (Not production tested).

11.9.3 MHz External Crystal Oscillator

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-77. MHzECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[83]	13.56 MHz crystal	–	3.8	–	mA

Table 11-78. MHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency range		4	–	25	MHz

11.9.4 kHz External Crystal Oscillator

Table 11-79. kHzECO DC Specifications[83]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	Low-power mode; CL= 6 pF	–	0.25	1.0	µA
DL	Drive level		–	–	1	µW

Table 11-80. kHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T_{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-81. External Clock Reference AC Specifications[83]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-82. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-83. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[84]		1	–	48	MHz
	PLL intermediate frequency[85]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[84]		24	–	67	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[83]		–	–	250	ps

Notes

[83] Based on device characterization (Not production tested).
[84] This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
[85] PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* **Document Number: 001-53413**				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*D	2903576	04/01/10	MKEA	Updated Vb pin in PCB Schematic Updated Tstartup parameter in AC Specifications table Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table Updated I_{CC} parameter in LCD Direct Drive DC Specs table Updated I_{OUT} parameter in LCD Direct Drive DC Specs table Updated Table 6-2 and Table 6-3 Added bullets on CapSense in page 1; added CapSense column in Section 12 Removed some references to footnote [1] Changed INC_Rn cycles from 3 to 2 (Table 4-1) Added footnote in PLL AC Specification table Added PLL intermediate frequency row with footnote in PLL AC Specs table Added UDBs subsection under 11.6 Digital Peripherals Updated Figure 2-6 (PCB Layout) Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9 Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1 Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Changed V_{REF} from 0.9 to 0.1% Updated boost converter section (6.2.2) Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-68. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated V_{REF} specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table11- 72. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated T_{RESP}, high and low-power modes, in Table 11-24. Updated f_TCK values in Table 11-73 and f_SWDCK values in Table 11-74. Updated SNR condition in Table 11-20. Corrected unit of measurement in Table 11-21. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71 V <= V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-74. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Change PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed I_{DD} values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed sample rate row in Table 11-20. Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22. Changed V_{IOFF} values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-57. Changed max response time value in Tables 11-69 and 11-71. Changed the Startup time in Table 11-79. Added condition to intermediate frequency row in Table 11-85. Added row to Table 11-69. Added brown out note to Section 11.8.1.

Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)*
Document Number: 001-53413

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*M	3464258	12/14/2011	MKEA	Updated Analog Global specs Updated IDAC range Updated TIA section Modified VDDIO description in Section 3 Added note on Sleep and Hibernate modes in the Power Modes section Updated Boost Converter section Updated conditions for Inductive boost AC specs Added VDAC/IDAC noise graphs and specs Added pin capacitance specs for ECO pins Removed C_L from 32 kHz External Crystal DC Specs table. Added reference to AN54439 in Section 6.1.2.2 Deleted T_SWDO_hold row from the SWD Interface AC Specifications table Removed Pin 46 connections in “Example Schematic for 100-pin TQFP Part with Power Connections” Updated Active Mode IDD description in Table 11-2. Added I_{DDDR} and I_{DDAR} specs in Table 11-2. Replaced “total device program time” with T_{PROG} in Flash AC specs table Added I_{GPIO}, I_{SIO} and I_{USBIO} specs in Absolute Maximum Ratings Added conditions to I_{CC} spec in 32 kHz External Crystal DC Specs table. Updated TCV_{OS} value Removed Boost Efficiency vs V_{OUT} graph Updated boost graphs Updated min value of GPIO input edge rate Removed 3.4 Mbps in UDBs from I2C section Updated USBIO Block diagram; added USBIO drive mode description Updated Analog Interconnect diagram Changed max IMO startup time to 12 µs Added note for I_{IL} spec in USBIO DC specs table Updated GPIO Block diagram Updated voltage reference specs Added text explaining power supply ramp up in Section 11-4.

Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)*
Document Number: 001-53413

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*T	4188568	11/14/2013	MKEA	Added SIO Comparator Specifications. Corrected typo in the V_{REF} parameter in the Voltage Reference Specifications. Added CSP information in Packaging and Ordering Information sections. Updated delta-sigma V_{OS} spec conditions.
*U	4385782	05/21/2014	MKEA	Updated General Description and Features. Added More Information and PSoC Creator sections. Updated 100-pin TQFP package diagram.
*V	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in VDAC DC Specifications. Updated Figure 6-11. Added second note after Figure 6-4. Added a reference to Fig 6-1 in *Section 6.1.1* and *Section 6.1.2*. Updated *Section 6.2.2*. Added *Section 7.8.1*. Updated Boost specifications.
*W	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of TWRITE from 2 to 10 in EEPROM AC specs table. Changed “Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Section 11.7.5. Updated Delta-sigma ADC DC Specifications
*X	4932879	09/24/2015	MKEA	Changed the Regulator Output Capacitor min and max from "-" to 0.9 and 1.1, respectively. Added reference to AN54439 in Section 11.9.3. Added MHz ECO DC specs table. Removed references to IPOR rearm issues in Section 6.3.1.1. Table 6-1: Changed DSI Fmax to 33 MHz. Figure 6-1: Changed External I/O or DSI to 0-33 MHz. Table 11-10: Changed Fgpioin Max to 33 MHz. Table 11-12: Changed Fsioin Max to 33 MHz.
*Y	5322536	06/27/2016	MKEA	Updated More Information. Corrected typos in External Electrical Connections. Added links to CAD Libraries in Section 2.