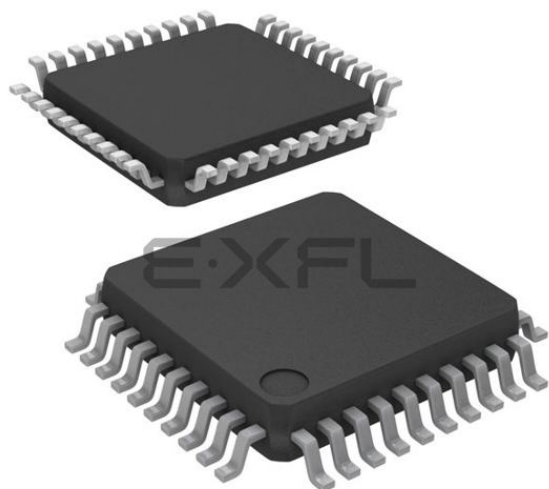




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Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21132dfp-u0

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1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

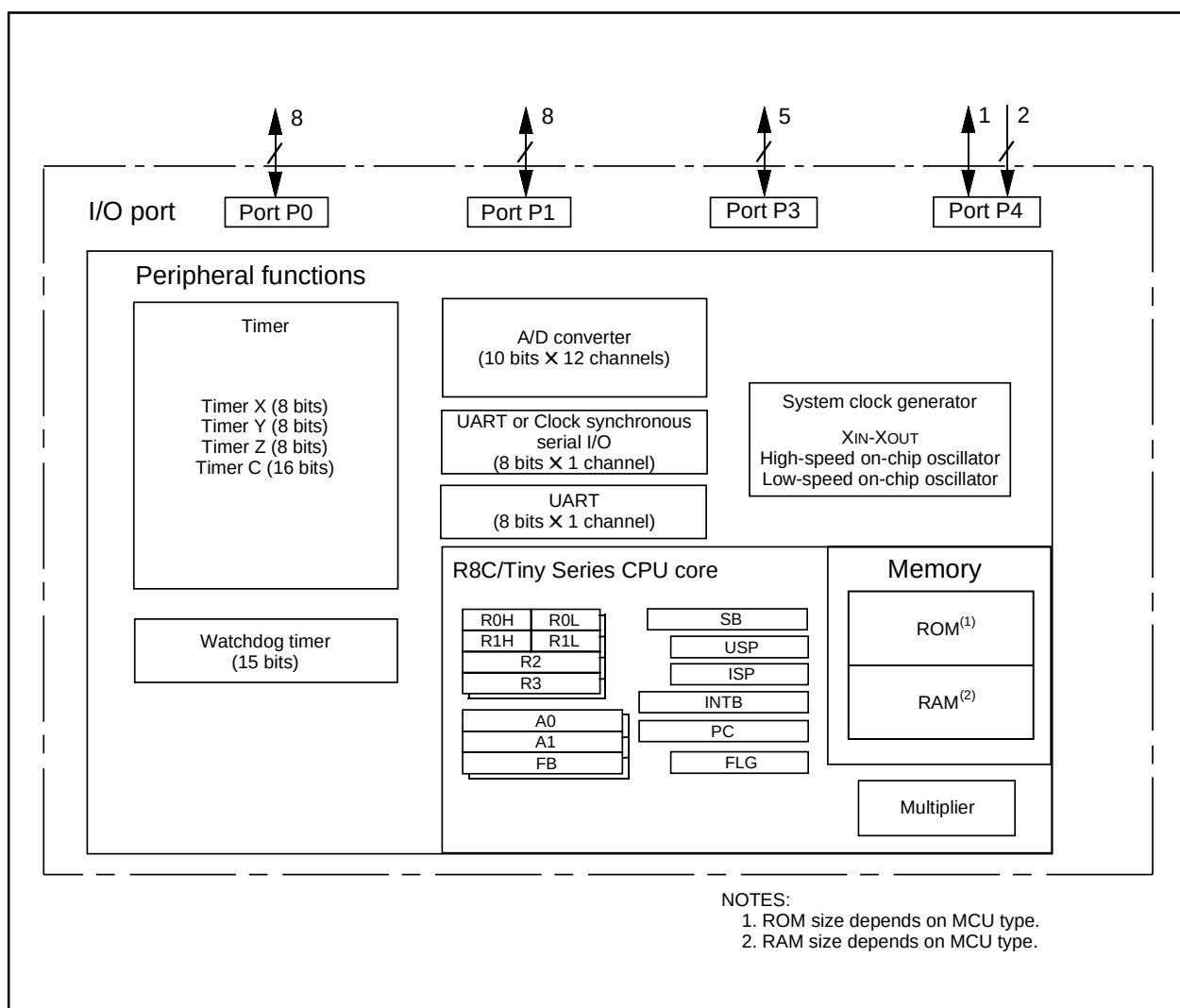


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the product information.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program ROM	Data flash			
R5F21132FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21133FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21132DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21133DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

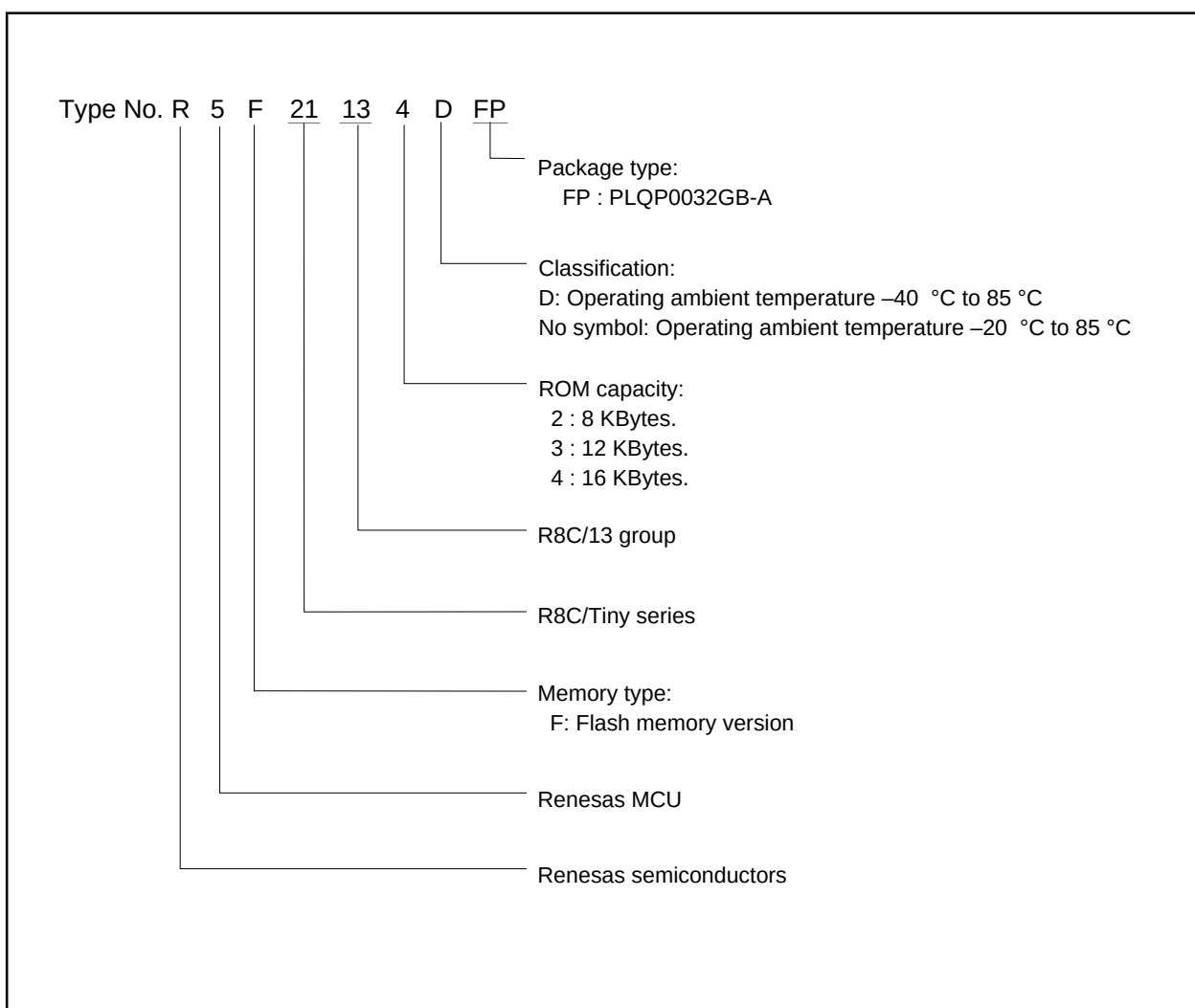


Figure 1.2 Type No., Memory Size, and Package

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μ F). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT0 to INT3	I	INT interrupt input pins.
Key input interrupt input	KI0 to KI3	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	CNTR0	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP00 to CMP02, CMP10 to CMP12	O	The timer C output pins
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN11	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Register. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

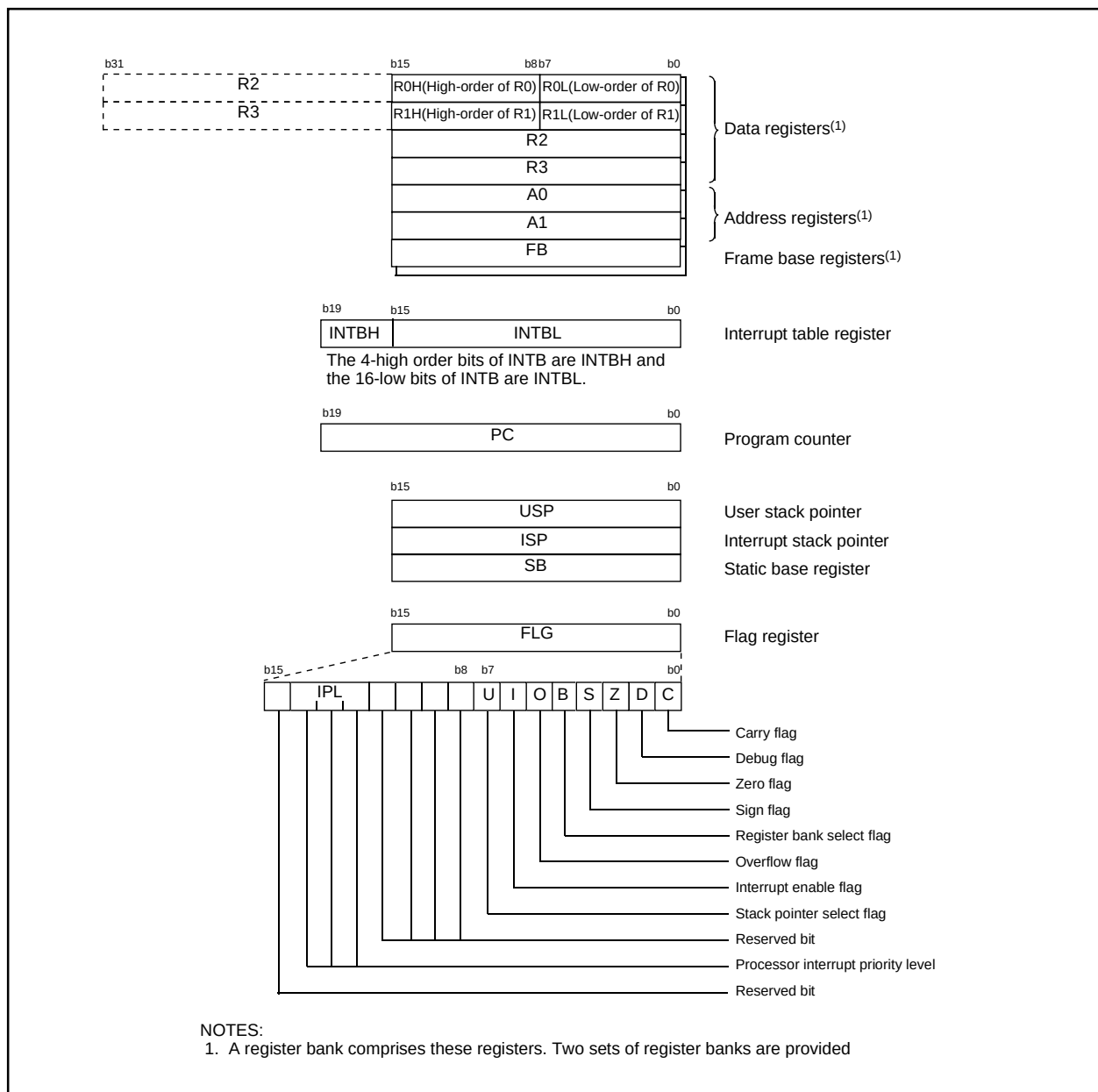


Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A1 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.

The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆.

The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFF₁₆. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000₁₆ to 0FFFF₁₆.

The fixed interrupt vector table is allocated addresses 0FFDC₁₆ to 0FFFF₁₆. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 02000₁₆ to 02FFF₁₆.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated addresses 00400₁₆ to 007FF₁₆. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000₁₆ to 002FF₁₆. The peripheral function control registers are located there. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

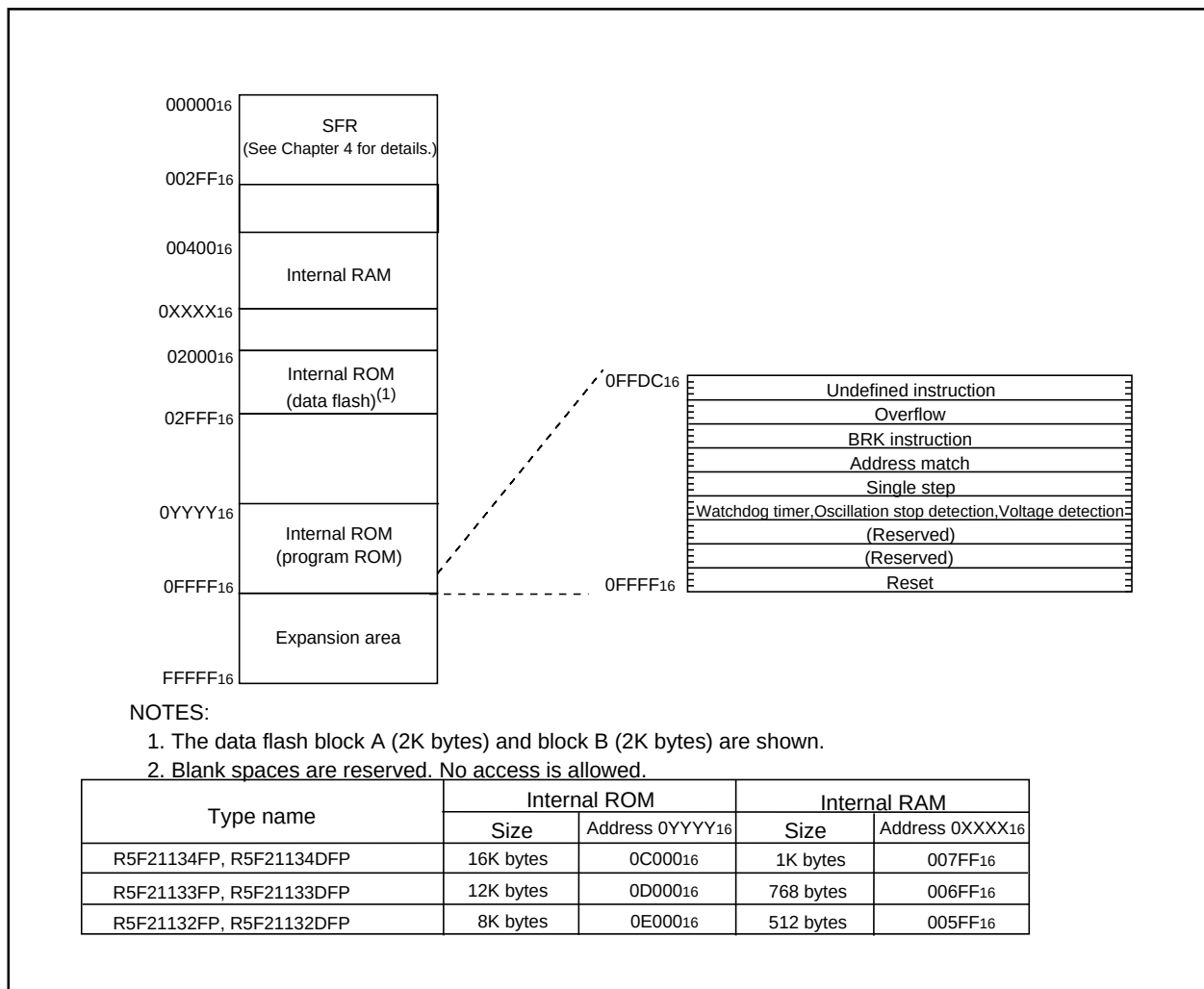


Figure 3.1 Memory Map

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080 ₁₆	Timer Y, Z mode register	TYZMR	0016
0081 ₁₆	Prescaler Y register	PREY	FF16
0082 ₁₆	Timer Y secondary register	TYSC	FF16
0083 ₁₆	Timer Y primary register	TYPR	FF16
0084 ₁₆	Timer Y, Z waveform output control register	PUM	0016
0085 ₁₆	Prescaler Z register	PREZ	FF16
0086 ₁₆	Timer Z secondary register	TZSC	FF16
0087 ₁₆	Timer Z primary register	TZPR	FF16
0088 ₁₆			
0089 ₁₆			
008A ₁₆	Timer Y, Z output control register	TYZOC	0016
008B ₁₆	Timer X mode register	TXMR	0016
008C ₁₆	Prescaler X register	PREX	FF16
008D ₁₆	Timer X register	TX	FF16
008E ₁₆	Count source set register	TCSS	0016
008F ₁₆			
0090 ₁₆	Timer C register	TC	0016
0091 ₁₆			0016
0092 ₁₆			
0093 ₁₆			
0094 ₁₆			
0095 ₁₆			
0096 ₁₆	External input enable register	INTEN	0016
0097 ₁₆			
0098 ₁₆	Key input enable register	KIEN	0016
0099 ₁₆			
009A ₁₆	Timer C control register 0	TCC0	0016
009B ₁₆	Timer C control register 1	TCC1	0016
009C ₁₆	Capture, compare 0 register	TM0	0016
009D ₁₆			0016 ⁽²⁾
009E ₁₆	Compare 1 register	TM1	FF16
009F ₁₆			FF16
00A0 ₁₆	UART0 transmit/receive mode register	U0MR	0016
00A1 ₁₆	UART0 bit rate register	U0BRG	XX16
00A2 ₁₆	UART0 transmit buffer register	U0TB	XX16
00A3 ₁₆			XX16
00A4 ₁₆	UART0 transmit/receive control register 0	U0C0	000010002
00A5 ₁₆	UART0 transmit/receive control register 1	U0C1	000000102
00A6 ₁₆	UART0 receive buffer register	U0RB	XX16
00A7 ₁₆			XX16
00A8 ₁₆	UART1 transmit/receive mode register	U1MR	0016
00A9 ₁₆	UART1 bit rate register	U1BRG	XX16
00AA ₁₆	UART1 transmit buffer register	U1TB	XX16
00AB ₁₆			XX16
00AC ₁₆	UART1 transmit/receive control register 0	U1C0	000010002
00AD ₁₆	UART1 transmit/receive control register 1	U1C1	000000102
00AE ₁₆	UART1 receive buffer register	U1RB	XX16
00AF ₁₆			XX16
00B0 ₁₆	UART transmit/receive control register 2	UCON	0016
00B1 ₁₆			
00B2 ₁₆			
00B3 ₁₆			
00B4 ₁₆			
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X : Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.

2. When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is set to "FFFF16".

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V _{CC}	Supply voltage	V _{CC} =AV _{CC}	-0.3 to 6.5	V
AV _{CC}	Analog supply voltage	V _{CC} =AV _{CC}	-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} +0.3	V
V _O	Output voltage		-0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _{opr} =25 °C	300	mW
T _{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage		2.7	—	5.5	V
AV _{CC}	Analog supply voltage		—	V _{CC} (3)	—	V
V _{SS}	Supply voltage		—	0	—	V
AV _{SS}	Analog supply voltage		—	0	—	V
V _{IH}	"H" input voltage		0.8V _{CC}	—	V _{CC}	V
V _{IL}	"L" input voltage		0	—	0.2V _{CC}	V
I _{OH} (sum)	"H" peak all output currents	Sum of all pins' I _{OH} (peak)	—	—	-60.0	mA
I _{OH} (peak)	"H" peak output current		—	—	-10.0	mA
I _{OH} (avg)	"H" average output current		—	—	-5.0	mA
I _{OL} (sum)	"L" peak all output currents	Sum of all pins' I _{OL} (peak)	—	—	60	mA
I _{OL} (peak)	"L" peak output current	Except P10 to P17	—	—	10	mA
		P10 to P17	—	—	30	mA
		Drive ability LOW	—	—	10	mA
I _{OL} (avg)	"L" average output current	Except P10 to P17	—	—	5	mA
		P10 to P17	—	—	15	mA
		Drive ability LOW	—	—	5	mA
f (X _{IN})	Main clock input oscillation frequency	3.0V ≤ V _{CC} ≤ 5.5V	0	—	20	MHz
		2.7V ≤ V _{CC} < 3.0V	0	—	10	MHz

NOTES:

1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC}=AV_{CC}.

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = V_{CC}$	—	—	10	Bit
—	Absolute accuracy	10 bit mode	$\phi AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8 bit mode	$\phi AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10 bit mode	$\phi AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 5	LSB
		8 bit mode	$\phi AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 2	LSB
R_{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10	—	40	$k\Omega$
t_{CONV}	Conversion time	10 bit mode	$\phi AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8 bit mode	$\phi AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{REF}	Reference voltage			—	$V_{CC}^{(4)}$	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
—	A/D operating clock frequency ⁽²⁾	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:

1. $V_{CC} = AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -20$ to 85°C / -40 to 85°C , unless otherwise specified.
2. If f_{AD} exceeds 10 MHz more, divide the f_{AD} and hold A/D operating clock frequency (ϕAD) 10 MHz or below.
3. If the AV_{CC} is less than 4.2V, divide the f_{AD} and hold A/D operating clock frequency (ϕAD) $f_{AD}/2$ or below.
4. Hold $V_{CC} = V_{ref}$.

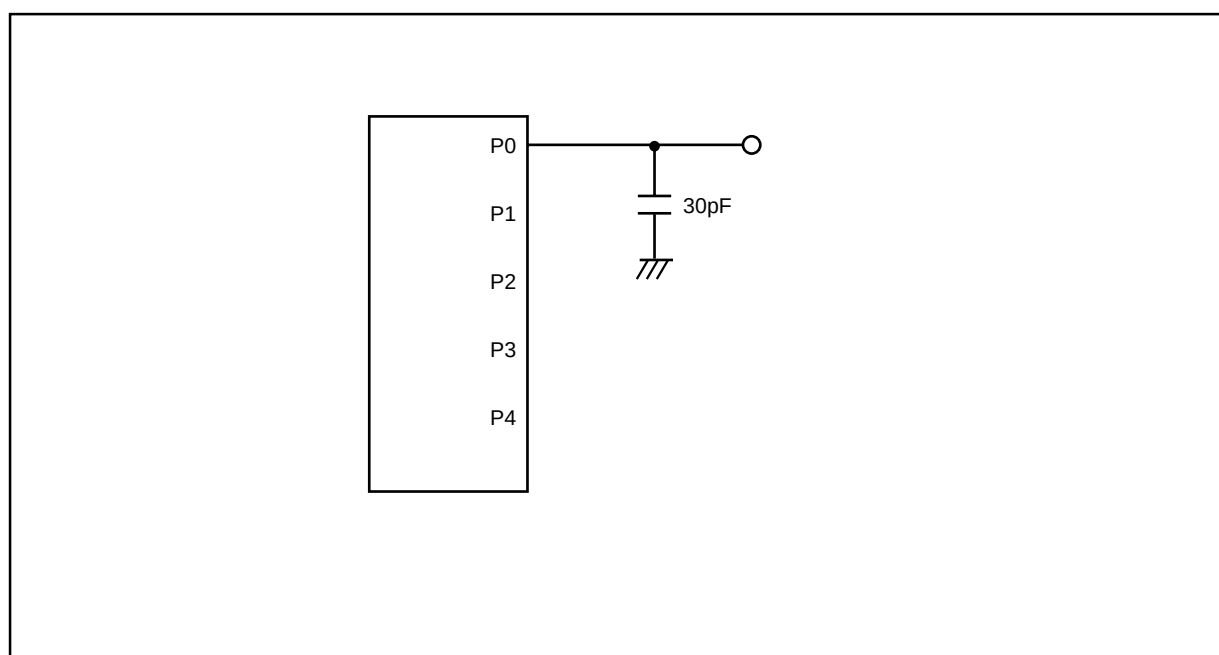
**Figure 5.1 Port P0 to P4 measurement circuit**

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
—	Program/Erase endurance ⁽²⁾		1000 ⁽³⁾	—	—	times
—	Byte program time		—	50	—	μs
—	Block erase time		—	0.4	—	s
t _d (SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
—	Erase Suspend Request Interval		10	—	—	ms
—	Program, Erase Voltage		2.7	—	5.5	V
—	Read Voltage		2.7	—	5.5	V
—	Program, Erase Temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

NOTES:

1. Referenced to V_{CC}=A_VCC=2.7 to 5.5V at T_{opr} = 0°C to 60°C unless otherwise specified.

2. Definition of Program/Erase

The endurance of Program/Erase shows a time for each block.

If the program/erase number is “n” (n = 1000, 10000), “n” times erase can be performed for each block.

For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.

However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).

3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.

4. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.

5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.

6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.6 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time ⁽²⁾			40		μs
	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V		600		nA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾				20	μs
Vccmin	Microcomputer operation voltage minimum value		2.7			V

NOTES:

1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr=-40°C to 85°C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2^(1, 3))

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor2	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled ⁽²⁾	-20°C ≤ Topr < 85°C, tw(por2) ≥ 0s ⁽⁴⁾	—	—	100	ms

NOTES:

1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2 of Hardware Manual for details.
2. This condition is not applicable when using Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage (Vpor1) for greater than 10 seconds, refer to Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor1	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	0.1	V
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s ⁽²⁾	—	—	100	ms
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 30s ⁽²⁾	—	—	100	ms
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 10s ⁽²⁾	—	—	1	ms
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s ⁽²⁾	—	—	0.5	ms

NOTES:

1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).

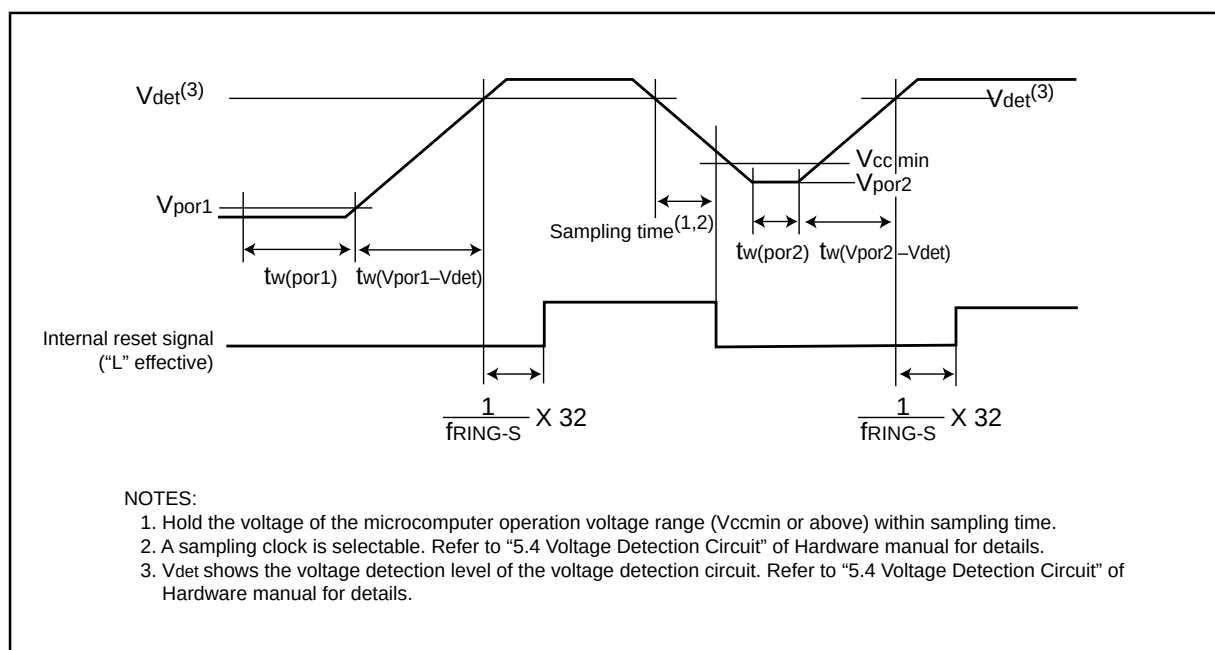
**Figure 5.3 Reset Circuit Electrical Characteristics**

Table 5.12 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} =3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V _{SS}	High-speed mode X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	9	15	mA
		X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	8	14	mA
		X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	4	—	mA
		X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	3	—	mA
		X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	2	—	mA
		High-speed on-chip oscillator mode Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division	—	4	8	mA
		Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.5	—	mA
		Low-speed on-chip oscillator mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	470	900	μA
		Wait mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation VC27="0"	—	40	80	μA
		Wait mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off VC27="0"	—	38	76	μA
		Stop mode Main clock off, T _{opr} = -25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"	—	0.8	3.0	μA

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements [Vcc=5V] (Unless otherwise noted: Vcc = 5V, Vss = 0V at Topr = 25 °C)**Table 5.13 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	50	—	ns
tWH(XIN)	XIN input HIGH pulse width	25	—	ns
tWL(XIN)	XIN input LOW pulse width	25	—	ns

Table 5.14 CNTR0 input, CNTR1 input, INT2 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	100	—	ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40	—	ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40	—	ns

Table 5.15 TCIN input, INT3 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	400 ⁽¹⁾	—	ns
tWH(TCIN)	TCIN input HIGH pulse width	200 ⁽²⁾	—	ns
tWL(TCIN)	TCIN input LOW pulse width	200 ⁽²⁾	—	ns

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.5 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200	—	ns
tw(CKH)	CLKi input HIGH pulse width	100	—	ns
tw(CKL)	CLKi input LOW pulse width	100	—	ns
td(C-Q)	TxDi output delay time	—	80	ns
th(C-Q)	TxDi hold time	0	—	ns
tsu(D-C)	RxDi input setup time	35	—	ns
th(C-D)	RxDi input hold time	90	—	ns

Table 5.17 External interrupt INT0 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	INT0 input HIGH pulse width	250 ⁽¹⁾	—	ns
tw(INL)	INT0 input LOW pulse width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the INT0 input filter select bit, use the INT0 input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the INT0 input filter select bit, use the INT0 input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

Table 5.18 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-1mA		Vcc-0.5	—	Vcc	V
		XOUT	Drive capacity HIGH	IOH=-0.1 mA	Vcc-0.5	—	Vcc	V
			Drive capacity LOW	IOH=-50 μA	Vcc-0.5	—	Vcc	V
VOL	"L" output voltage	Except P10 to P17, XOUT	IOL= 1 mA		—	—	0.5	V
		P10 to P17	Drive capacity HIGH	IOL= 2 mA	—	—	0.5	V
			Drive capacity LOW	IOL= 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	IOL= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	IOL=50 μA	—	—	0.5	V
VT+·VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	0.8	V
		RESET			0.2	—	1.8	V
IIH	"H" input current		VI=3V		—	—	4.0	μA
IIL	"L" input current		VI=0V		—	—	-4.0	μA
RPULLUP	Pull-up resistance		VI=0V		66	160	500	kΩ
RXIN	Feedback resistance	XIN			—	3.0	—	MΩ
fRING-S	Low-speed on-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:

1. Referenced to Vcc = AVcc = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz unless otherwise specified.

Timing requirements [$V_{CC}=3V$] (Unless otherwise noted: $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_{op} = 25\text{ }^{\circ}\text{C}$)**Table 5.20 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(XIN)$	XIN input cycle time	100	—	ns
$t_{WH}(XIN)$	XIN input HIGH pulse width	40	—	ns
$t_{WL}(XIN)$	XIN input LOW pulse width	40	—	ns

Table 5.21 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(CNTR0)$	CNTR0 input cycle time	300	—	ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	120	—	ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	120	—	ns

Table 5.22 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TCIN)$	TCIN input cycle time	1200 ⁽¹⁾	—	ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	600 ⁽²⁾	—	ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	600 ⁽²⁾	—	ns

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time above ($1/\text{Timer C count source frequency} \times 3$).
2. When using the Timer C input capture mode, adjust the pulse width above ($1/\text{Timer C count source frequency} \times 1.5$).

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(CLKi)$	CLKi input cycle time	300	—	ns
$t_{W}(CLKH)$	CLKi input HIGH pulse width	150	—	ns
$t_{W}(CLKL)$	CLKi input LOW pulse width	150	—	ns
$t_d(C-Q)$	TxDi output delay time	—	160	ns
$t_h(C-Q)$	TxDi hold time	0	—	ns
$t_{su}(D-C)$	RxDi input setup time	55	—	ns
$t_h(C-D)$	RxDi input hold time	90	—	ns

Table 5.24 External interrupt $\overline{INT0}$ input

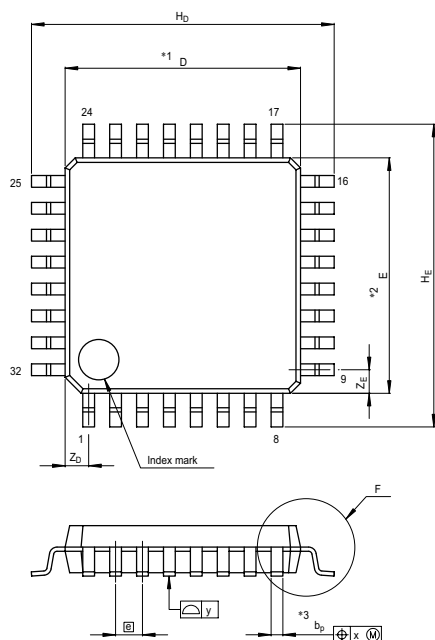
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W}(\overline{INT0}H)$	$\overline{INT0}$ input HIGH pulse width	380 ⁽¹⁾	—	ns
$t_{W}(\overline{INT0}L)$	$\overline{INT0}$ input LOW pulse width	380 ⁽²⁾	—	ns

NOTES:

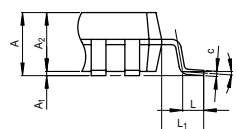
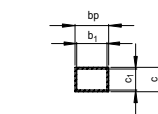
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value, either ($1/\text{digital filter clock frequency} \times 3$) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pulse width to the greater value, either ($1/\text{digital filter clock frequency} \times 3$) or the minimum value of standard.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g



Terminal cross section



Detail F

NOTE)

1. DIMENSIONS "1" AND "2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A ₂	—	1.4	—
H _D	8.8	9.0	9.2
H _E	8.8	9.0	9.2
A	—	—	1.7
A ₁	0	0.1	0.2
b _D	0.32	0.37	0.42
b ₁	—	0.35	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
θ	0°	—	8°
[e]	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z _D	—	0.7	—
Z _E	—	0.7	—
L	0.3	0.5	0.7
L ₁	—	1.0	—

REVISION HISTORY	R8C/13 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Oct 28, 2003		First edition issued
0.20	Dec05, 2003	5	Figure 1.3 revised
		10	Chapter 4, NOTES revised
		16	Table 5.4 revised Table 5.5 revised
		17	Table 5.6 revised Figure 5.3 added
		18	Table 5.8 revised Table 5.10 revised
		21	Figure 5.3 revised to Figure 5.4
		22	Table 5.17 revised
		25	Figure 5.4 revised to Figure 5.5
1.00	Sep 30, 2004	All pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Titles of Table 4.1 to 4.4 added
		12	Table 4.3 revised ; Table 4.4 revised
		14	Table 5.2 revised
		15	Table 5.3 revised
		16	Table 5.4 and Table 5.5 revised
		17	Table 5.6, 5.7 and 5.8 revised ; Figure 5.3 revised
		18	Table 5.9 and 5.11 revised
		19	Table 5.12 revised
		20	Table 5.13 revised
		22	Table 5.18 revised
		23	Table 5.19 revised
		24	Table 5.20 and Table 5.24 revised
1.10	Apr.27.2005	4	Table 1.2, Figure 1.2 package name revised
		5	Figure 1.3 package name revised
		10	Table 4.1 revised
		12	Table 4.3 revised
		15	Table 5.3 partly revised
		16	Table 5.4, Table 5.5 partly added

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Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 205, AZIA Center, No.133 Yincheng Rd (n), Pudong District, Shanghai 200120, China
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510