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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21132fp-w4

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	50 ns (f(X _{IN}) = 20 MHz, V _{CC} = 3.0 to 5.5 V) 100 ns (f(X _{IN}) = 10 MHz, V _{CC} = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Circuits of input capture and output compare)
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high-speed, low-speed) On high-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	Included
	Power on reset circuit	Included
Electrical characteristics	Supply voltage	V _{CC} = 3.0 to 5.5V (f(X _{IN}) = 20MHz) V _{CC} = 2.7 to 5.5V (f(X _{IN}) = 10MHz)
	Power consumption	Typ.9 mA (V _{CC} = 5.0V, (f(X _{IN}) = 20MHz) Typ.5 mA (V _{CC} = 3.0V, (f(X _{IN}) = 10MHz) Typ.35 μA (V _{CC} = 3.0V, Wait mode, Peripheral clock stops) Typ.0.7 μA (V _{CC} = 3.0V, Stop mode)
Flash memory	Program/erase supply voltage	V _{CC} = 2.7 to 5.5 V
	Program/erase endurance	10,000 times (Data flash) 1,000 times (Program ROM)
		Operating ambient temperature
		-20 to 85°C -40 to 85°C (D-version)
Package		32-pin plastic mold LOFP

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

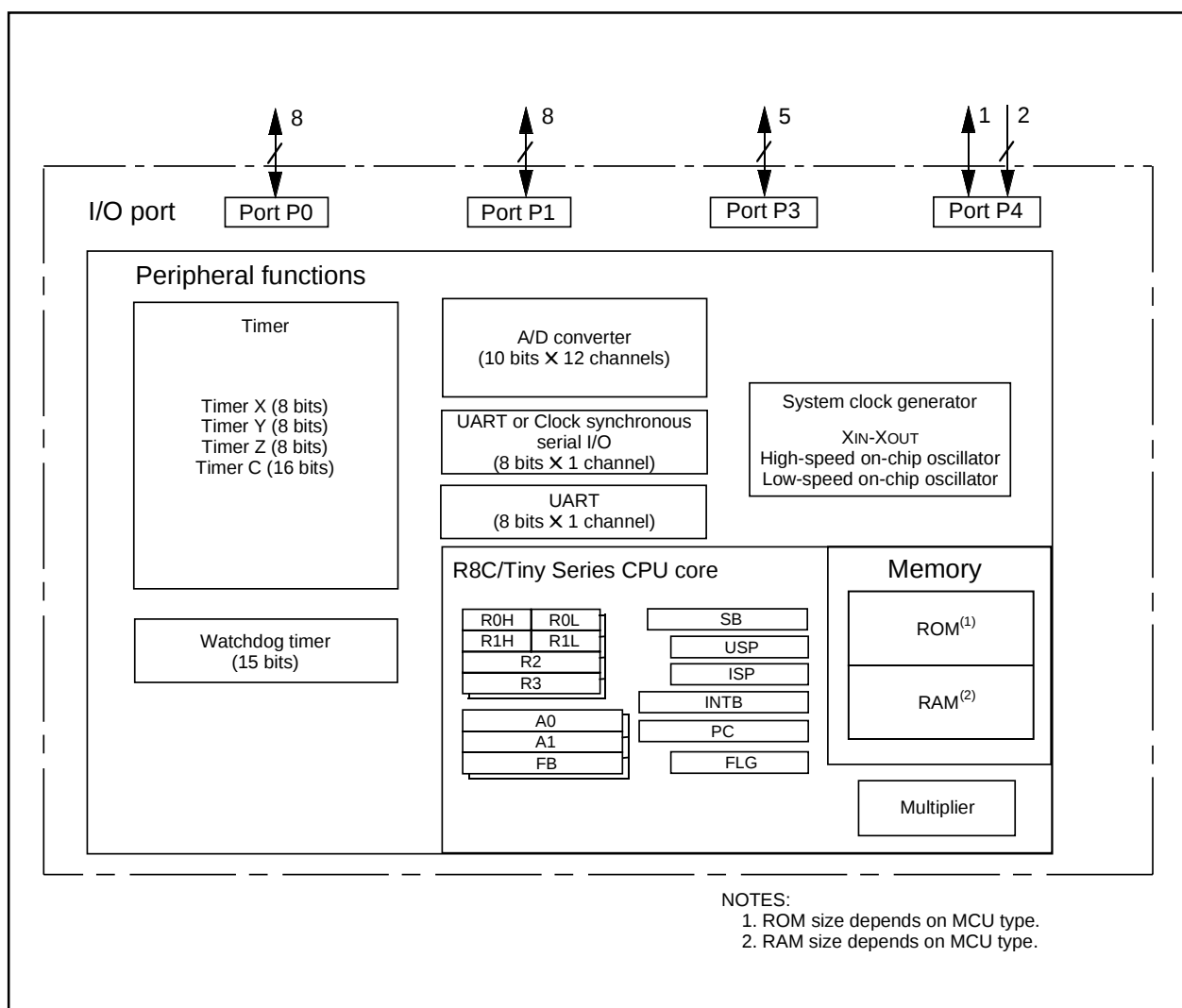


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the product information.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program ROM	Data flash			
R5F21132FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21133FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21132DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21133DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

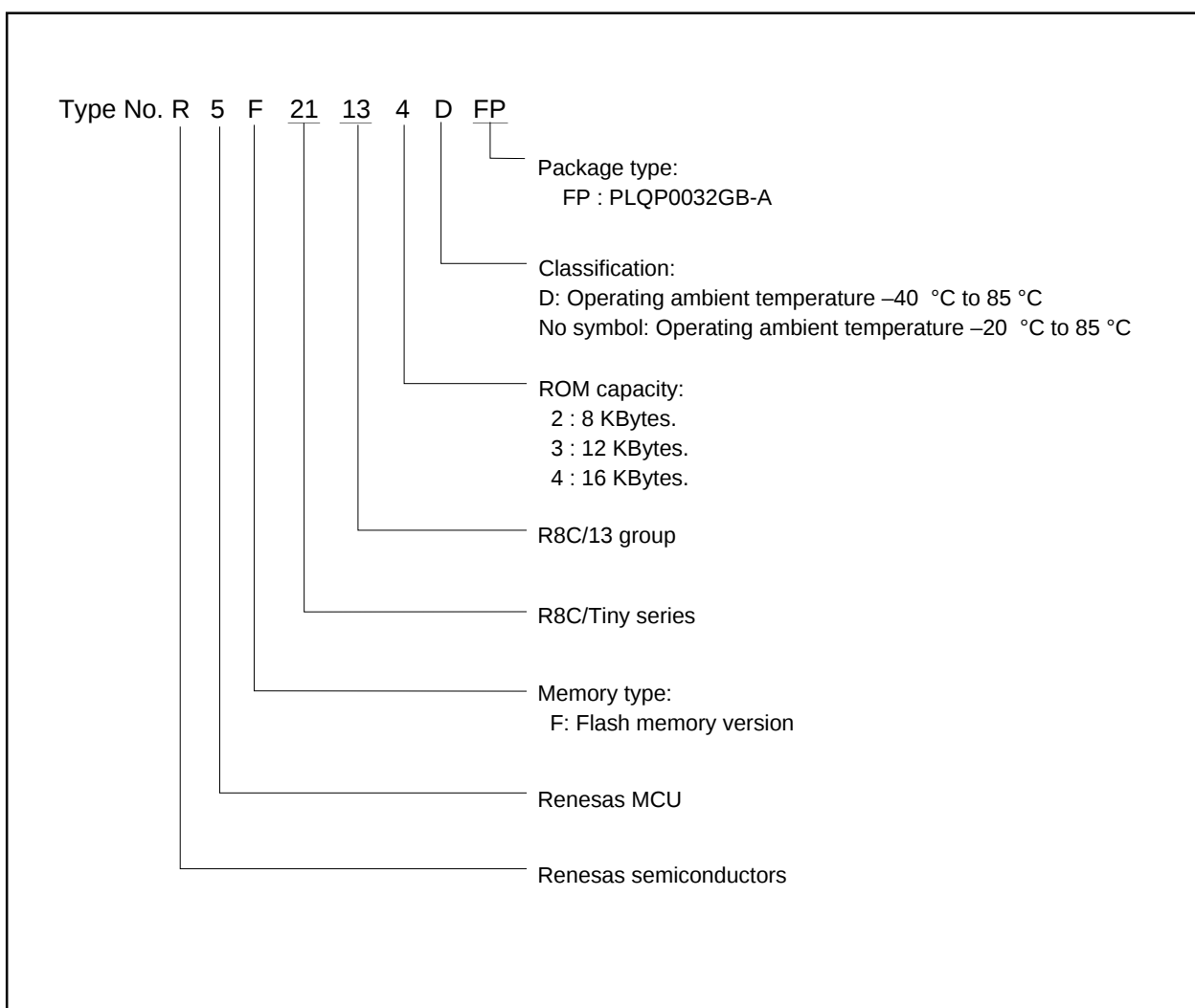


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

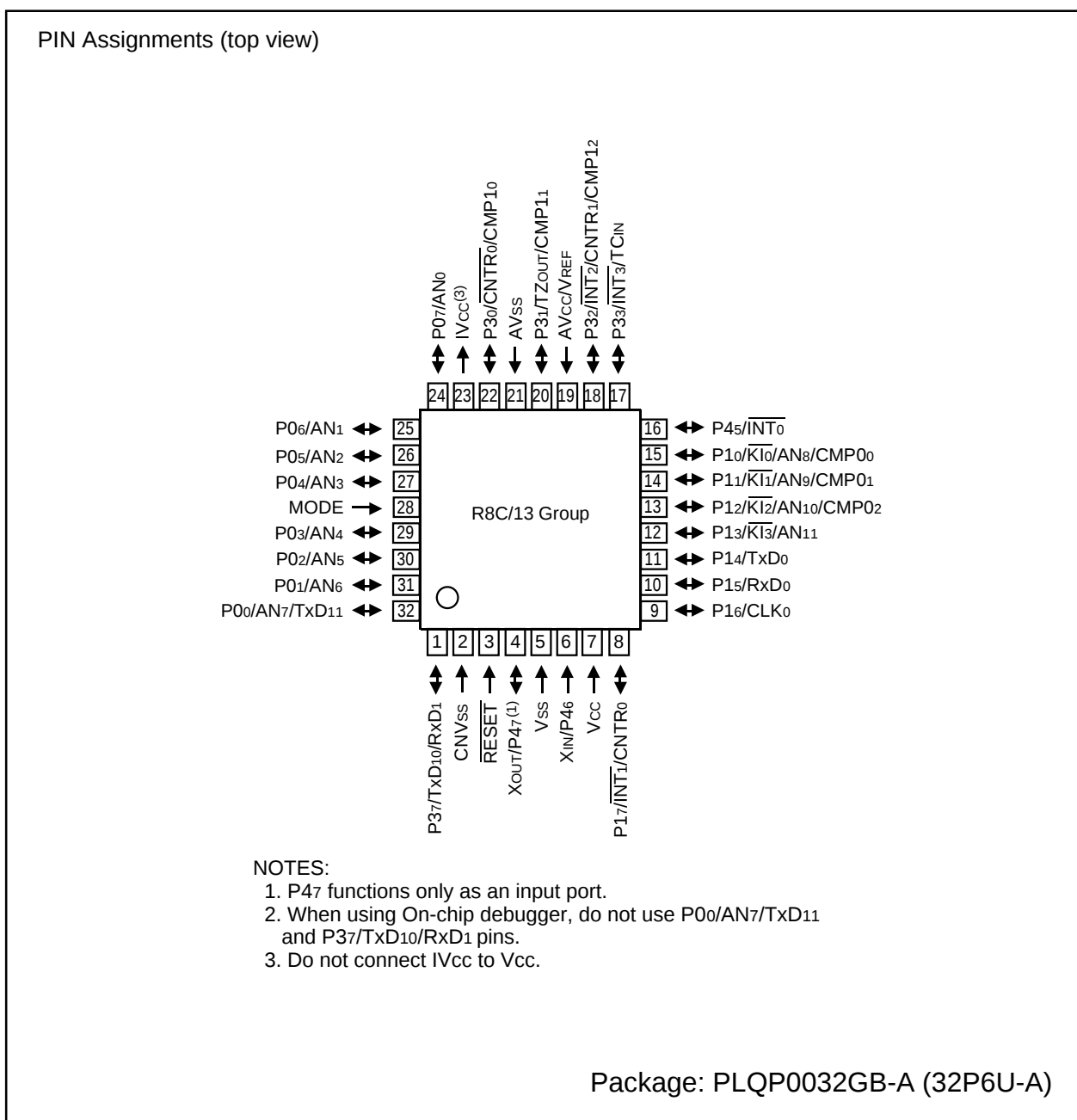


Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μ F). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT0 to INT3	I	INT interrupt input pins.
Key input interrupt input	KI0 to KI3	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	CNTR0	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP00 to CMP02, CMP10 to CMP12	O	The timer C output pins
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN11	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Register. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

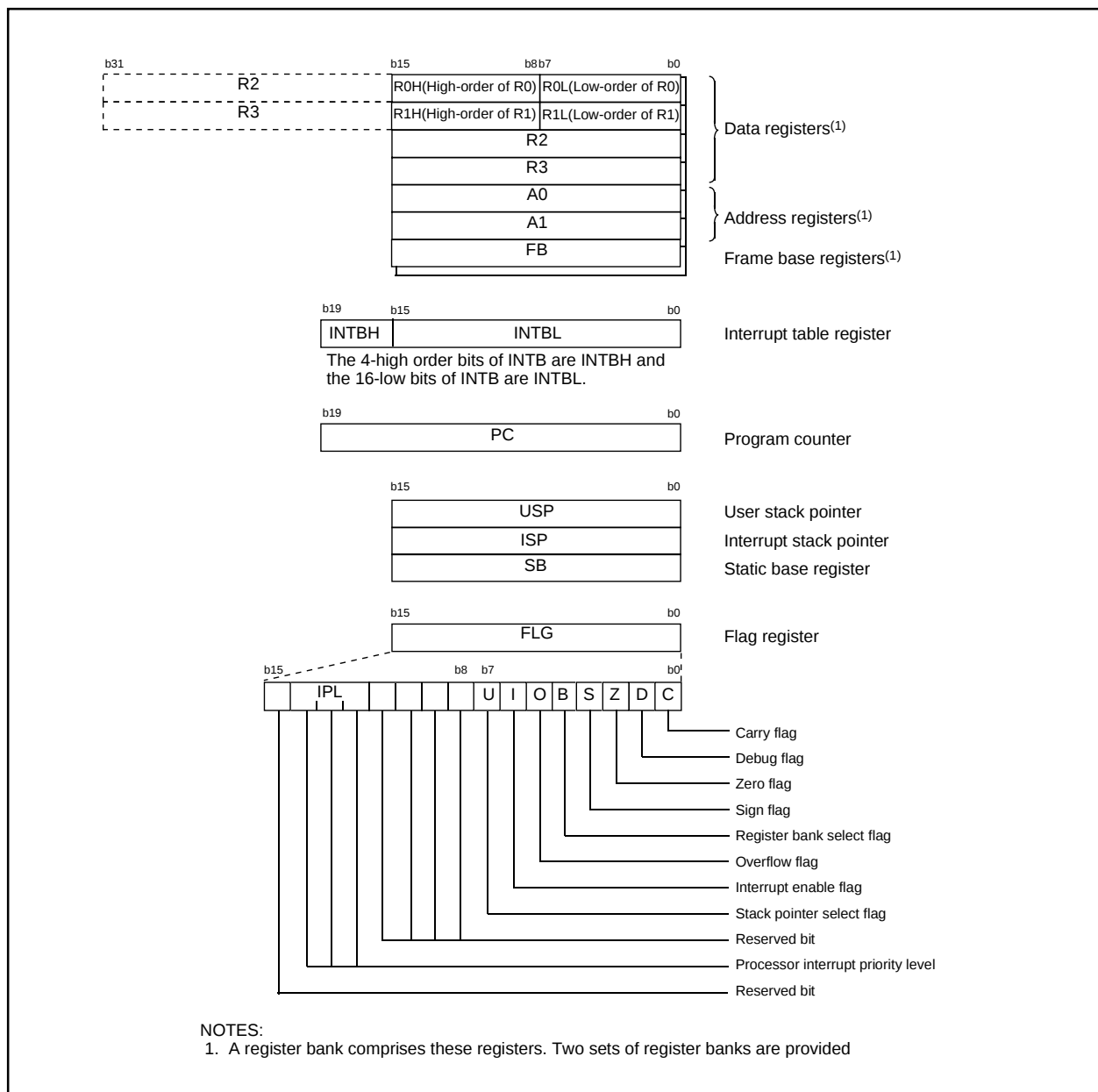


Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A1 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.

The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆.

The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFF₁₆. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000₁₆ to 0FFFF₁₆.

The fixed interrupt vector table is allocated addresses 0FFDC₁₆ to 0FFFF₁₆. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 02000₁₆ to 02FFF₁₆.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated addresses 00400₁₆ to 007FF₁₆. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000₁₆ to 002FF₁₆. The peripheral function control registers are located there. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

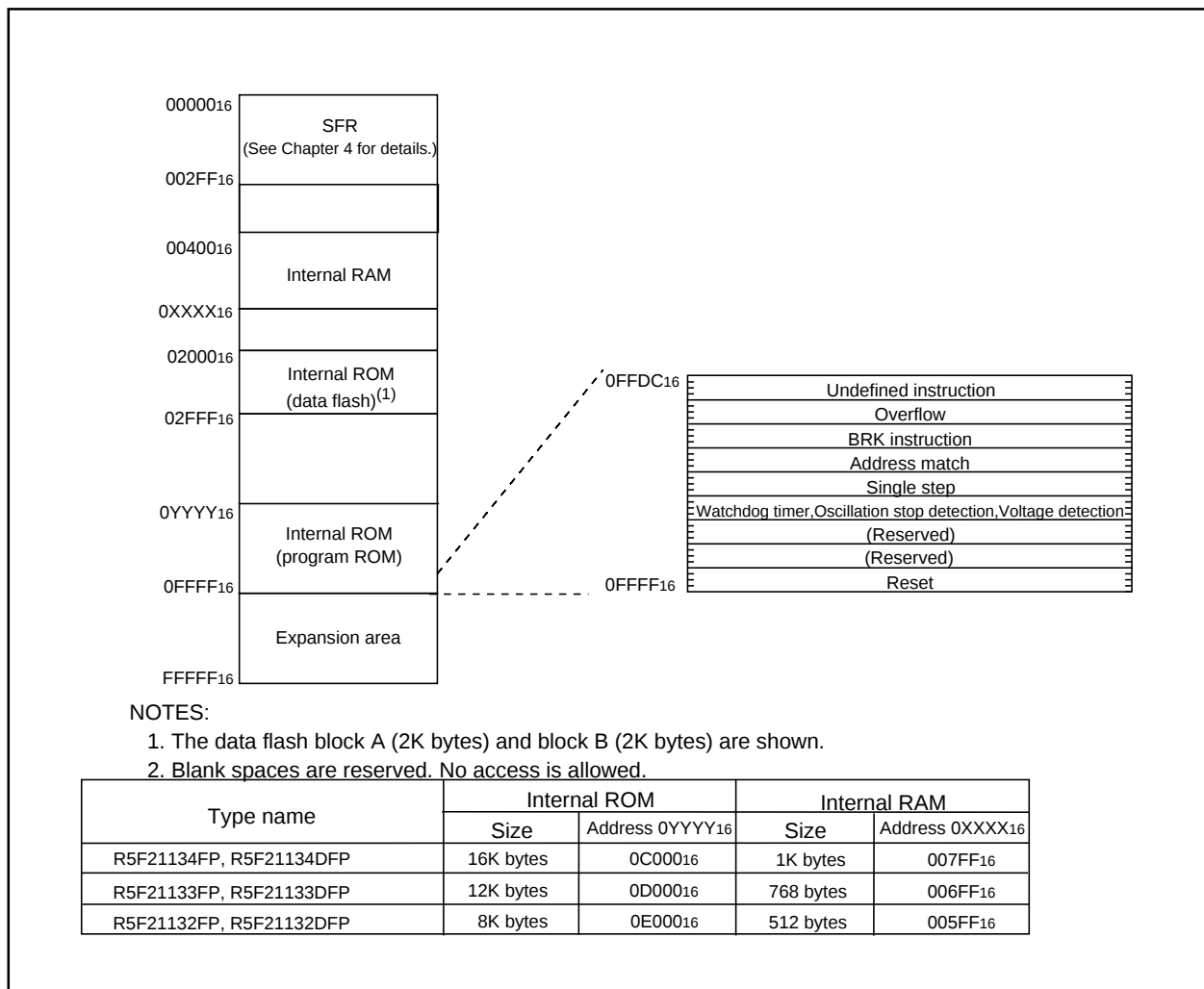


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0 ⁽¹⁾	PM0	0016
0005 ₁₆	Processor mode register 1	PM1	0016
0006 ₁₆	System clock control register 0	CM0	011010002
0007 ₁₆	System clock control register 1	CM1	001000002
0008 ₁₆	High-speed on-chip oscillator control register 0	HR0	0016
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX002
000A ₁₆	Protect register	PRCR	00XXX0002
000B ₁₆	High-speed on-chip oscillator control register 1	HR1	4016
000C ₁₆	Oscillation stop detection register	OCD	000001002
000D ₁₆	Watchdog timer reset register	WDTR	XX16
000E ₁₆	Watchdog timer start register	WDTs	XX16
000F ₁₆	Watchdog timer control register	WDC	000111112
0010 ₁₆	Address match interrupt register 0	RMAD0	0016
0011 ₁₆			0016
0012 ₁₆			X016
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	0016
0015 ₁₆			0016
0016 ₁₆			X016
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Voltage detection register 1 ⁽²⁾	VCR1	000010002
001A ₁₆	Voltage detection register 2 ⁽²⁾	VCR2	0016 ⁽³⁾ 100000002 ⁽⁴⁾
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	INT0 input filter select register	INT0F	XXXXX0002
001F ₁₆	Voltage detection interrupt register ⁽²⁾	D4INT	0016 ⁽³⁾ 010000012 ⁽⁴⁾
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			

X : Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.
- Software reset or the watchdog timer reset does not affect this register.
- Owing to Reset input.
- In the case of RESET pin = H retaining.

Table 4.2 SFR Information(2)⁽¹⁾

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆			
0049 ₁₆			
004A ₁₆			
004B ₁₆			
004C ₁₆			
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E ₁₆	AD conversion interrupt control register	ADIC	XXXXX0002
004F ₁₆			
0050 ₁₆	Compare 1 interrupt control register	CMP1IC	XXXXX0002
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 ₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056 ₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057 ₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058 ₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059 ₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A ₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B ₁₆	Timer C interrupt control register	TCIC	XXXXX0002
005C ₁₆	Compare 0 interrupt control register	CMP0IC	XXXXX0002
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E ₁₆			
005F ₁₆			
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

X : Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = V_{CC}$	—	—	10	Bit
—	Absolute accuracy	10 bit mode	$\phi_{AD}=10\text{ MHz}$, $V_{ref}=V_{CC}=5.0\text{V}$	—	—	± 3	LSB
		8 bit mode	$\phi_{AD}=10\text{ MHz}$, $V_{ref}=V_{CC}=5.0\text{V}$	—	—	± 2	LSB
		10 bit mode	$\phi_{AD}=10\text{ MHz}$, $V_{ref}=V_{CC}=3.3\text{V}^{(3)}$	—	—	± 5	LSB
		8 bit mode	$\phi_{AD}=10\text{ MHz}$, $V_{ref}=V_{CC}=3.3\text{V}^{(3)}$	—	—	± 2	LSB
R_{LADDER}	Ladder resistance		$V_{REF}=V_{CC}$	10	—	40	$k\Omega$
t_{CONV}	Conversion time	10 bit mode	$\phi_{AD}=10\text{ MHz}$, $V_{ref}=V_{CC}=5.0\text{V}$	3.3	—	—	μs
		8 bit mode	$\phi_{AD}=10\text{ MHz}$, $V_{ref}=V_{CC}=5.0\text{V}$	2.8	—	—	μs
V_{REF}	Reference voltage			—	$V_{CC}^{(4)}$	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
—	A/D operating clock frequency ⁽²⁾	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:

1. $V_{CC}=AV_{CC}=2.7$ to 5.5V at $T_{opr} = -20$ to $85\text{ }^{\circ}\text{C}$ / -40 to $85\text{ }^{\circ}\text{C}$, unless otherwise specified.
2. If f_{AD} exceeds 10 MHz more, divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) 10 MHz or below.
3. If the AV_{CC} is less than 4.2V, divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) $f_{AD}/2$ or below.
4. Hold $V_{CC}=V_{ref}$.

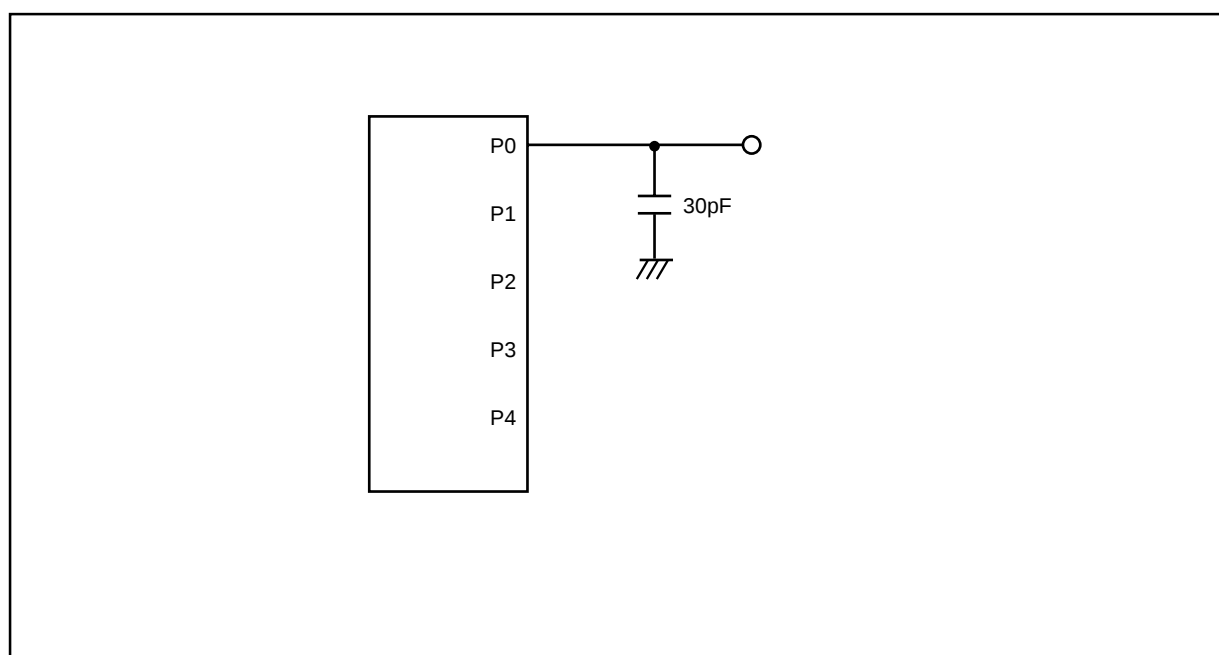
**Figure 5.1 Port P0 to P4 measurement circuit**

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
—	Program/Erase endurance ⁽²⁾		10000 ⁽³⁾	—	—	times
—	Byte program time(program/erase endurance ≤1000 times)		—	50	400	μs
—	Byte program time(program/erase endurance >1000 times)		—	65	—	μs
—	Block erase time(program/erase endurance ≤1000 times)		—	0.2	9	s
—	Block erase time(program/erase endurance >1000 times)		—	0.3	—	s
t _d (SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
—	Erase Suspend Request Interval		10	—	—	ms
—	Program, Erase Voltage		2.7	—	5.5	V
—	Read Voltage		2.7	—	5.5	V
—	Program/Erase Temperature		-20(-40) ⁽⁸⁾	—	85	°C
—	Data hold time ⁽⁹⁾	Ambient temperature = 55 °C	20	—	—	year

NOTES:

1. Referenced to V_{cc}=AV_{cc}=2.7 to 5.5V at Topr = -20°C to 85°C / -40°C to 85°C unless otherwise specified.
2. Definition of Program/Erase
The endurance of Program/Erase shows a time for each block.
If the program/erase number is “n” (n = 1000, 10000), “n” times erase can be performed for each block.
For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4. Table 5.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

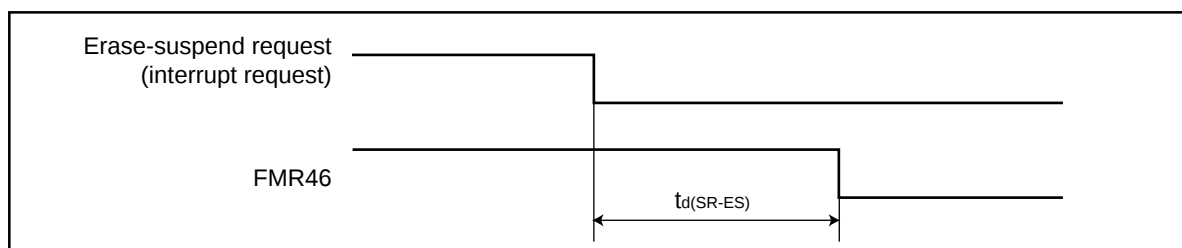
**Figure 5.2 Time delay from Suspend Request until Erase Suspend**

Table 5.6 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time ⁽²⁾			40		μs
	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V		600		nA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾				20	μs
Vccmin	Microcomputer operation voltage minimum value		2.7			V

NOTES:

1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr=-40°C to 85°C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2^(1, 3))

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor2	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled ⁽²⁾	-20°C ≤ Topr < 85°C, tw(por2) ≥ 0s ⁽⁴⁾	—	—	100	ms

NOTES:

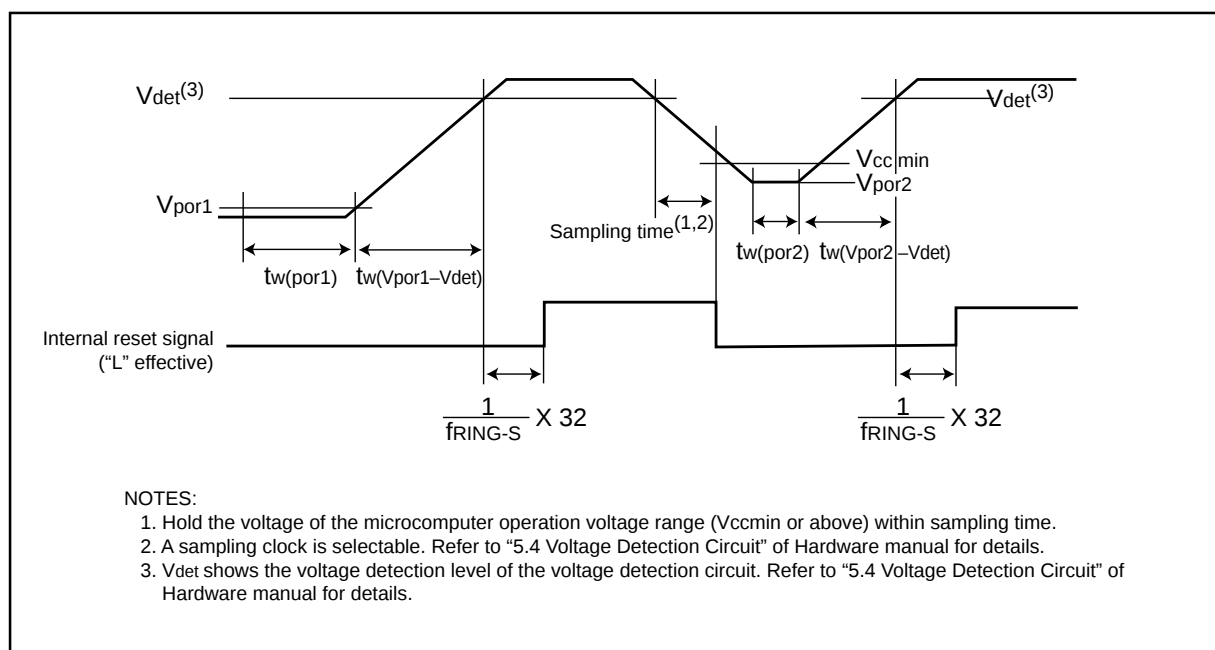
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2 of Hardware Manual for details.
2. This condition is not applicable when using Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage (Vpor1) for greater than 10 seconds, refer to Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor1	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	0.1	V
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s ⁽²⁾	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 30s ⁽²⁾	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 10s ⁽²⁾	—	—	1	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s ⁽²⁾	—	—	0.5	ms

NOTES:

1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).

**Figure 5.3 Reset Circuit Electrical Characteristics**

Timing requirements [V_{CC}=5V] (Unless otherwise noted: V_{CC} = 5V, V_{SS} = 0V at T_{opr} = 25 °C)**Table 5.13 X_{IN} input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _C (X _{IN})	X _{IN} input cycle time	50	—	ns
t _{WH} (X _{IN})	X _{IN} input HIGH pulse width	25	—	ns
t _{WL} (X _{IN})	X _{IN} input LOW pulse width	25	—	ns

Table 5.14 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _C (CNTR0)	CNTR0 input cycle time	100	—	ns
t _{WH} (CNTR0)	CNTR0 input HIGH pulse width	40	—	ns
t _{WL} (CNTR0)	CNTR0 input LOW pulse width	40	—	ns

Table 5.15 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _C (TCIN)	TCIN input cycle time	400 ⁽¹⁾	—	ns
t _{WH} (TCIN)	TCIN input HIGH pulse width	200 ⁽²⁾	—	ns
t _{WL} (TCIN)	TCIN input LOW pulse width	200 ⁽²⁾	—	ns

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.5 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _C (CK)	CLK _i input cycle time	200	—	ns
t _W (CKH)	CLK _i input HIGH pulse width	100	—	ns
t _W (CKL)	CLK _i input LOW pulse width	100	—	ns
t _d (C-Q)	TxD _i output delay time	—	80	ns
t _h (C-Q)	TxD _i hold time	0	—	ns
t _{su} (D-C)	RxD _i input setup time	35	—	ns
t _h (C-D)	RxD _i input hold time	90	—	ns

Table 5.17 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _W (INH)	$\overline{\text{INT0}}$ input HIGH pulse width	250 ⁽¹⁾	—	ns
t _W (INL)	$\overline{\text{INT0}}$ input LOW pulse width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

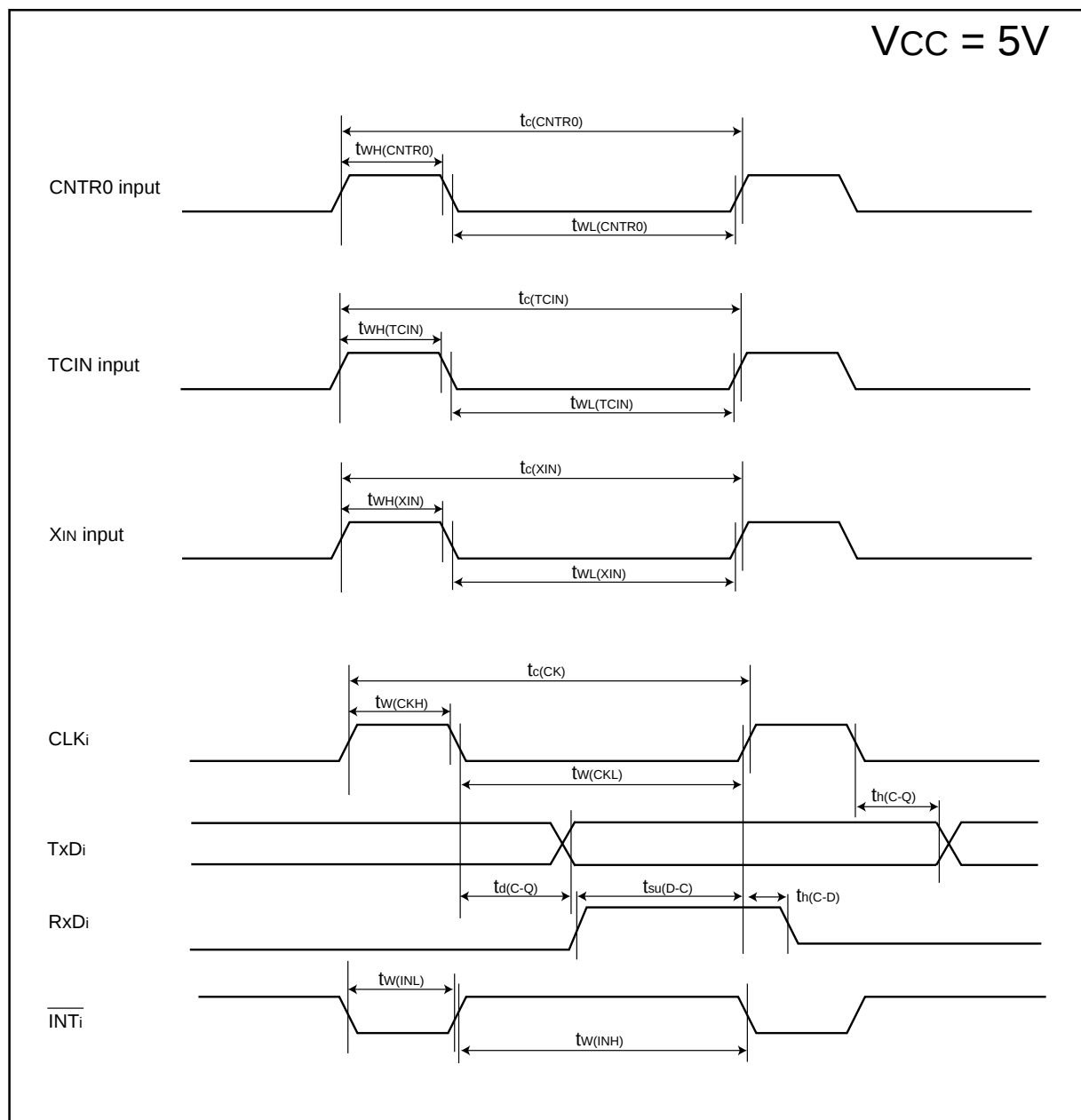
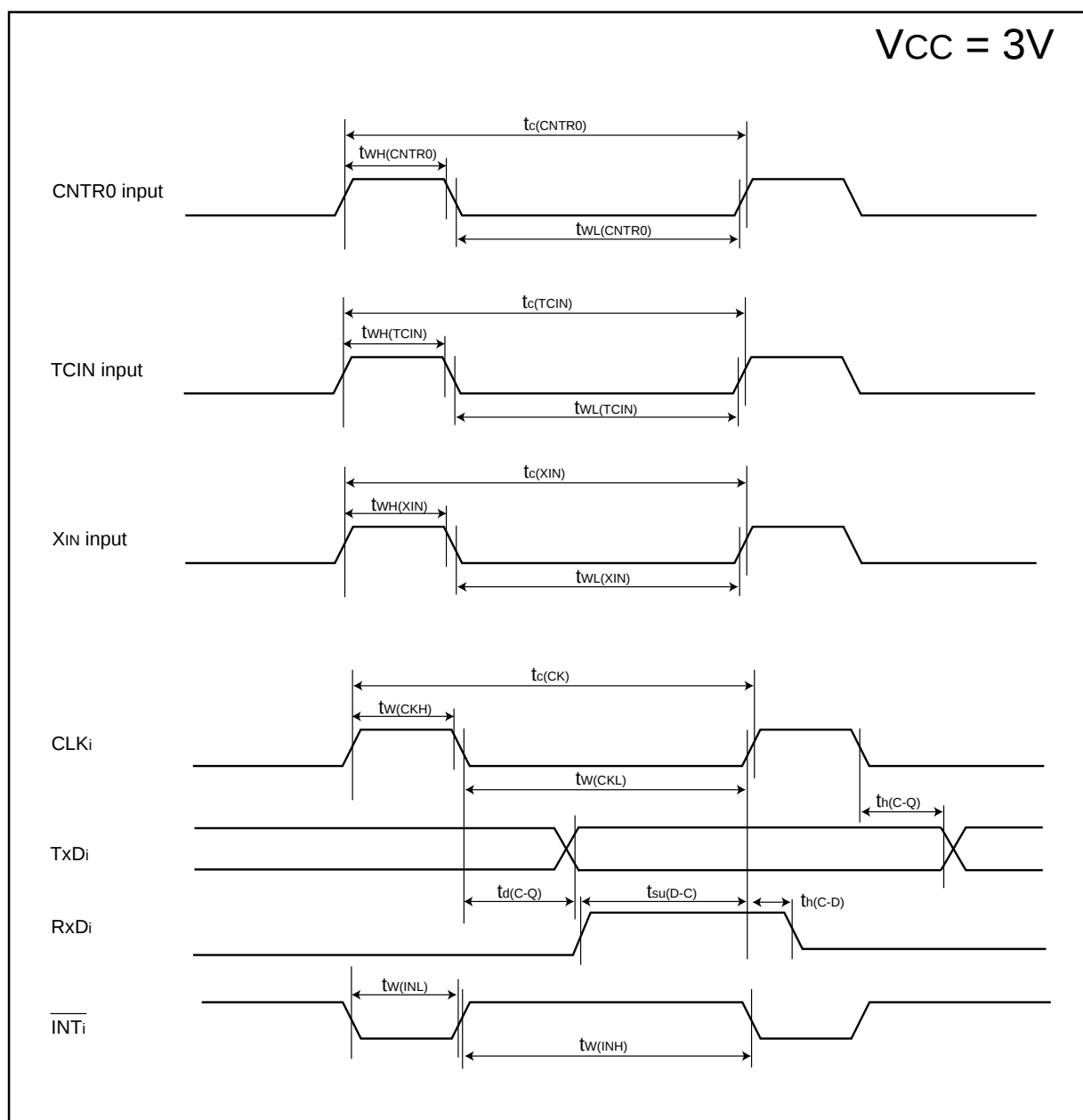
Figure 5.4 $V_{CC}=5V$ timing diagram

Table 5.19 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V _{SS}	High-speed mode X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	8	13	mA
		X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	7	12	mA
		X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	3	—	mA
		X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
		X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
		High-speed on-chip oscillator mode Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division	—	3.5	7.5	mA
		Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.5	—	mA
		Low-speed on-chip oscillator mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	420	800	μA
		Wait mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation VC27="0"	—	37	74	μA
		Wait mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off VC27="0"	—	35	70	μA
		Stop mode Main clock off, Topr=-25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"	—	0.7	3.0	μA

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Figure 5.5 $V_{CC}=3V$ timing diagram

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