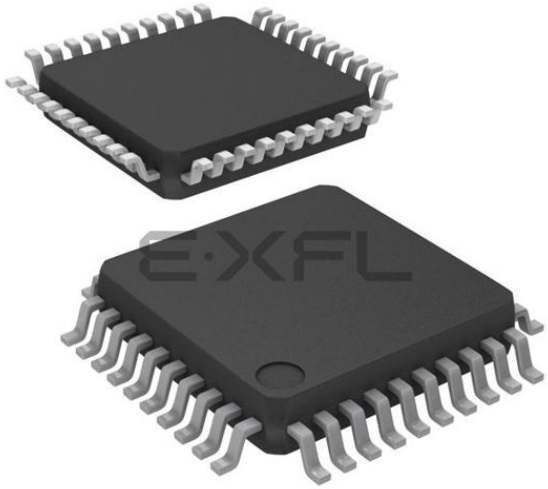

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	22
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21133fp-u0

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1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Circuits of input capture and output compare)
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high-speed, low-speed) On high-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	Included
	Power on reset circuit	Included
Electrical characteristics	Supply voltage	VCC = 3.0 to 5.5V (f(XIN) = 20MHz) VCC = 2.7 to 5.5V (f(XIN) = 10MHz)
	Power consumption	Typ.9 mA (VCC = 5.0V, (f(XIN) = 20MHz) Typ.5 mA (VCC = 3.0V, (f(XIN) = 10MHz) Typ.35 µA (VCC = 3.0V, Wait mode, Peripheral clock stops) Typ.0.7 µA (VCC = 3.0V, Stop mode)
Flash memory	Program/erase supply voltage	VCC = 2.7 to 5.5 V
	Program/erase endurance	10,000 times (Data flash)
		1,000 times (Program ROM)
Operating ambient temperature		-20 to 85°C -40 to 85°C (D-version)
Package		32-pin plastic mold LQFP

1.4 Product Information

Table 1.2 lists the product information.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program ROM	Data flash			
R5F21132FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21133FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21132DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21133DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

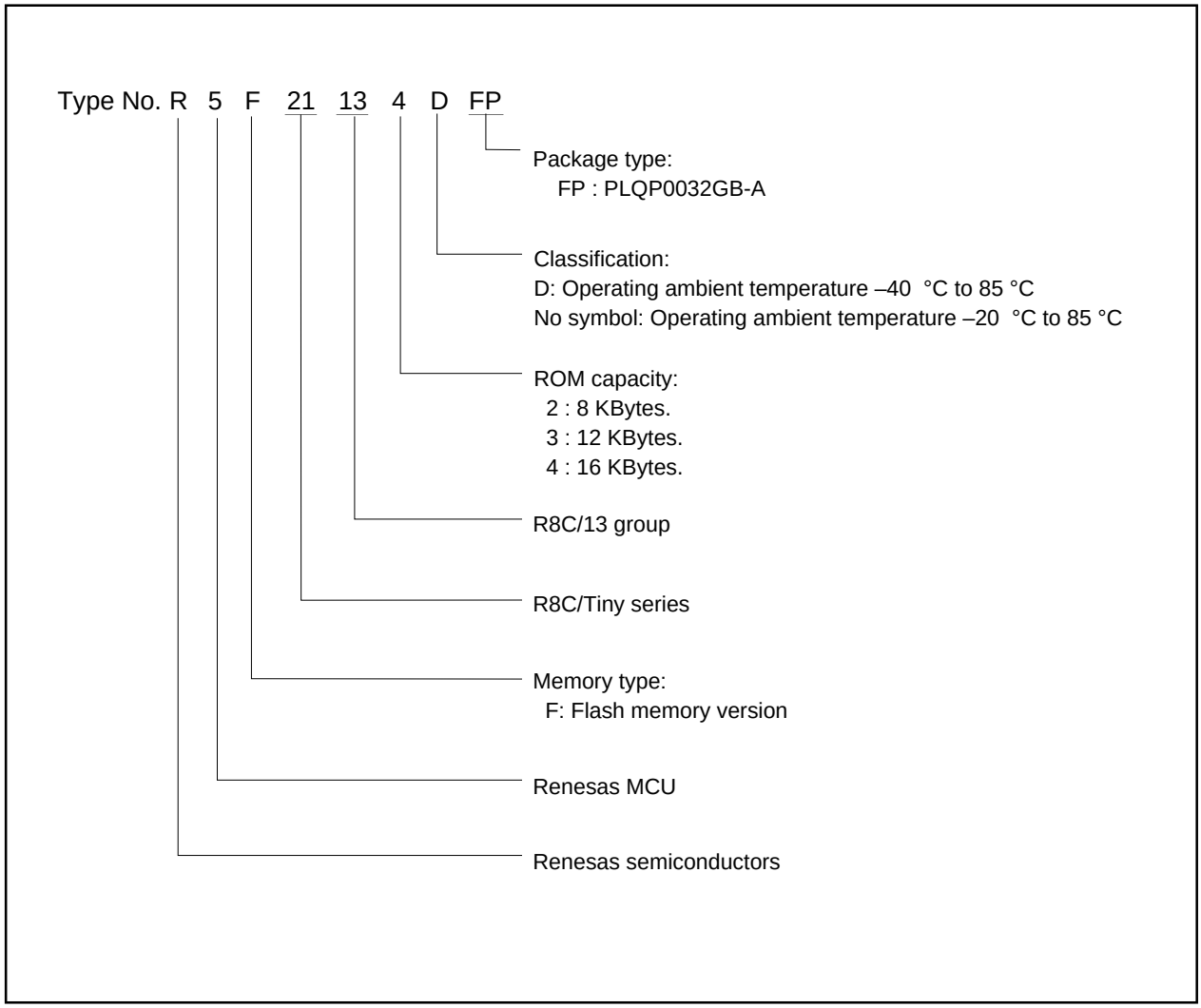
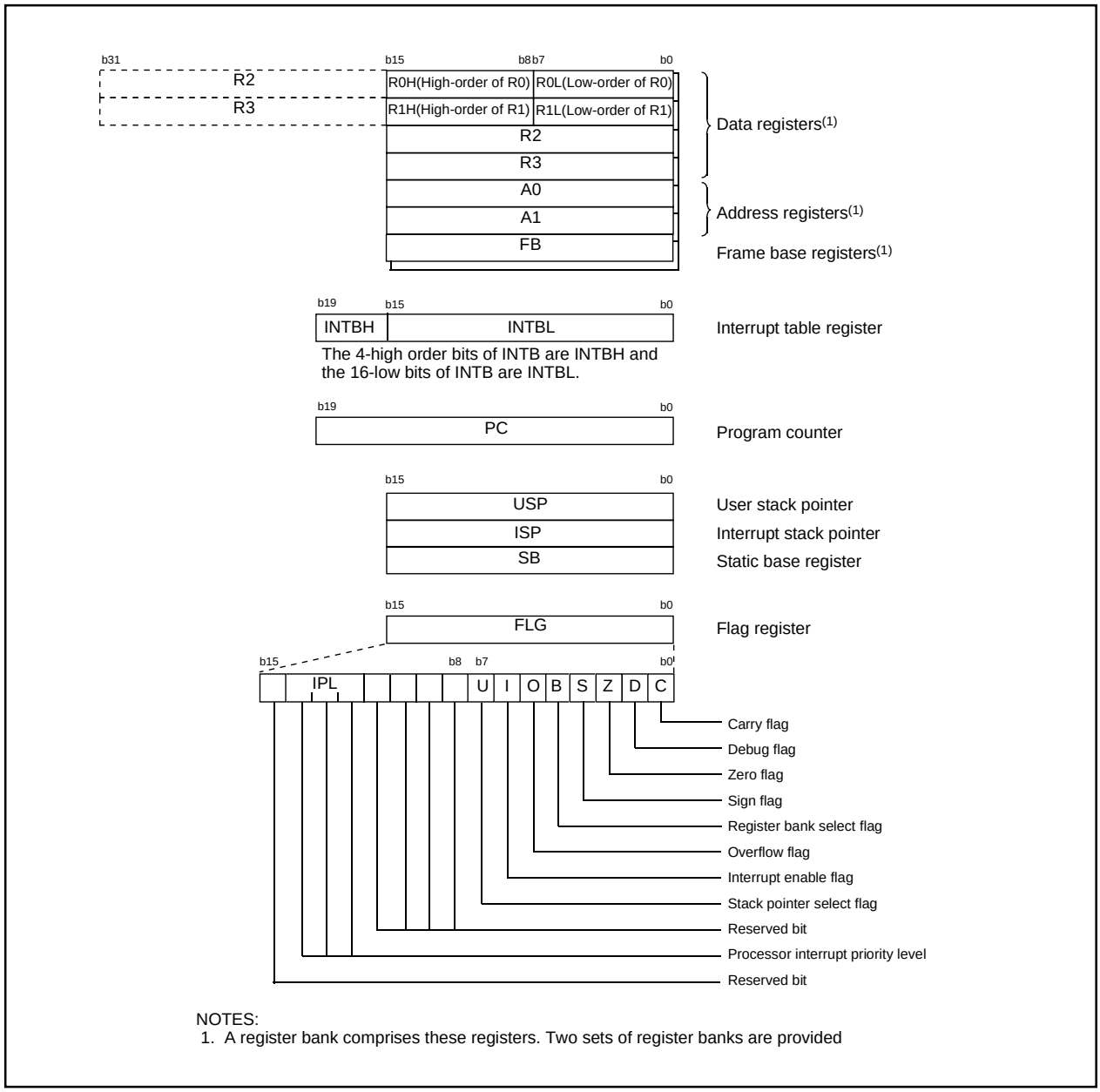


Figure 1.2 Type No., Memory Size, and Package

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Register. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.



NOTES:
1. A register bank comprises these registers. Two sets of register banks are provided

Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$.

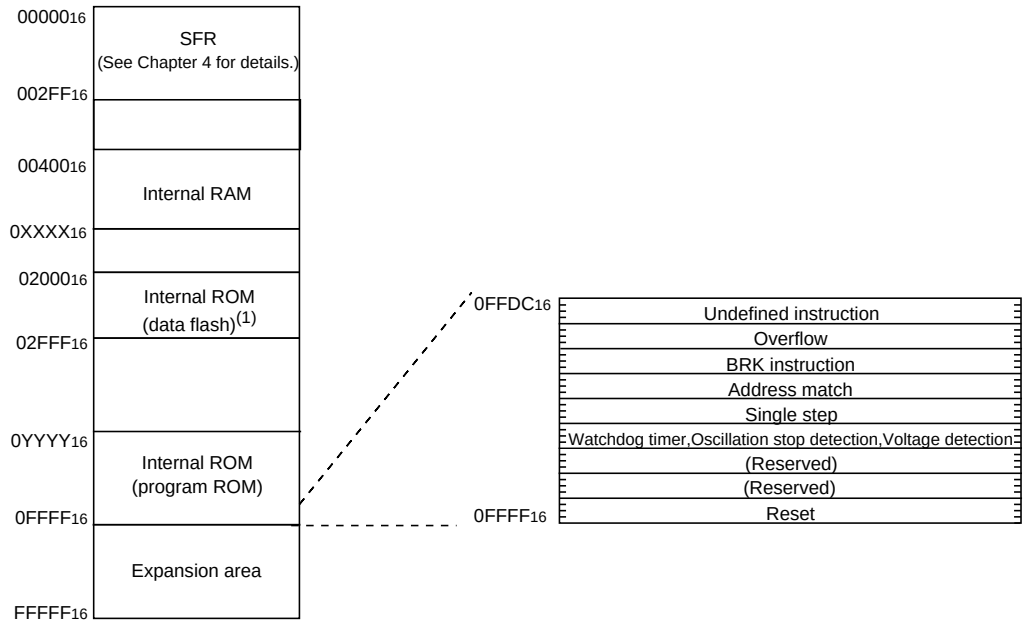
The internal ROM (program ROM) is allocated lower addresses beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated addresses from $0C000_{16}$ to $0FFFF_{16}$.

The fixed interrupt vector table is allocated addresses $0FFDC_{16}$ to $0FFFF_{16}$. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 02000_{16} to $02FFF_{16}$.

The internal RAM is allocated higher addresses beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated addresses 00400_{16} to $007FF_{16}$. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000_{16} to $002FF_{16}$. The peripheral function control registers are located them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



NOTES:
1. The data flash block A (2K bytes) and block B (2K bytes) are shown.
2. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY₁₆	Size	Address 0XXXX₁₆
R5F21134FP, R5F21134DFP	16K bytes	0C000₁₆	1K bytes	007FF₁₆
R5F21133FP, R5F21133DFP	12K bytes	0D000₁₆	768 bytes	006FF₁₆
R5F21132FP, R5F21132DFP	8K bytes	0E000₁₆	512 bytes	005FF₁₆

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0(1)	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00₁₆
0006₁₆	System clock control register 0	CM0	01101000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆	High-speed on-chip oscillator control register 0	HR0	00₁₆
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	00XXX000₂
000B₁₆	High-speed on-chip oscillator control register 1	HR1	40₁₆
000C₁₆	Oscillation stop detection register	OCD	00000100₂
000D₁₆	Watchdog timer reset register	WDTR	XX₁₆
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00011111₂
0010₁₆ 0011₁₆ 0012₁₆	Address match interrupt register 0	RMAD0	00₁₆ 00₁₆ X0₁₆
0013₁₆			
0014₁₆ 0015₁₆ 0016₁₆	Address match interrupt register 1	RMAD1	00₁₆ 00₁₆ X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1(2)	VCR1	00001000₂
001A₁₆	Voltage detection register 2(2)	VCR2	00₁₆(3) 10000000₂(4)
001B₁₆			
001C₁₆			
001D₁₆			
001E₁₆	$\overline{\text{INT0}}$ input filter select register	INT0F	XXXXX000₂
001F₁₆	Voltage detection interrupt register(2)	D4INT	00₁₆(3) 01000001₂(4)
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			

X : Undefined
NOTES:
1. Blank spaces are reserved. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of $\overline{\text{RESET}}$ pin = H retaining.

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080₁₆	Timer Y, Z mode register	TYZMR	00₁₆
0081₁₆	Prescaler Y register	PREY	FF₁₆
0082₁₆	Timer Y secondary register	TYSC	FF₁₆
0083₁₆	Timer Y primary register	TYPR	FF₁₆
0084₁₆	Timer Y, Z waveform output control register	PUM	00₁₆
0085₁₆	Prescaler Z register	PREZ	FF₁₆
0086₁₆	Timer Z secondary register	TZSC	FF₁₆
0087₁₆	Timer Z primary register	TZPR	FF₁₆
0088₁₆			
0089₁₆			
008A₁₆	Timer Y, Z output control register	TYZOC	00₁₆
008B₁₆	Timer X mode register	TXMR	00₁₆
008C₁₆	Prescaler X register	PREX	FF₁₆
008D₁₆	Timer X register	TX	FF₁₆
008E₁₆	Count source set register	TCSS	00₁₆
008F₁₆			
0090₁₆ 0091₁₆	Timer C register	TC	00₁₆ 00₁₆
0092₁₆			
0093₁₆			
0094₁₆			
0095₁₆			
0096₁₆	External input enable register	INTEN	00₁₆
0097₁₆			
0098₁₆	Key input enable register	KIEN	00₁₆
0099₁₆			
009A₁₆	Timer C control register 0	TCC0	00₁₆
009B₁₆	Timer C control register 1	TCC1	00₁₆
009C₁₆ 009D₁₆	Capture, compare 0 register	TM0	00₁₆ 00₁₆(2)
009E₁₆ 009F₁₆	Compare 1 register	TM1	FF₁₆ FF₁₆
00A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
00A1₁₆	UART0 bit rate register	U0BRG	XX₁₆
00A2₁₆ 00A3₁₆	UART0 transmit buffer register	U0TB	XX₁₆ XX₁₆
00A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
00A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
00A6₁₆ 00A7₁₆	UART0 receive buffer register	U0RB	XX₁₆ XX₁₆
00A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
00A9₁₆	UART1 bit rate register	U1BRG	XX₁₆
00AA₁₆ 00AB₁₆	UART1 transmit buffer register	U1TB	XX₁₆ XX₁₆
00AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
00AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
00AE₁₆ 00AF₁₆	UART1 receive buffer register	U1RB	XX₁₆ XX₁₆
00B0₁₆	UART transmit/receive control register 2	UCON	00₁₆
00B1₁₆			
00B2₁₆			
00B3₁₆			
00B4₁₆			
00B5₁₆			
00B6₁₆			
00B7₁₆			
00B8₁₆			
00B9₁₆			
00BA₁₆			
00BB₁₆			
00BC₁₆			
00BD₁₆			
00BE₁₆			
00BF₁₆			

X : Undefined
NOTES:
1. Blank spaces are reserved. No access is allowed.
2. When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is set to "FFFF₁₆".

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	—	5.5	V
AVcc	Analog supply voltage			—	V_{CC}(3)	—	V
Vss	Supply voltage			—	0	—	V
AVss	Analog supply voltage			—	0	—	V
V_{IH}	"H" input voltage			0.8V_{CC}	—	V_{CC}	V
V_{IL}	"L" input voltage			0	—	0.2V_{CC}	V
$I_{OH\ (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)		—	—	-60.0	mA
$I_{OH\ (peak)}$	"H" peak output current			—	—	-10.0	mA
$I_{OH\ (avg)}$	"H" average output current			—	—	-5.0	mA
$I_{OL\ (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)		—	—	60	mA
$I_{OL\ (peak)}$	"L" peak output current	Except $P1_0$ to $P1_7$		—	—	10	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	30	mA
			Drive ability LOW	—	—	10	mA
$I_{OL\ (avg)}$	"L" average output current	Except $P1_0$ to $P1_7$		—	—	5	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	15	mA
			Drive ability LOW	—	—	5	mA
f (X_{IN})	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0	—	20	MHz
			2.7V ≤ Vcc < 3.0V	0	—	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold Vcc=AVcc.

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} =V_{CC}	—	—	10	Bit
–	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)	—	—	±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)	—	—	±2	LSB
R_{LADDER}	Ladder resistance		V_{REF}=V_{CC}	10	—	40	kΩ
t_{CONV}	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3	—	—	µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8	—	—	µs
V_{REF}	Reference voltage			—	V_{CC}(4)	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
–	A/D operating clock frequency(2)	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:
1. V_{CC}=AV_{CC}=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f_{AD} exceeds 10 MHz more, divide the f_{AD} and hold A/D operating clock frequency (Ø$_{AD}$) 10 MHz or below.
3. If the AVcc is less than 4.2V, divide the f_{AD} and hold A/D operating clock frequency (Ø$_{AD}$) f_{AD}/2 or below.
4. Hold Vcc=Vref.

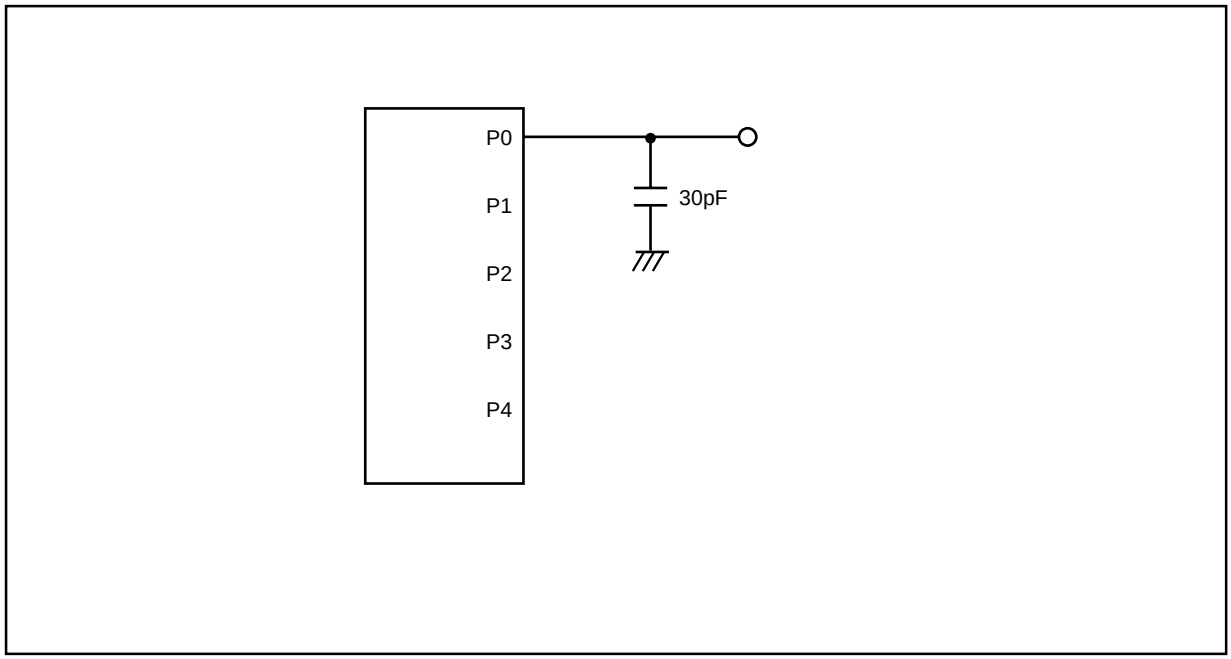


Figure 5.1 Port P0 to P4 measurement circuit

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance(2)		10000(3)	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)		—	50	400	µs
–	Byte program time(program/erase endurance >1000 times)		—	65	—	µs
–	Block erase time(program/erase endurance ≤1000 times)		—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)		—	0.3	—	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40)(8)	—	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	—	—	year

NOTES:
1. Referenced to VCC=AVcc=2.7 to 5.5V at Topr = -20°C to 85°C / -40°C to 85°C unless otherwise specified.
2. Definition of Program/Erase
   The endurance of Program/Erase shows a time for each block.
   If the program/erase number is “n” (n = 1000, 10000), “n” times erase can be performed for each block.
   For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
   However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4. Table 5.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

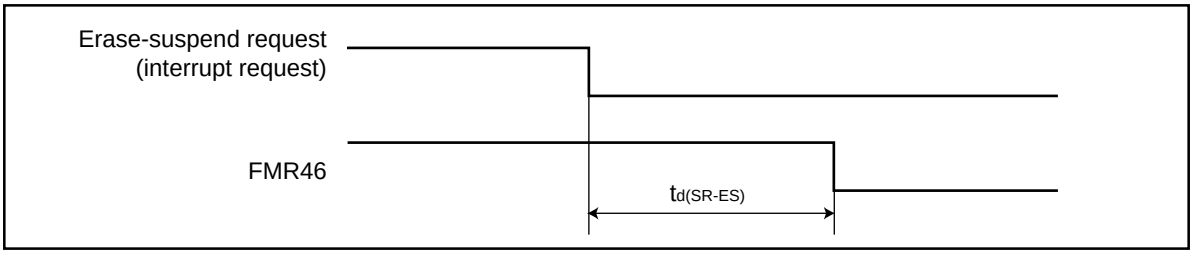


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time(2)			40		µs
	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V		600		nA
td(E-A)	Waiting time until voltage detection circuit operation starts(3)				20	µs
Vccmin	Microcomputer operation voltage minimum value		2.7			V

NOTES:
1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr=-40°C to 85°C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to “0”.

Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2(1, 3))

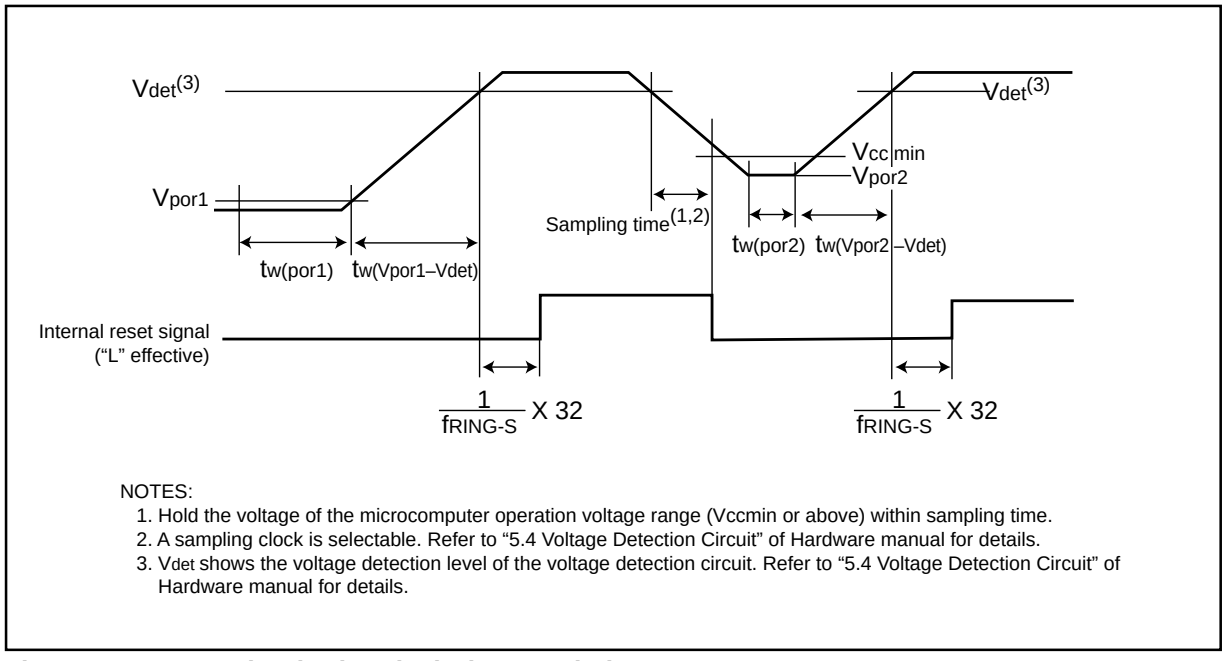
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor2	Power-on reset valid voltage	–20°C ≤ Topr < 85°C	—	—	Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled(2)	–20°C ≤ Topr < 85°C, tw(por2) ≥ 0s(4)	—	—	100	ms

NOTES:
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2 of Hardware Manual for details.
2. This condition is not applicable when using Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage (Vpor1) for greater than 10 seconds, refer to Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor1	Power-on reset valid voltage	–20°C ≤ Topr < 85°C	—	—	0.1	V
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s(2)	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	–20°C ≤ Topr < 0°C, tw(por1) ≥ 30s(2)	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	–20°C ≤ Topr < 0°C, tw(por1) ≥ 10s(2)	—	—	1	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s(2)	—	—	0.5	ms

NOTES:
1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock is selectable. Refer to “5.4 Voltage Detection Circuit” of Hardware manual for details.
3. Vdet shows the voltage detection level of the voltage detection circuit. Refer to “5.4 Voltage Detection Circuit” of Hardware manual for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency 1 / {td(HRoffset)+td(HR)} when the reset is released	VCC=5.0V, Topr=25 °C Set "40$_{16}$" in the HR1 register	—	8	—	MHz
td(HRoffset)	Settable high-speed on-chip oscillator minimum period	VCC=5.0V, Topr=25 °C Set "00$_{16}$" in the HR1 register	—	61	—	ns
td(HR)	High-speed on-chip oscillator period adjusted unit	Differences when setting "01$_{16}$" and "00$_{16}$" in the HR register	—	1	—	ns
—	High-speed on-chip oscillator frequency temperature dependence(1)	Frequency fluctuation in temperature range of -10 °C to 50 °C	—	±5	—	%
—	High-speed on-chip oscillator frequency temperature dependence(2)	Frequency fluctuation in temperature range of -40 °C to 85 °C	—	±10	—	%

NOTES:
1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.10 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on(2)		1		2000	µs
td(R-S)	STOP release time(3)				150	µs

NOTES:
1. The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2. This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.11 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA		Vcc-2.0	—	Vcc	V
			I_{OH}=-200µA		Vcc-0.3	—	Vcc	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-1 mA	Vcc-2.0	—	Vcc	V
			Drive capacity LOW	I_{OH}=-500µA	Vcc-2.0	—	Vcc	V
V_{OL}	"L" output voltage	Except P10 to P17, X_{OUT}	I_{OL}= 5 mA		—	—	2.0	V
			I_{OL}= 200 µA		—	—	0.45	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 15 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 5 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 200 µA	—	—	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 1 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}=500 µA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, T_{CIN}, RxD0, RxD1, P45			0.2	—	1.0	V
		$\overline{RESET}$			0.2	—	2.2	V
I_{IH}	"H" input current		V_I=5V		—	—	5.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	1.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:
1. Referenced to Vcc = AVcc = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.12 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
I_{CC}	Power supply current (V_{CC}=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V_{SS}		High-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	9	15	mA
				X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	8	14	mA
				X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	5	—	mA
			Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	4	—	mA
				X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	3	—	mA
				X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	2	—	mA
			High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division	—	4	8	mA
				Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.5	—	mA
			Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	470	900	µA
			Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation VC27="0"	—	40	80	µA
			Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off VC27="0"	—	38	76	µA
			Stop mode	Main clock off, Topr=-25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"	—	0.8	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements [Vcc=5V] (Unless otherwise noted: Vcc = 5V, Vss = 0V at Topr = 25 °C)

Table 5.13 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	50	–	ns
twH(XIN)	XIN input HIGH pulse width	25	–	ns
twL(XIN)	XIN input LOW pulse width	25	–	ns

Table 5.14 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	100	–	ns
twH(CNTR0)	CNTR0 input HIGH pulse width	40	–	ns
twL(CNTR0)	CNTR0 input LOW pulse width	40	–	ns

Table 5.15 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	400(1)	–	ns
twH(TCIN)	TCIN input HIGH pulse width	200(2)	–	ns
twL(TCIN)	TCIN input LOW pulse width	200(2)	–	ns

NOTES:
1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.5 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200	–	ns
tw(CKH)	CLKi input HIGH pulse width	100	–	ns
tw(CKL)	CLKi input LOW pulse width	100	–	ns
td(C-Q)	TxDi output delay time	–	80	ns
th(C-Q)	TxDi hold time	0	–	ns
tsu(D-C)	RxDi input setup time	35	–	ns
th(C-D)	RxDi input hold time	90	–	ns

Table 5.17 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	250(1)	–	ns
tw(INL)	$\overline{\text{INT0}}$ input LOW pulse width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

Table 5.19 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC}=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V_{SS}		High-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	8	13	mA
				X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	7	12	mA
				X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	5	—	mA
			Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	3	—	mA
				X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
				X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
			High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division	—	3.5	7.5	mA
				Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.5	—	mA
			Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	420	800	µA
			Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation VC27="0"	—	37	74	µA
			Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off VC27="0"	—	35	70	µA
			Stop mode	Main clock off, Topr=-25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"	—	0.7	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Timing requirements [VCC=3V] (Unless otherwise noted: VCC = 3V, VSS = 0V at Topr = 25 °C)

Table 5.20 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	100	–	ns
tWH(XIN)	XIN input HIGH pulse width	40	–	ns
tWL(XIN)	XIN input LOW pulse width	40	–	ns

Table 5.21 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300	–	ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120	–	ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120	–	ns

Table 5.22 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200(1)	–	ns
tWH(TCIN)	TCIN input HIGH pulse width	600(2)	–	ns
tWL(TCIN)	TCIN input LOW pulse width	600(2)	–	ns

NOTES:
1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300	–	ns
tW(CKH)	CLKi input HIGH pulse width	150	–	ns
tW(CKL)	CLKi input LOW pulse width	150	–	ns
td(C-Q)	TxDi output delay time	–	160	ns
th(C-Q)	TxDi hold time	0	–	ns
tsu(D-C)	RxDi input setup time	55	–	ns
th(C-D)	RxDi input hold time	90	–	ns

Table 5.24 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	380(1)	–	ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2 . When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

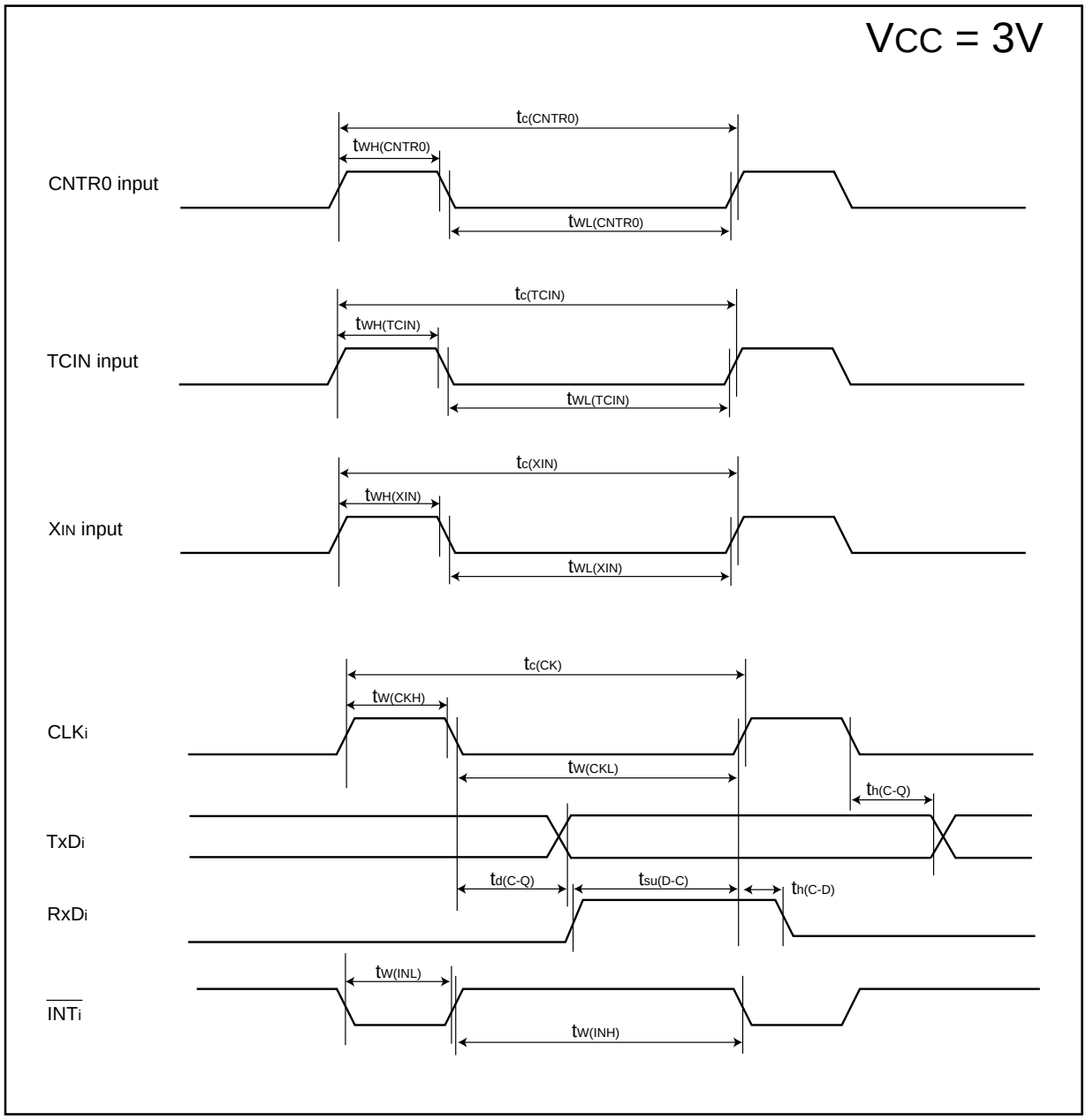
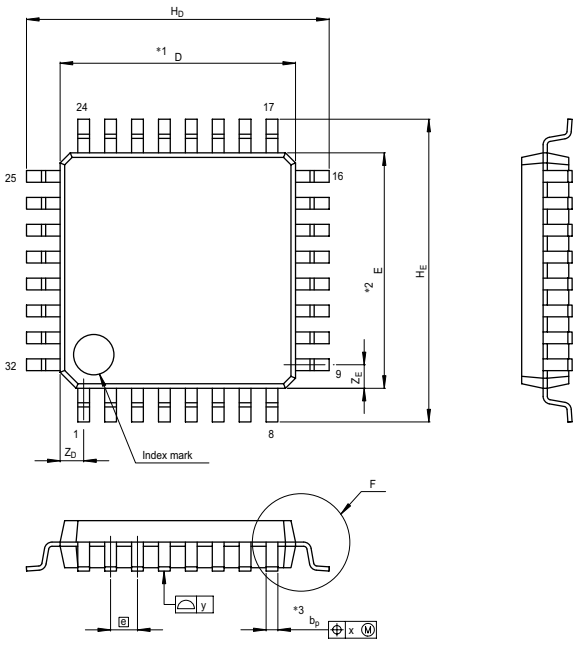
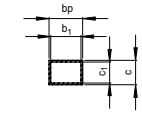


Figure 5.5 Vcc=3V timing diagram

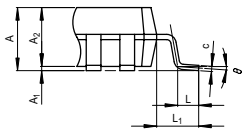
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Rev.	Date	Description	
		Page	Summary
1.10	Apr.27.2005	17	Table 5.7, 5.8 revised
		18	Table 5.10, Table 5.11 partly revised
		22	Table 5.18 partly revised
		26	Package Dimensions revised
1.20	Jan.27.2006	2	Table 1.1 Performance outline revised
		3	Figure 1.1 Block diagram partly revised
		4	1.4 Product Information, title of Table 1.2 "Product List" → "Product Informaton" revised ROM capacity; "Program area" → "Program ROM", "Data area" → "Data flash" revised Figure 1.2 Type No., Memory Size, and Package partly revised
		6	Table 1.3 Pin description revised
		7-8	2 Central Processing Unit (CPU) revised Figure 2.1 CPU register revised
		9	3 Memory, Figure 3.1 Memory Map; "Program area" → "Program ROM", "Data area" → "Data flash" revised
		10	Table 4.1 SFR Information(1) NOTES:1 revised
		11	Table 4.2 SFR Information(2) NOTES:1 revised
		12	Table 4.3 SFR Information(3); 0081_{16}: "Prescaler Y" → "Prescaler Y Register" 0082_{16}: "Timer Y Secondary" → "Timer Y Secondary Register" 0083_{16}: "Timer Y Primary" → "Timer Y Primary Register" 0085_{16}: "Prescaler Z" → "Prescaler Z Register" 0086_{16}: "Timer Z Secondary" → "Timer Z Secondary Register" 0087_{16}: "Timer Z Primary" → "Timer Z Primary Register" $008C_{16}$: "Prescaler X" → "Prescaler X Register" revised NOTES:1, 2 revised
		13	Table 4.4 SFR Information(4) NOTES:1 revised
		14	Table 5.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised
		15	Table 5.3 A/D Conversion Characteristics; "A/D operation clock frequency" → "A/D operating clock frequency" revised NOTES: 1, 2, 3, 4 revised
		16	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; "Data retention duration" → "Data hold time" revised "Topr" → "Ambient temperature" NOTES: 1 to 7 added Measuring condition of byte program time and block erase time deleted
		17	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical characteristics "Data retention duration" → "Data hold time" revised "Topr" → "Ambient temperature" NOTES: 1, 3 revised, NOTES: 9 added Measuring condition of byte program time and block erase time deleted
		18	Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2) NOTES: 3 revised
		19	Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics; "High-speed on-chip oscillator temperature dependence" → "High-speed on-chip oscillator frequency temperature dependence" revised Table 5.11 Electrical Characteristics (1) [V_{CC}=5V]; "$P1_0$ to $P1_7$ Except X_{OUT}" → "Except $P1_0$ to $P1_7$, X_{OUT}" revised

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