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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1cs288

Datasheet Categories 6-14
Microsemi SoC Products Group Safety Critical, Life Support, and High-Reliability Applications Policy 6-14

Power Consumption of Various Internal Resources

***Table 2-14* • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	3.39	3.40	5.05	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	1.14	1.83	2.50	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	1.15	1.15	1.15	µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.12	0.12	0.12	µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07	0.07	0.07	µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	1.04	0.79	0.79	µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11				
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11				
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00			µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00			µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60			µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00			µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88			mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80			µW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98			mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30			mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00			mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25			mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00			mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00			µW
PAC22	MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1]	VCC	1.5 V	67.50			mW
PAC23	Temperature Monitor Power Contribution	See Table 2-94 on page 2-79	–	1.23			mW

***Table 2-70* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* *See Figure 2-15 on page 2-46 for more information.*

Input Register

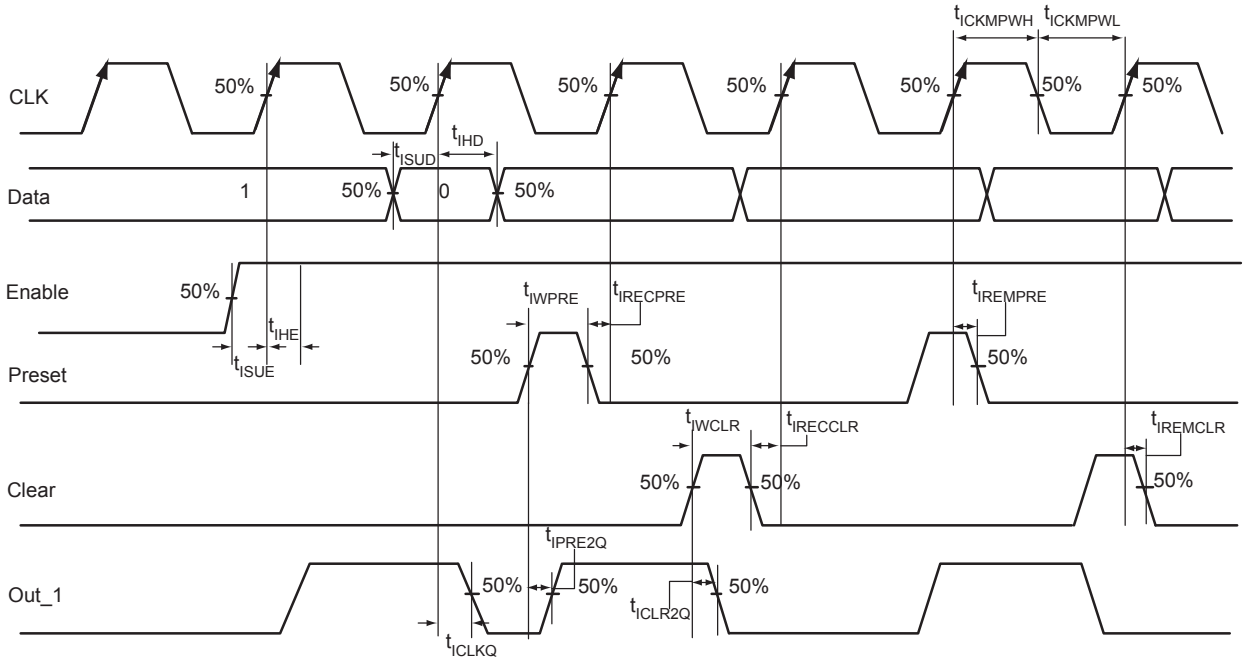

Figure 2-16 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-71 • **Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.55	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.55	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

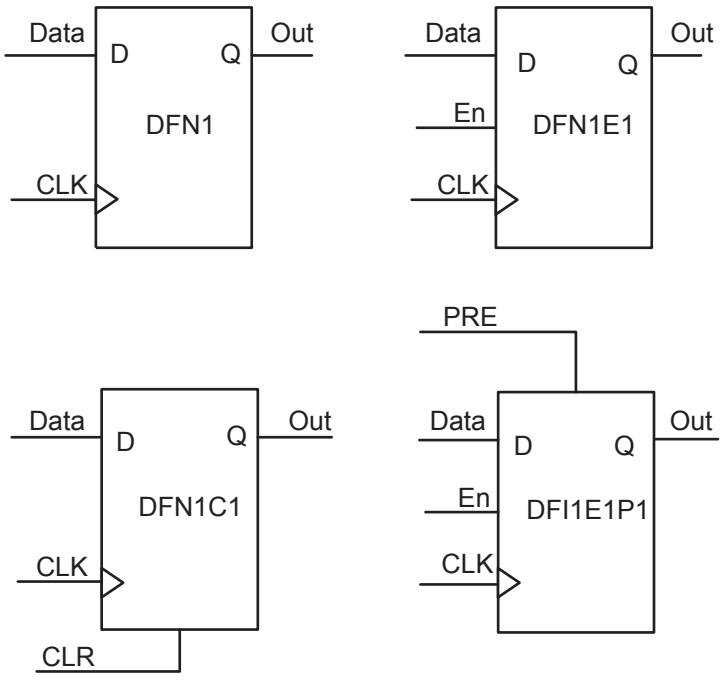

Figure 2-25 • Sample of Sequential Cells

***Table 2-96* • ABPS Performance Specifications (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input referred offset voltage					
	GDEC[1:0] = 11	–0.31	–0.07	0.31	% FS*
	–40ºC to +100ºC	–1.00		1.47	% FS*
	GDEC[1:0] = 10	–0.34	–0.07	0.34	% FS*
	–40ºC to +100ºC	–0.90		1.37	% FS*
	GDEC[1:0] = 01	–0.61	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.05		1.35	% FS*
	GDEC[1:0] = 00	–0.39	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.06		1.38	% FS*
SINAD		53	56		dB
Non-linearity	RMS deviation from BFSL			0.5	% FS*
Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 11*	GDEC[1:0] = 11 (±2.56 range), –1 dBFS input				
	12-bit mode 10 KHz	8.6	9.1		Bits
	12-bit mode 100 KHz	8.6	9.1		Bits
	10-bit mode 10 KHz	8.5	8.9		Bits
	10-bit mode 100 KHz	8.5	8.9		Bits
	8-bit mode 10 KHz	7.7	7.8		Bits
	8-bit mode 100 KHz	7.7	7.8		Bits
Large-signal bandwidth	–1 dBFS input		1		MHz
Analog settling time	To 0.1% of final value (with ADC load)			10	µs
Input resistance			1		MΩ
Power supply rejection ratio	DC (0–1 KHz)	38	40		dB
ABPS power supply current requirements (not including ADC or VAREFx)	ABPS_EN = 1 (operational mode)				
	VCC33A		123	134	µA
	VCC33AP		89	94	µA
	VCC15A		1		µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

4 – SmartFusion Programming

SmartFusion cSoCs have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
   a. A2F060 and A2F500: The FPGA fabric, eNVM, and eFROM
   b. A2F200: Only the FPGA fabric and the eNVM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. Table 4-1 describes the JTAG programming hardware that will program a SmartFusion cSoC and Table 4-2 defines the JTAG pins that provide the interface for the programming hardware.

***Table 4-1* • Supported JTAG Programming Hardware**

Dongle	Source	JTAG	SWD[1]	SWV[2]	Program FPGA	Program eFROM	Program eNVM
FlashPro3/4	SoC Products Group	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes

Notes:

1. *SWD = ARM Serial Wire Debug*
2. *SWV = ARM Serial Wire Viewer*
3. *Planned support*

***Table 4-2* • JTAG Pin Descriptions**

Pin Name	Description
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

User-Defined Supply Pins

Name	Type	Polarity/ Bus Size	Description
VAREF0	Input	1	Analog reference voltage for first ADC. The SmartFusion cSoC can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the *SmartFusion Programmable Analog User's Guide* for more information. The SoC Products Group recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, the VAREFOUT pin must be connected to the appropriate ADC VAREFx input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1 and VAREF2 together, if ADC0, ADC1, and ADC2 all are used.
VAREF1	Input	1	Analog reference voltage for second ADC See "VAREF0" above for more information.
VAREF2	Input	1	Analog reference voltage for third ADC See "VAREF0" above for more.
VAREFOUT	Out	1	Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.

TQ144	
Pin Number	**A2F060 Function**
37	VCC33AP
38	VCC33N
39	SDD0
40	GNDA
41	GNDAQ
42	GNDAQ
43	ADC0
44	ADC1
45	ADC2
46	ADC3
47	ADC4
48	ADC5
49	ADC6
50	ADC7
51	ADC8
52	ADC9
53	ADC10
54	NC
55	NC
56	NC
57	GND15ADC0
58	VCC15ADC0
59	GND33ADC0
60	VCC33ADC0
61	GND33ADC0
62	VAREF0
63	ABPS0
64	ABPS1
65	CM0
66	TM0
67	GNDTM0
68	GNDAQ
69	GNDA
70	GNDVAREF
71	VAREFOUT
72	PU_N

TQ144	
Pin Number	**A2F060 Function**
109	VPP
110	GNDQ
111	GCA1/IO20PDB0V0
112	GCA0/IO20NDB0V0
113	GCB1/IO19PDB0V0
114	GCB0/IO19NDB0V0
115	GCC1/IO18PDB0V0
116	GCC0/IO18NDB0V0
117	VCCFPGAIOB0
118	GND
119	VCC
120	IO14PDB0V0
121	IO14NDB0V0
122	IO13NSB0V0
123	IO11PDB0V0
124	IO11NDB0V0
125	IO09PDB0V0
126	IO09NDB0V0
127	VCCFPGAIOB0
128	GND
129	IO07PDB0V0
130	IO07NDB0V0
131	IO06PDB0V0
132	IO06NDB0V0
133	IO05PDB0V0
134	IO05NDB0V0
135	IO03PDB0V0
136	IO03NDB0V0
137	VCCFPGAIOB0
138	GND
139	VCC
140	IO01PDB0V0
141	IO01NDB0V0
142	IO00PDB0V0
143	IO00NDB0V0
144	GNDQ

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
C21	IO17NDB0V0	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
D1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
D3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D19	GND	GND	GND
D21	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E3	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E5	GNDQ	GNDQ	GNDQ
E6	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
E7	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
E8	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
E9	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
E10	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
E11	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
E12	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
E13	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
E14	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
E15	GCC0/IO18NPB0V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
E16	GCA1/IO20PPB0V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E17	GCC1/IO18PPB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
E19	GCB2/IO22PPB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
E21	IO21NDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
F1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F5	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
F6	EMC_DB[11]/IO43PDB5V0	EMC_DB[11]/IO69PDB5V0	EMC_DB[11]/IO86PDB5V0
F7	GND	GND	GND
F8	NC	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
F9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
F10	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
F11	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
M21	TRSTB	TRSTB	TRSTB
N1	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
N3	GND	GND	GND
N5	GPIO_4/IO29RSB4V0	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
N6	GPIO_8/IO25RSB4V0	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
N7	GPIO_9/IO24RSB4V0	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
N8	VCC	VCC	VCC
N9	GND	GND	GND
N10	VCC	VCC	VCC
N11	GND	GND	GND
N12	VCC	VCC	VCC
N13	GND	GND	GND
N14	VCC	VCC	VCC
N15	GND	GND	GND
N16	TCK	TCK	TCK
N17	TDI	TDI	TDI
N19	GNDENVM	GNDENVM	GNDENVM
N21	VCCENVM	VCCENVM	VCCENVM
P1	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
P3	GPIO_7/IO26RSB4V0	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0
P5	GPIO_6/IO27RSB4V0	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
P6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
P8	GND	GND	GND
P9	VCC	VCC	VCC
P10	GND	GND	GND
P11	VCC	VCC	VCC
P12	GND	GND	GND
P13	VCC	VCC	VCC
P14	GND	GND	GND
P16	JTAGSEL	JTAGSEL	JTAGSEL
P17	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

Notes:

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2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
32	VCCRCOSC	VCCRCOSC
33	MSS_RESET_N	MSS_RESET_N
34	VCCESRAM	VCCESRAM
35	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
36	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
37	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
38	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
39	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
40	GND	GND
41	VCCMSSIOB4	VCCMSSIOB4
42	VCC	VCC
43	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
44	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
45	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
46	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
47	MAC_CLK	MAC_CLK
48	GNDSDD0	GNDSDD0
49	VCC33SDD0	VCC33SDD0
50	VCC15A	VCC15A
51	PCAP	PCAP
52	NCAP	NCAP
53	VCC33AP	VCC33AP
54	VCC33N	VCC33N
55	SDD0	SDD0
56	GNDA	GNDA
57	GNDAQ	GNDAQ
58	ABPS0	ABPS0
59	ABPS1	ABPS1
60	CM0	CM0
61	TM0	TM0
62	GNDTM0	GNDTM0

Notes:

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2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
D15	GCA1/IO20PDB0V0	IO24NDB1V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E3	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ	GNDQ
E6	GND	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
E13	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND	GND
F8	VCC	VCC	VCC
F9	GND	GND	GND
F10	VCC	VCC	VCC
F11	GND	GND	GND
F12	IO22NDB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
F13	NC	GNDQ	GNDQ

Notes:

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2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
K12	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
K13	GND	GND	GND
K14	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
K15	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
K16	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
L1	GND	GND	GND
L2	GPIO_2/IO31RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
L3	GPIO_3/IO30RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
L4	GPIO_4/IO29RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
L5	GPIO_9/IO24RSB4V0	MAC_CLK	MAC_CLK
L6	GND	GND	GND
L7	VCC	VCC	VCC
L8	GND	GND	GND
L9	VCC	VCC	VCC
L10	GND	GND	GND
L11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
L12	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
L13	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
L14	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
L15	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
L16	GND	GND	GND
M1	GPIO_5/IO28RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
M2	GPIO_6/IO27RSB4V0	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
M3	GPIO_7/IO26RSB4V0	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
M4	GND	GND	GND
M5	NC	ADC3	ADC3
M6	NC	GND15ADC0	GND15ADC0
M7	GND33ADC0	GND33ADC1	GND33ADC1
M8	GND33ADC0	GND33ADC1	GND33ADC1
M9	ADC7	ADC4	ADC4
M10	GNDTM0	GNDTM1	GNDTM1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
C15	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO19NPB0V0	GBA0/IO23NPB0V0
C20	NC	NC
C21	GBC2/IO21PDB1V0	GBC2/IO30PDB1V0
C22	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
D1	GND	GND
D2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC	NC
D5	NC	NC
D6	GND	GND
D7	NC	IO00NPB0V0
D8	NC	IO03NPB0V0
D9	GND	GND
D10	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
D14	GND	GND
D15	GBC1/IO17PPB0V0	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
D17	GND	GND
D18	GBA1/IO19PPB0V0	GBA1/IO23PPB0V0
D19	NC	NC
D20	NC	NC
D21	IO21NDB1V0	IO30NDB1V0
D22	GND	GND
E1	GFC2/IO67PPB5V0	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5	VCCFPGAIOB5
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
P11	GND	GND
P12	VCC	VCC
P13	GND	GND
P14	VCC	VCC
P15	GND	GND
P16	VCCFPGAIOB1	VCCFPGAIOB1
P17	TDI	TDI
P18	TCK	TCK
P19	GND	GND
P20	TMS	TMS
P21	TDO	TDO
P22	TRSTB	TRSTB
R1	MSS_RESET_N	MSS_RESET_N
R2	VCCFPGAIOB5	VCCFPGAIOB5
R3	GPIO_1/IO46RSB4V0	GPIO_1/IO55RSB4V0
R4	NC	NC
R5	NC	NC
R6	NC	NC
R7	NC	NC
R8	GND	GND
R9	VCC	VCC
R10	GND	GND
R11	VCC	VCC
R12	GND	GND
R13	VCC	VCC
R14	GND	GND
R15	VCC	VCC
R16	JTAGSEL	JTAGSEL
R17	NC	NC
R18	NC	NC
R19	NC	NC
R20	NC	NC
R21	VCCFPGAIOB1	VCCFPGAIOB1
R22	NC	NC

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 9 (continued)	The following note was added to Table 2-86 • SmartFusion CCC/PLL Specification in regard to delay increments in programmable delay blocks (SAR 34816): "When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information."	2-63
	Figure 2-36 • FIFO Read and Figure 2-37 • FIFO Write have been added (SAR 34851).	2-72
	Information regarding the MSS resetting itself after IAP of the FPGA fabric was added to the "Reprogramming the FPGA Fabric Using the Cortex-M3" section (SAR 37970).	4-8
	Instructions for unused VCC33ADCx pins were revised in "Supply Pins" (SAR 41137).	5-1
	Libero IDE was changed to Libero SoC throughout the document (SAR 40264).	N/A
Revision 8 (March 2012)	In the "Analog Front-End (AFE)" section, the resolution for the first-order sigma delta DAC was corrected from 12-bit to "8-bit, 16-bit, or 24-bit." The same correction was made in the "SmartFusion cSoC Family Product Table" (SAR 36541).	I, II
	The "SmartFusion cSoC Family Product Table" was revised to break out the features by package as well as device. The table now indicates that only one SPI is available for the PQ208 package in A2F200 and A2F500, and in the TQ144 package for A2F060 (SAR 33477). The EMC address bus size has been corrected to 26 bits (SAR 35664).	II
	The "SmartFusion cSoC Device Status" table was revised to change the CS288 package for A2F200 and A2F500 from preliminary to production status (SAR 37811).	III
	TQ144 package information for A2F060 was added to the "Package I/Os: MSS + FPGA I/Os" table, "SmartFusion cSoC Device Status" table, "Product Ordering Codes", and "Temperature Grade Offerings" table (SAR 36246).	III, VI
	Table 1 • SmartFusion cSoC Package Sizes Dimensions is new (SAR 31178).	III
	The Halogen-Free Packaging code (H) was removed from the "Product Ordering Codes" table (SAR 34017).	VI
	The "Specifying I/O States During Programming" section is new (SAR 34836).	1-3
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—P_{CLOCK}" section, was corrected to the "Device Architecture" chapter in the *SmartFusion FPGA Fabric User's Guide* (SAR 34742).	2-15
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34891).	2-30, 2-24
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34799): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-32
	In the SRAM "Timing Characteristics" tables, reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34874).	2-69
	The note for Table 2-93 • Current Monitor Performance Specification was modified to include the statement that the restriction on the TM pad being no greater than 10 mV above the CM pad.is applicable only if current monitor is used (SAR 26373).	2-78
	The unit "FR" in Table 2-96 • ABPS Performance Specifications and Table 2-98 • Analog Sigma-Delta DAC, used to designate full-scale error, was changed to "FS" and clarified with a table note (SAR 35342).	2-82, 2-85

Revision	Changes	Page
Revision 7 (continued)	The following sentence was removed from the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section because it is incorrect (SAR 31047): "The many different supplies can power up in any sequence with minimized current spikes or surges."	2-4
	Table 2-8 • Quiescent Supply Current Characteristics was divided into two tables: one for power supplies configurations and one for quiescent supply current. SoC mode was added to both tables (SAR 26378) and VCOMPLAx was removed from Table 2-8 • Power Supplies Configuration (SAR 29591). Quiescent supply current values were updated in Table 2-9 • Quiescent Supply Current Characteristics (SAR 33067).	2-10
	The "Total Static Power Consumption—P_{STAT}" section was revised: "$N_{eNVM\text{-}BLOCKS}$ * P_{DC4}" was removed from the equation for P_{STAT} (SAR 33067).	2-14
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs were revised to reflect updates in the SmartFusion power calculator (SARs 26405, 33067).	2-12, 2-13
	Table 2-82 • A2F060 Global Resource is new (SAR 33132).	2-61
	Output duty cycle was corrected to 50% in Table 2-83 • Electrical Characteristics of the RC Oscillator. It was incorrectly noted as 1% previously. Operating current for 3.3 domain was added (SAR 32940).	2-61
	Table 2-86 • SmartFusion CCC/PLL Specification was revised to add information and measurements regarding CCC output peak-to-peak period jitter (SAR 32996).	2-63
	The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-38 • FIFO Reset, and the FIFO "Timing Waveforms" tables were revised to ensure consistency with the software names (SAR 29991).	2-66 to 2-75
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised to correct the maximum frequencies (SAR 32410).	2-76
	Table 2-97 • Comparator Performance Specifications was moved to the "SmartFusion DC and Switching Characteristics" section from the SmartFusion Programmable Analog User's Guide because the information is extracted from characterization (SAR 24298).	2-84
	The hysteresis section in Table 2-97 • Comparator Performance Specifications was revised (SAR 33158).	2-84
	The "SmartFusion Development Tools" was extensively updated (SAR 33216).	3-1
	The text following Table 4-2 • JTAG Pin Descriptions was updated to add information on control of the JTAGSEL pin. Manual jumpers on the evaluation and development kits allow manual selection of this function for J-Link and ULINK debuggers (SAR 25592).	4-7