

Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1cs288i

VCCxxxxIOBx Trip Point:Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$ Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$ **VCC Trip Point:**Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$ Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1\text{ V}$

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to "[Specifying I/O States During Programming](#)" on page 1-3.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see [Figure 2-1](#) on [page 2-6](#) for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the [ProASIC3 FPGA Fabric User's Guide](#) for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 2-6 • Package Thermal Resistance

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
A2F200M3F-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
A2F200M3F-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
A2F200M3F-CS288	26.6	20.2	18.1	7.3	9.4	°C/W
A2F200M3F-PQG208I	38.5	34.6	33.1	0.7	31.6	°C/W

Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03			mW
PAC25	ABPS Power Contribution	See Table 2-96 on page 2-82	–	0.70			mW
PAC26	Sigma-Delta DAC Power Contribution ²	See Table 2-98 on page 2-85	–	0.58			mW
PAC27	Comparator Power Contribution	See Table 2-97 on page 2-84	–	1.02			mW
PAC28	Voltage Regulator Power Contribution ³	See Table 2-99 on page 2-87	–	36.30			mW

Notes:

1. For a different use of MSS peripherals and resources, refer to SmartPower.
2. Assumes Input = Half Scale Operation mode.
3. Assumes 100 mA load on 1.5 V domain.

Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PDC1	Core static power contribution in SoC mode	VCC	1.5 V	11.10	23.70	37.95	mW
PDC2	Device static power contribution in Standby Mode	See Table 2-8 on page 2-10	–	11.10	23.70	37.95	mW
PDC3	Device static power contribution in Time Keeping mode	See Table 2-8 on page 2-10	3.3 V	33.00	33.00	33.00	μW
PDC7	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11.				
PDC8	Static contribution per output pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11.				
PDC9	Static contribution per PLL	VCC	1.5 V	2.55	2.55	2.55	mW

Table 2-16 • eNVM Dynamic Power Consumption

Parameter	Description	Condition	Min.	Typ.	Max.	Units
eNVMSystem	eNVM array operating power	Idle		795		μA
		Read operation	See Table 2-14 on page 2-12.			
		Erase		900		μA
		Write		900		μA
PNVMCTRL	eNVM controller operating power			20		μW/MHz

Table 2-28 • I/O Output Buffer Maximum Resistances¹
 Applicable to MSS I/O Banks

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	8mA	50	150
2.5 V LVCMOS	8 mA	50	100
1.8 V LVCMOS	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC_{xxxxIOBx}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the [Microsemi SoC Products Group website](#).
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
 Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCC _{xxxxIOBx}	R _(WEAK PULL-UP) ¹ (Ω)		R _(WEAK PULL-DOWN) ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (V_{OLspec}) / I_{(WEAK PULL-DOWN-MIN)}$

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-47 • Minimum and Maximum DC Input and Output Levels
Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	-0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx - 0.45	2	2	11	9	15	15
4 mA	-0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx - 0.45	4	4	22	17	15	15
6 mA	-0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx - 0.45	6	6	44	35	15	15
8 mA	-0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx - 0.45	8	8	51	45	15	15
12 mA	-0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx - 0.45	12	12	74	91	15	15
16 mA	-0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx - 0.45	16	16	74	91	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-48 • Minimum and Maximum DC Input and Output Levels
Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
4 mA	-0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx - 0.45	4	4	22	17	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

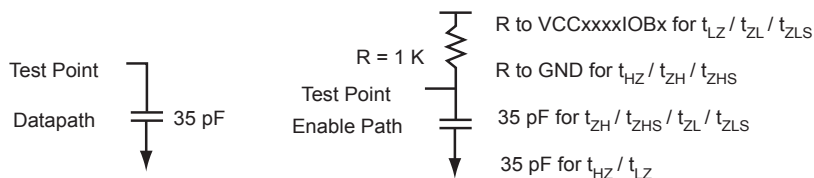


Figure 2-8 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)	C _{LOAD} (pF)
0	1.8	0.9	-	35

* Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-59 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
Per PCI specification	Per PCI curves										15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in [Figure 2-10](#).

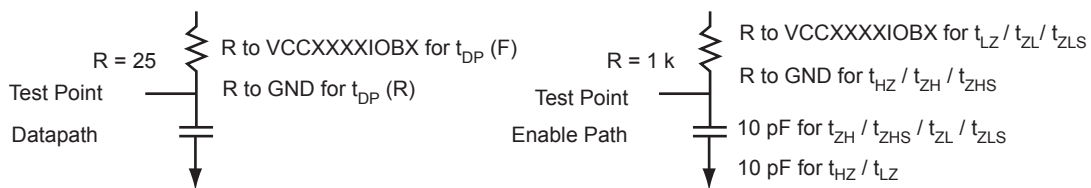


Figure 2-10 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in [Table 2-60](#).

Table 2-60 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)	C _{LOAD} (pF)
0	3.3	0.285 * VCCxxxIOBx for t _{DP(R)} 0.615 * VCCxxxIOBx for t _{DP(F)}	–	10

* Measuring point = V_{trip}. See [Table 2-22 on page 2-24](#) for a complete table of trip points.

Timing Characteristics

Table 2-61 • 3.3 V PCI

Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxIOBx = 3.0 V

Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.60	2.54	0.04	0.82	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-62 • 3.3 V PCI-X

Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxIOBx = 3.0 V

Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.60	2.54	0.04	0.77	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-63 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}^1	Output lower current	0.65	0.91	1.16	mA
I_{OH}^1	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}^2	Input high leakage current			15	μ A
I_{IL}^2	Input low leakage current			15	μ A
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

- I_{OL}/I_{OH} defined by $V_{ODIFF}/(\text{resistor network})$.
- Currents are measured at 85°C junction temperature.

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* Measuring point = V_{trip} . See Table 2-22 on page 2-24 for a complete table of trip points.

Timing Characteristics

Table 2-65 • LVDS

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
 Worst-Case VCCFPGAIOBx = 2.3 V
 Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.83	0.04	1.87	ns
–1	0.50	1.53	0.03	1.55	ns

Notes:

- For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.
- The above mentioned timing parameters correspond to 24mA drive strength.

Output Register

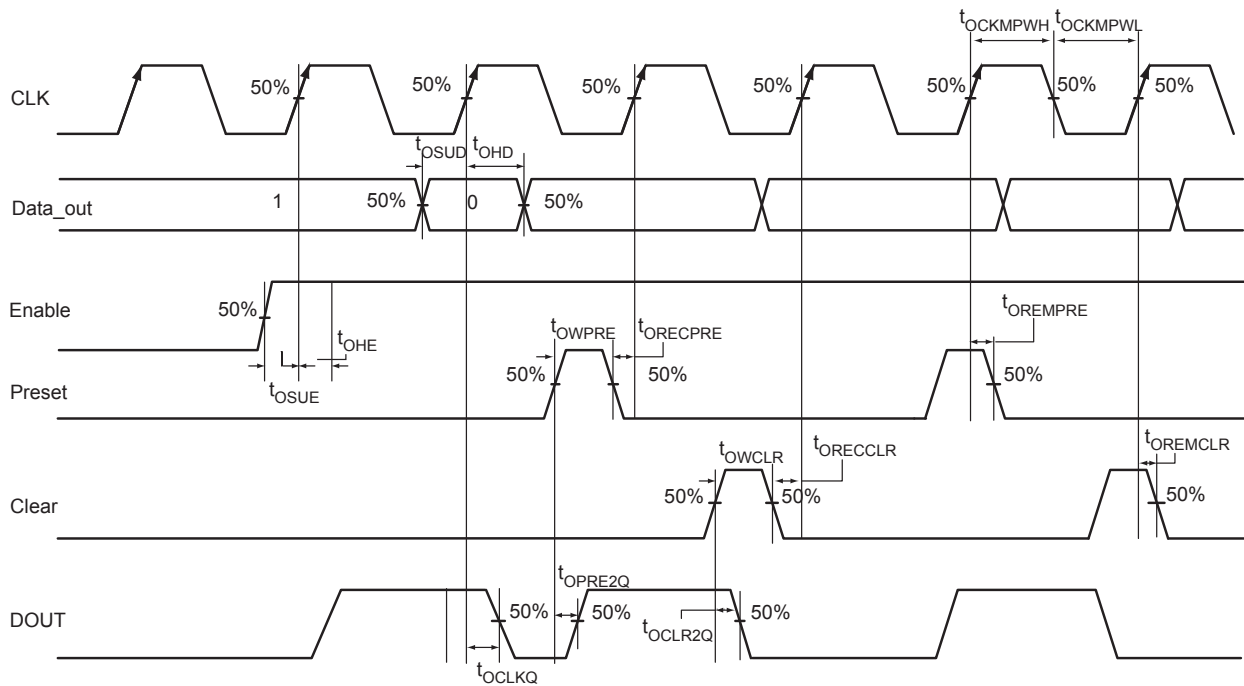


Figure 2-17 • Output Register Timing Diagram

Timing Characteristics

Table 2-72 • Output Data Register Propagation Delays
 Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.72	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.38	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.98	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.98	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Output Enable Register

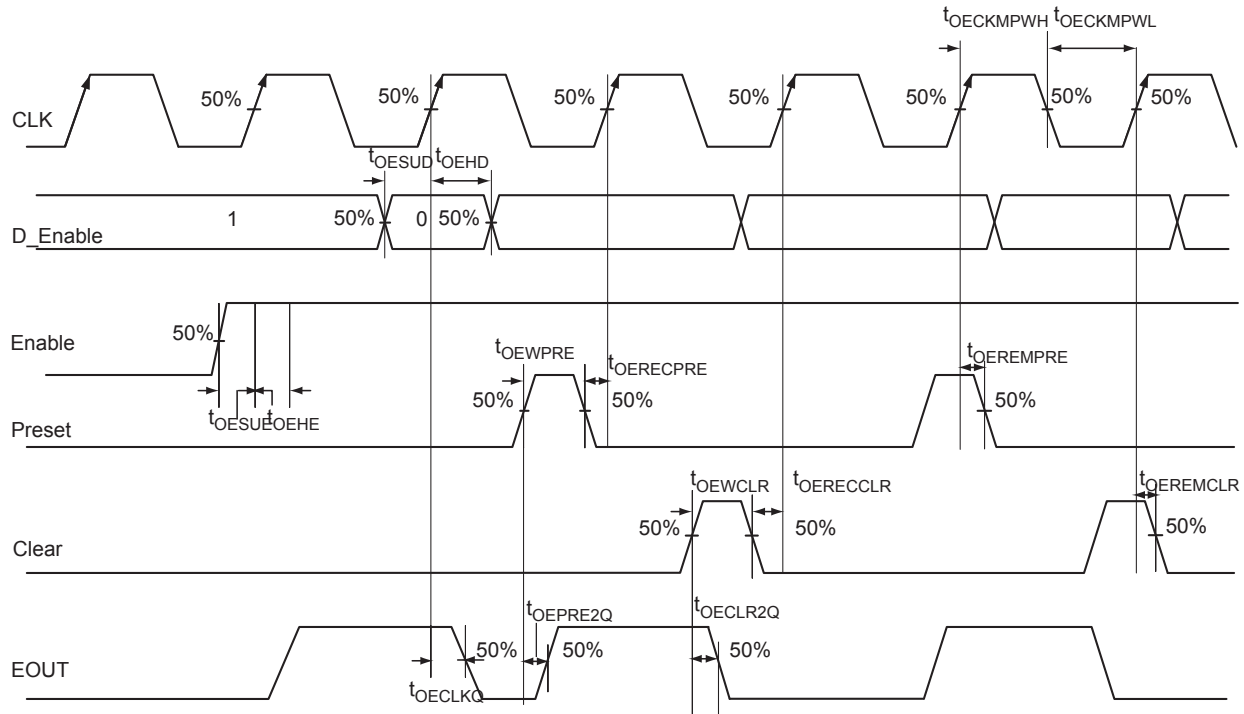


Figure 2-18 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-73 • Output Enable Register Propagation Delays
Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.54	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.38	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.53	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-86 • SmartFusion CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units				
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz				
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350 ¹	MHz				
Delay Increments in Programmable Delay Blocks ^{2,3,4}		160		ps				
Number of Programmable Values in Each Programmable Delay Block			32					
Input Period Jitter			1.5	ns				
Acquisition Time								
LockControl = 0			300	μs				
LockControl = 1			6.0	ms				
Tracking Jitter ⁵								
LockControl = 0			1.6	ns				
LockControl = 1			0.8	ns				
Output Duty Cycle	48.5		5.15	%				
Delay Range in Block: Programmable Delay ^{1,2,3}	0.6		5.56	ns				
Delay Range in Block: Programmable Delay ^{2,3}	0.025		5.56	ns				
Delay Range in Block: Fixed Delay ^{2,3}		2.2		ns				
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} ^{6,7}	Maximum Peak-to-Peak Period Jitter							
	SSO ≤ 2		SSO ≤ 4		SSO ≤ 8		SSO ≤ 16	
	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

- One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the *SmartFusion Microcontroller Subsystem User's Guide*.
- This delay is a function of voltage and temperature. See [Table 2-7 on page 2-9](#) for deratings.
- $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
- When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the *Liberio SoC Online Help* associated with the core for more information.
- Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
- Measurement done with LVTTTL 3.3 V 12 mA I/O drive strength and High slew rate. $V_{CC}/V_{CCPLL} = 1.425\text{ V}$, $V_{CCI} = 3.3\text{ V}$, 20 pF output load. All I/Os are placed outside of the PLL bank.
- SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within $\pm 200\text{ ps}$ of each other.
- VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.

Analog Sigma-Delta Digital to Analog Converter (DAC)

Unless otherwise noted, sigma-delta DAC performance is specified at 25°C with nominal power supply voltages, using the internal sigma-delta modulators with 16-bit inputs, HCLK = 100 MHz, modulator inputs updated at a 100 KHz rate, in voltage output mode with an external 160 pF capacitor to ground, after trimming and digital [pre-]compensation.

Table 2-98 • Analog Sigma-Delta DAC

Specification	Test Conditions	Min.	Typ.	Max.	Units
Resolution		8		24	Bits
Output range			0 to 2.56		V
	Current output mode		0 to 256		μA
Output Impedance		6	10	12	KΩ
	Current output mode	10			MΩ
Output voltage compliance	Current output mode		0–3.0		V
	–40°C to +100°C	0–2.7		0–3.4	V
Gain error	Voltage output mode		0.3	±2	%
	A2F060: –40°C to +100°C		0.3	±2	%
	A2F200: –40°C to +100°C		1.2	±5.3	%
	A2F500: –40°C to +100°C		0.3	±2	%
	Current output mode		0.3	±2	%
	A2F060: –40°C to +100°C		0.3	±2	%
	A2F200: –40°C to +100°C		1.2	±5.3	%
	A2F500: –40°C to +100°C		0.3	±2	%
Output referred offset	DACBYTE0 = h'00 (8-bit)		0.25	±1	mV
	–40°C to +100°C		1	±2.5	mV
	Current output mode		0.3	±1	μA
	–40°C to +100°C		1	±2.5	μA
Integral non-linearity	RMS deviation from BFSL		0.1	0.3	% FS*
Differential non-linearity			0.05	0.4	% FS*
Analog settling time			Refer to Figure 2-44 on page 2-86		μs
Power supply rejection ratio	DC, full scale output	33	34		dB

Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the *SmartFusion Programmable Analog User's Guide* for more information.

The JTAGSEL pin selects the FPGA TAP controller or the Cortex-M3 debug logic. When JTAGSEL is asserted, the FPGA TAP controller is selected and the TRSTB input into the Cortex-M3 is held in a reset state (logic 0), as depicted in Figure 4-1. Users should tie the JTAGSEL pin high externally.

Microsemi's free Eclipse-based IDE, SoftConsole, has the ability to control the JTAGSEL pin directly with the FlashPro4 programmer. Manual jumpers are provided on the evaluation and development kits to allow manual selection of this function for the J-Link and ULINK debuggers.

Note: Standard ARM JTAG connectors do not have access to the JTAGSEL pin. SoftConsole automatically selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care."

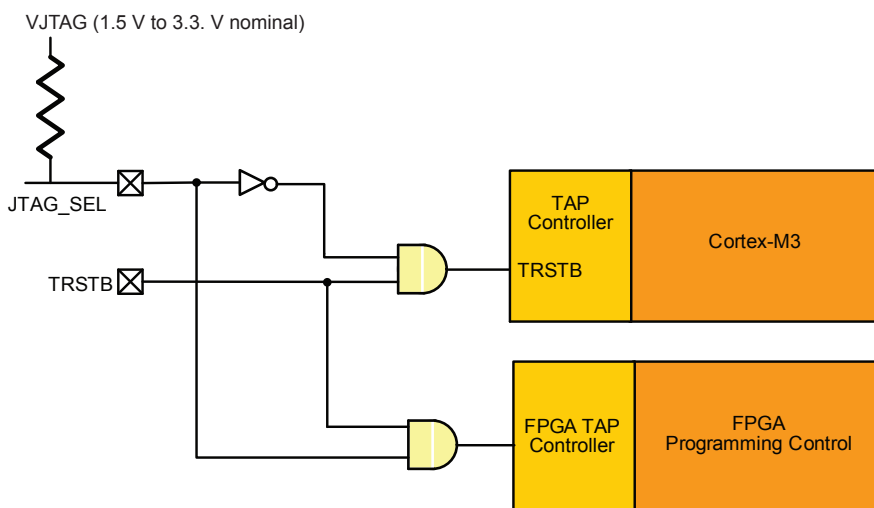


Figure 4-1 • TRSTB Logic

In-Application Programming

In-application programming refers to the ability to reprogram the various flash areas under direct supervision of the Cortex-M3.

Reprogramming the FPGA Fabric Using the Cortex-M3

In this mode, the Cortex-M3 is executing the programming algorithm on-chip. The IAP driver can be incorporated into the design project and executed from eNVM or eSRAM. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog. The new bitstream to be programmed into the FPGA can reside on the user's printed circuit board (PCB) in a separate SPI flash memory. Alternately, the user can modify the existing projects supplied by the SoC Products Group and, via custom handshaking software, throttle the download of the new image and program the FPGA a piece at a time in real time. A cost-effective and reliable approach would be to store the bitstream in an external SPI flash. Another option is storing a redundant bitstream image in an external SPI flash and loading the newest version into the FPGA only when receiving an IAP command. Since the FPGA I/Os are tristated or held at predefined or last known state during FPGA programming, the user must use MSS I/Os to interface to external memories. Since there are two SPI controllers in the MSS, the user can dedicate one to an SPI flash and the other to the particulars of an application. The amount of flash memory required to program the FPGA always exceeds the size of the eNVM block that is on-chip. The external memory controller (EMC) cannot be used as an interface to a memory device for storage of a bitstream because its I/O pads are FPGA I/Os; hence they are tristated when the FPGA is in a programming state.

The MSS resets itself after IAP of the FPGA fabric. This reset is internally asserted on MSS_RESETN by the power supply monitor (PSM) and reset controller of the MSS.

Re-Programming the eNVM Blocks Using the Cortex-M3

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

Secure Programming

For background, refer to the "Security in Low Power Flash Devices" chapter of the *Fusion FPGA Fabric User's Guide* on the SoC Products Group website. SmartFusion ISP behaves identically to Fusion ISP. IAP of SmartFusion cSoCs is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed with the protection of security measures by using the IAP driver.

Typical Programming and Erase Times

Table 4-3 documents the typical programming and erase times for two components of SmartFusion cSoCs, FPGA fabric and eNVM, using the SoC Products Group's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The **Program** action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

Table 4-3 • Typical Programming and Erase Times

	FPGA Fabric (seconds)			eNVM (seconds)			FlashROM (seconds)		
	A2F060	A2F200	A2F500	A2F060	A2F200	A2F500	A2F060	A2F200	A2F500
Erase	21	21	21	N/A	N/A	N/A	21	21	21
Program	28	35	48	18	39	71	22	22	22
Verify	2	6	12	9	18	37	1	1	1

References

User's Guides

DirectC User's Guide

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132588

In-System Programming (ISP) of Microsemi's Low-Power Flash Devices Using FlashPro4/3/3X

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129973

Programming Flash Devices HandBook

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129930

Application Notes on IAP Programming Technique

SmartFusion cSoC: Programming FPGA Fabric and eNVM Using In-Application Programming Interface App Note

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129818

SmartFusion cSoC: Basic Bootloader and Field Upgrade eNVM Through IAP Interface App Note

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129823

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

Table 5-2 • Relationships Between Signals in the Analog Front-End

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. ABPS_x_IN: Input to active bipolar prescaler channel *x*.
2. CM_x_H/L: Current monitor channel *x*, high/low side.
3. TM_x_IO: Temperature monitor channel *x*.
4. CMP_x_P/N: Comparator channel *x*, positive/negative input.
5. LVTTTL_x_IN: LVTTTL I/O channel *x*.
6. SDDM_x_OUT: Output from sigma-delta DAC MUX channel *x*.
7. SDD_x_OUT: Direct output from sigma-delta DAC channel *x*.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
D15	GCA1/IO20PDB0V0	IO24NDB1V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E3	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ	GNDQ
E6	GND	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
E13	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND	GND
F8	VCC	VCC	VCC
F9	GND	GND	GND
F10	VCC	VCC	VCC
F11	GND	GND	GND
F12	IO22NDB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
F13	NC	GNDQ	GNDQ

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
P10	TM0	TM3	TM3
P11	GND A	GND A	GND A
P12	VCCMAINXTAL	VCCMAINXTAL	VCCMAINXTAL
P13	GNDLPXTAL	GNDLPXTAL	GNDLPXTAL
P14	VDDBAT	VDDBAT	VDDBAT
P15	PTEM	PTEM	PTEM
P16	PTBASE	PTBASE	PTBASE
R1	PCAP	PCAP	PCAP
R2	SDD0	SDD0	SDD0
R3	ADC0	ABPS0	ABPS0
R4	ADC3	TM0	TM0
R5	NC	ABPS2	ABPS2
R6	NC	ADC1	ADC1
R7	NC	VCC33ADC0	VCC33ADC0
R8	VCC15ADC0	VCC15ADC1	VCC15ADC1
R9	ADC10	ADC7	ADC7
R10	ABPS1	ABPS7	ABPS7
R11	NC	ABPS4	ABPS4
R12	MAINXIN	MAINXIN	MAINXIN
R13	MAINXOUT	MAINXOUT	MAINXOUT
R14	LPXIN	LPXIN	LPXIN
R15	LPXOUT	LPXOUT	LPXOUT
R16	VCC33A	VCC33A	VCC33A
T1	NCAP	NCAP	NCAP
T2	ADC1	ABPS1	ABPS1
T3	ADC2	CM0	CM0
T4	NC	GNDTM0	GNDTM0
T5	NC	ADC0	ADC0
T6	NC	VAREF0	VAREF0
T7	NC	GND33ADC0	GND33ADC0
T8	GND15ADC0	GND15ADC1	GND15ADC1

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
B3	NC	NC
B4	NC	NC
B5	VCCFPGAIOB0	VCCFPGAIOB0
B6	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
B7	NC	IO04PPB0V0
B8	VCCFPGAIOB0	VCCFPGAIOB0
B9	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
B10	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B11	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
B12	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
B13	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
B14	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
B15	VCCFPGAIOB0	VCCFPGAIOB0
B16	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B17	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
B18	VCCFPGAIOB0	VCCFPGAIOB0
B19	GBB0/IO18NDB0V0	GBB0/IO24NDB0V0
B20	GBB1/IO18PDB0V0	GBB1/IO24PDB0V0
B21	GND	GND
B22	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
C1	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	NC	NC
C3	NC	NC
C4	NC	IO01NDB0V0
C5	NC	IO01PDB0V0
C6	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
C7	NC	IO03PPB0V0
C8	NC	IO04NPB0V0
C9	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
C10	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
C11	GND	GND
C12	VCCFPGAIOB0	VCCFPGAIOB0
C13	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C14	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Revision	Changes	Page
Revision 10 (continued)	Corrected the Start-up time unit from "ms" to "μs" in Table 2-99 • Voltage Regulator (SAR 39395).	2-87
	Added the "References" section for "SmartFusion Development Tools" (SAR 43460).	3-1
	Updated the "References" section for Programming (SAR 43304). Added the "Application Notes on IAP Programming Technique" section (SAR 43458).	4-9
	A note was added to the "Supply Pins" table, referring to the SmartFusion cSoC Board Design Guidelines application note for details on VCCPLLx capacitor recommendations (SAR 42183).	5-1
	In the "Supply Pins" section , the VPP capacitor value section has been modified to: "For proper programming, 0.01μF, and 0.1μF to 1μF capacitors, (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible." (SAR 43569).	5-1
	In the "User-Defined Supply Pins" section , added description 'These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices.' for GPIO_x (SAR 28595).	5-5
	Updated the MAINXIN and MAINXOUT pin descriptions in the "Special Function Pins" section to read "If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating." (SAR 42807).	5-8
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 9 (September 2012)	The number of signal conditioning blocks (SCBs) for A2F500 in the "SmartFusion cSoC Family Product Table" was corrected to 4. Previously it had incorrectly been listed as 2 (SAR 39536).	II
	The "Product Ordering Codes" section was revised to clarify that only one eNVM size for each device is currently available (SAR 40333).	VI
	Information pertaining to analog I/Os was added to the "Specifying I/O States During Programming" section on page 1-3 (SAR 34836).	1-3
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34757).	2-27
	Maximum values for VIL and VIH were corrected in LVPECL Table 2-66 • Minimum and Maximum DC Input and Output Levels (SAR 37695).	2-43
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section . The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 29270).	2-59
	The temperature range for accuracy in Table 2-83 • Electrical Characteristics of the RC Oscillator was changed from "0°C to 85°C" to "-40°C to 100°C" (SAR 33670). The units for jitter were changed from ps to ps RMS (SAR 34270).	2-61
	In Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator , the output jitter for the 10 MHz crystal was corrected from 50 ps RMS to 1 ns RS (SAR 32939). Values for the startup time of VILXTAL were added (SAR 25248).	2-62
	In Table 2-85 • Electrical Characteristics of the Low Power Oscillator , output jitter was changed from 50 ps RMS to 30 ps RMS (SAR 32939). A value for ISTBXTAL standby current was added (SAR 25249). Startup time for a test load of 30 pF was added (SAR 27436).	2-62

Revision	Changes	Page
Revision 6 (continued)	Dynamic power values were updated in the following tables. The table subtitles changed where FPGA I/O banks were involved to note "I/O assigned to EMC I/O pins" (SAR 30987).	2-10
	Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings	2-11
	Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings.	
	The "Timing Model" was updated (SAR 30986).	2-19
	Values in the timing tables for the following sections were updated. Table subtitles were updated for FPGA I/O banks to note "I/O assigned to EMC I/O pins" (SAR 30986).	
	"Overview of I/O Performance" section: Table 2-24, Table 2-25	2-23
	"Detailed I/O DC Characteristics" section: Table 2-38, Table 2-39, Table 2-40, Table 2-44, Table 2-45, Table 2-46, Table 2-50, Table 2-51, Table 2-52, Table 2-56, Table 2-57, Table 2-58, Table 2-61, Table 2-62	2-26
	"LVDS" section: Table 2-65	2-40
"LVPECL" section: Table 2-68	2-42	
"Global Tree Timing Characteristics" section: Table 2-80, Table 2-81	2-59	
The "PQ208" section and pin tables are new (SAR 31005).	5-34	
Global clocks were removed from the A2F060 pin table for the "CS288" and "FG256" packages, resulting in changed function names for affected pins (SAR 31033).	5-43	
Revision 5 (December 2010)	Table 2-2 • Analog Maximum Ratings was revised. The recommended CM[n] pad voltage (relative to ground) was changed from –11 to –0.3 (SAR 28219).	2-2
	Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays was revised to change the values for 100°C.	2-9
	Power-down and Sleep modes, and all associated notes, were removed from Table 2-8 • Power Supplies Configuration (SAR 29479). IDC3 and IDC4 were renamed to IDC1 and IDC2 (SAR 29478). These modes are no longer supported. A note was added to the table stating that current monitors and temperature monitors should not be used when Power-down and/or Sleep mode are required by the application.	2-10
	The "Power-Down and Sleep Mode Implementation" section was deleted (SAR 29479).	N/A
	Values for PAC9 and PAC10 for LVDS and LVPECL were revised in Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings*.	2-10, 2-11
	Values for PAC1 through PAC4, PDC1, and PDC2 were added for A2F500 in Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs	2-12, 2-13
	The equation for "Total Dynamic Power Consumption— P_{DYN} " in "SoC Mode" was revised to add P_{MSS} . The "Microcontroller Subsystem Dynamic Contribution— P_{MSS} " section is new (SAR 29462).	2-14, 2-18
Information in Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to FPGA I/O banks) and Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to MSS I/O banks) was updated.	2-25	

Revision	Changes	Page
Revision 3 (continued)	<p>In Table 2-3 • Recommended Operating Conditions^{5,6}, the VDDBAT recommended operating range was changed from "2.97 to 3.63" to "2.7 to 3.63" (SAR 25246). Recommended operating range was changed to "3.15 to 3.45" for the following voltages:</p> <ul style="list-style-type: none"> VCC33A VCC33ADCx VCC33AP VCC33SDDx VCCMAINXTAL VCCLPXTAL <p>Two notes were added to the table (SAR 27109):</p> <ol style="list-style-type: none"> 1. <i>The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.</i> 2. <i>The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.</i> 	2-3
	<p>In Table 2-3 • Recommended Operating Conditions^{5,6}, the description for VCCLPXTAL was corrected to change "32 Hz" to "32 KHz" (SAR 27110).</p>	2-3
	<p>The "Power Supply Sequencing Requirement" section is new (SAR 27178).</p>	2-4
	<p>Table 2-8 • Power Supplies Configuration was revised to change most on/off entries to voltages. Note 5 was added, stating that "on" means proper voltage is applied. The values of 6 μA and 16 μA were removed for IDC1 and IDC2 for 3.3 V. A note was added for IDC1 and IDC2: "Power mode and Sleep mode are consuming higher current than expected in the current version of silicon. These specifications will be updated when new version of the silicon is available" (SAR 27926).</p>	2-10
	<p>The "Power-Down and Sleep Mode Implementation" section is new (SAR 27178).</p>	2-11
	<p>A note was added to Table 2-86 • SmartFusion CCC/PLL Specification, pertaining to f_{out_CCC}, stating that "one of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software" (SAR 26388).</p>	2-63
	<p>Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: $T_J = 85^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$ was revised. Values were included for A2F200 and A2F500, for –1 and Std. speed grades. A note was added to define 6:1:1:1 and 5:1:1:1 (SAR 26166).</p>	2-76
	<p>The units were corrected (mV instead of V) for input referred offset voltage, $GDEC[1:0] = 00$ in Table 2-96 • ABPS Performance Specifications (SAR 25381).</p>	2-82
	<p>The test condition values for operating current (ICC33A, typical) were changed in Table 2-99 • Voltage Regulator (SAR 26465).</p>	2-87
	<p>Figure 2-45 • Typical Output Voltage was revised to add legends for the three curves, stating the load represented by each (SAR 25247).</p>	2-88
	<p>The "SmartFusion Programming" chapter was moved to this document from the SmartFusion Subsystem Microcontroller User's Guide (SAR 26542). The "Typical Programming and Erase Times" section was added to this chapter.</p>	4-7
	<p>Figure 4-1 • TRSTB Logic was revised to change 1.5 V to "VJTAG (1.5 V to 3.3 V nominal)" (SAR 24694).</p>	4-8