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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

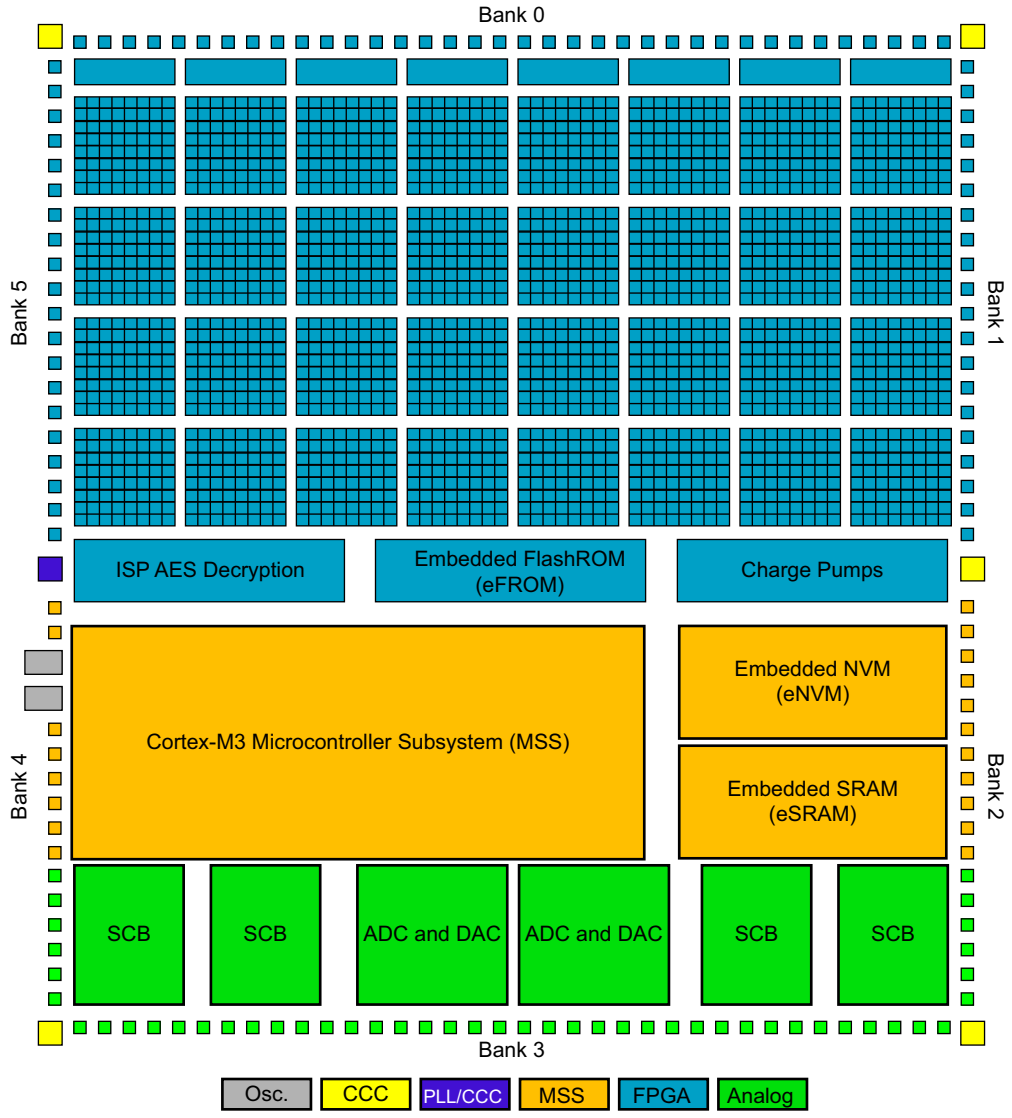
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1csg288

SmartFusion cSoC System Architecture



Note: Architecture for A2F200

Table 2-63 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}[1]	Output lower current	0.65	0.91	1.16	mA
I_{OH}[1]	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}[2]	Input high leakage current			15	µA
I_{IL}[2]	Input low leakage current			15	µA
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. *I_{OL}/I_{OH} defined by V_{ODIFF}/(resistor network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-65 • LVDS
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.83	0.04	1.87	ns
–1	0.50	1.53	0.03	1.55	ns

Notes:

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. SoC Products Group LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using SoC Products Group LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-12. The input and output buffer delays are available in the LVDS section in Table 2-65.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case commercial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

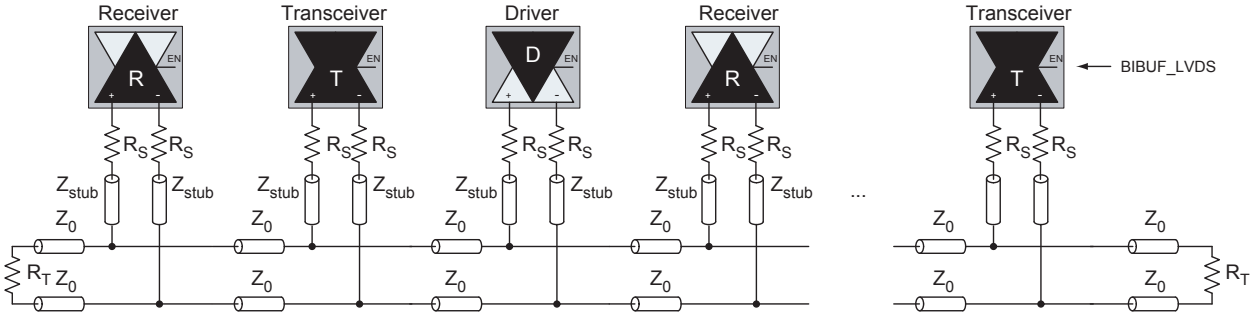


Figure 2-12 • **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-13. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

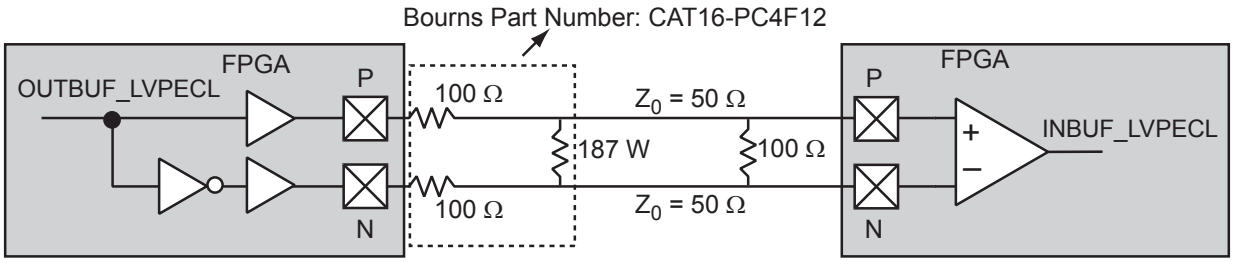


Figure 2-13 • **LVPECL Circuit Diagram and Board-Level Implementation**

***Table 2-69* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-14 on page 2-44 for more information.*

Input Register

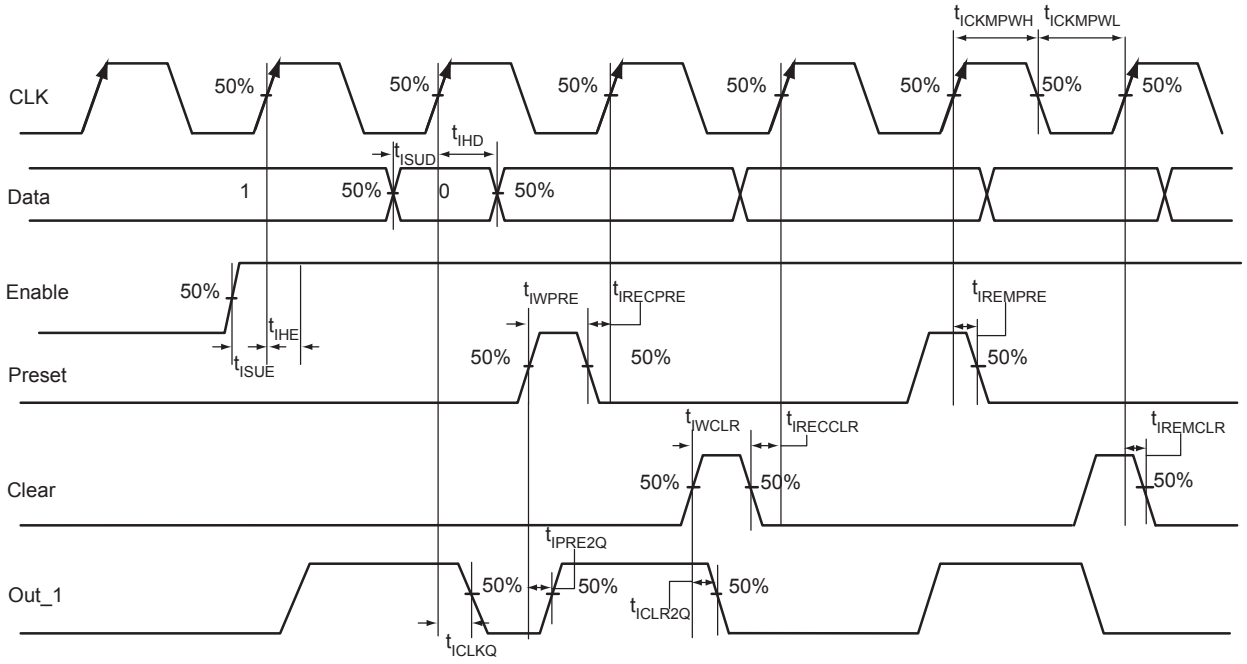


Figure 2-16 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-71 • **Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.55	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.55	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

DDR Module Specifications

Input DDR Module

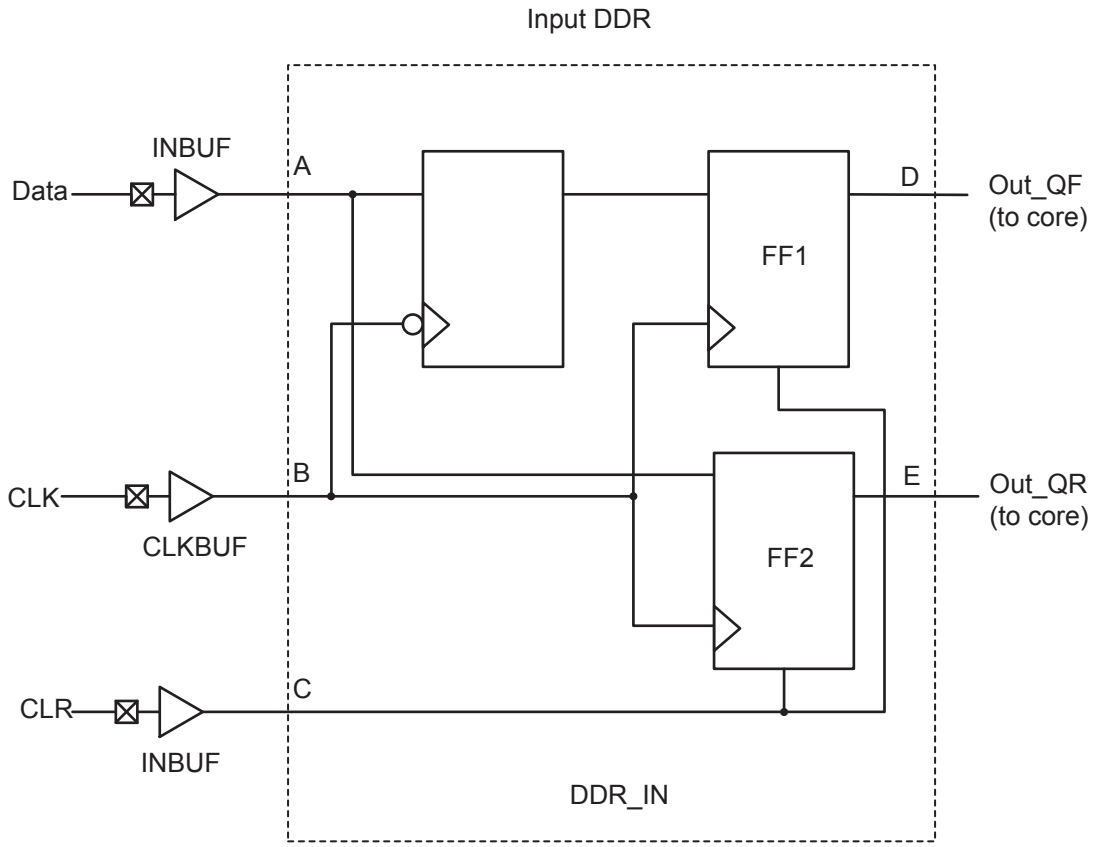


Figure 2-19 • **Input DDR Timing Model**

Table 2-74 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

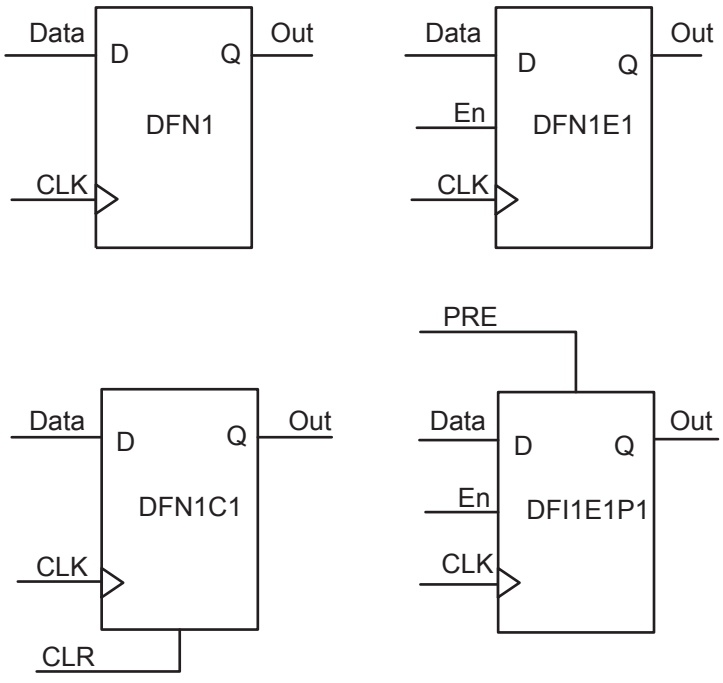


Figure 2-25 • Sample of Sequential Cells

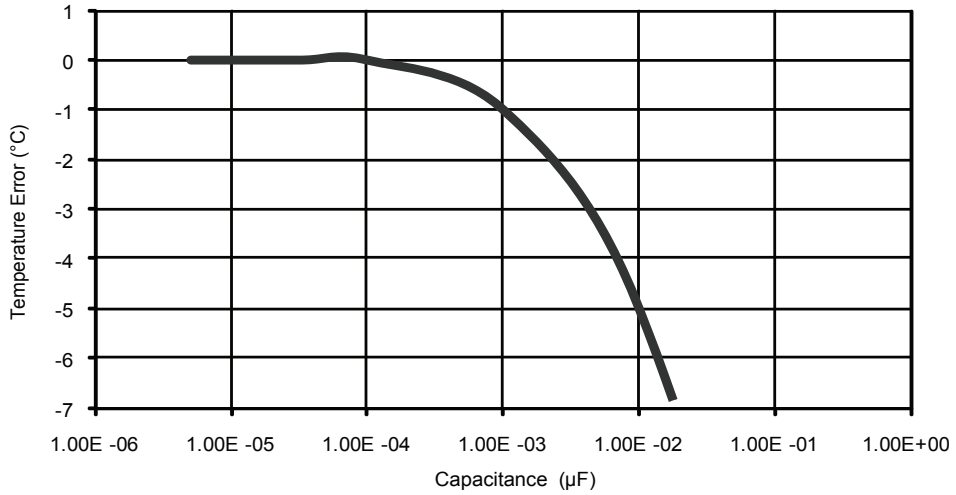


Figure 2-43 • **Temperature Error Versus External Capacitance**

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quite analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GNDA	Ground	Quiet analog ground to the analog front-end
GNDAQ	Ground	Quiet analog ground to the analog I/O of SmartFusion cSoCs
GNDENVM	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GNDLPXTAL	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GNDMAINXTAL	Ground	Analog ground to the main crystal oscillator circuitry
GNDQ	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND.
GNDRCOSC	Ground	Analog ground to the integrated RC oscillator circuit
GNDSDD0	Ground	Analog ground to the first sigma-delta DAC
GNDSDD1	Ground	Common analog ground to the second and third sigma-delta DACs
GNDTM0	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM1	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM2	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GNDVAREF	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Name	Type	Description
VCC15A	Supply	Clean analog 1.5 V supply to the analog circuitry. Always power this pin.
VCC15ADC0	Supply	Analog 1.5 V supply to the first ADC. Always power this pin.
VCC15ADC1	Supply	Analog 1.5 V supply to the second ADC. Always power this pin.
VCC15ADC2	Supply	Analog 1.5 V supply to the third ADC. Always power this pin.
VCC33A	Supply	Clean 3.3 V analog supply to the analog circuitry. VCC33A is also used to feed the 1.5 V voltage regulator for designs that do not provide an external supply to VCC. Refer to the Voltage Regulator (VR), Power Supply Monitor (PSM), and Power Modes section in the *SmartFusion Microcontroller Subsystem User's Guide* for more information.
VCC33ADC0	Supply	Analog 3.3 V supply to the first ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33ADC1	Supply	Analog 3.3 V supply to the second ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33ADC2	Supply	Analog 3.3 V supply to the third ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33AP	Supply	Analog clean 3.3 V supply to the charge pump. To avoid high current draw, VCC33AP should be powered up simultaneously with or after VCC33A. Can be pulled down if unused.[1]
VCC33N	Supply	–3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to GND. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
VCC33SDD0	Supply	Analog 3.3 V supply to the first sigma-delta DAC
VCC33SDD1	Supply	Common analog 3.3 V supply to the second and third sigma-delta DACs
VCCENVM	Supply	Digital 1.5 V power supply to the embedded nonvolatile memory blocks. To avoid high current draw, VCC should be powered up before or simultaneously with VCCENVM.
VCCESRAM	Supply	Digital 1.5 V power supply to the embedded SRAM blocks. Available only on the 208PQFP package. It should be connected to VCC (in other packages, it is internally connected to VCC).
VCCFPGAIOB0	Supply	Digital supply to the FPGA fabric I/O bank 0 (north FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB1	Supply	Digital supply to the FPGA fabric I/O bank 1 (east FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Analog Front-End (AFE)

Name	Type	Description	Associated With	
			ADC/SDD	SCB
ABPS0	In	SCB 0 / active bipolar prescaler input 1. See the Active Bipolar Prescaler (ABPS) section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ABPS1	In	SCB 0 / active bipolar prescaler Input 2	ADC0	SCB0
ABPS2	In	SCB 1 / active bipolar prescaler Input 1	ADC0	SCB1
ABPS3	In	SCB 1 / active bipolar prescaler Input 2	ADC0	SCB1
ABPS4	In	SCB 2 / active bipolar prescaler Input 1	ADC1	SCB2
ABPS5	In	SCB 2 / active bipolar prescaler Input 2	ADC1	SCB2
ABPS6	In	SCB 3 / active bipolar prescaler Input 1	ADC1	SCB3
ABPS7	In	SCB 3 / active bipolar prescaler input 2	ADC1	SCB3
ABPS8	In	SCB 4 / active bipolar prescaler input 1	ADC2	SCB4
ABPS9	In	SCB 4 / active bipolar prescaler input 2	ADC2	SCB4
ADC0	In	ADC 0 direct input 0 / FPGA Input. See the "Sigma-Delta Digital-to-Analog Converter (DAC)" section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ADC1	In	ADC 0 direct input 1 / FPGA input	ADC0	SCB0
ADC2	In	ADC 0 direct input 2 / FPGA input	ADC0	SCB1
ADC3	In	ADC 0 direct input 3 / FPGA input	ADC0	SCB1
ADC4	In	ADC 1 direct input 0 / FPGA input	ADC1	SCB2
ADC5	In	ADC 1 direct input 1 / FPGA input	ADC1	SCB2
ADC6	In	ADC 1 direct input 2 / FPGA input	ADC1	SCB3
ADC7	In	ADC 1 direct input 3 / FPGA input	ADC1	SCB3
ADC8	In	ADC 2 direct input 0 / FPGA input	ADC2	SCB4
ADC9	In	ADC 2 direct input 1 / FPGA input	ADC2	SCB4
ADC10	In	ADC 2 direct input 2 / FPGA input	ADC2	N/A
ADC11	In	ADC 2 direct input 3 / FPGA input	ADC2	N/A
CM0	In	SCB 0 / high side of current monitor / comparator Positive input. See the Current Monitor section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
CM1	In	SCB 1 / high side of current monitor / comparator. Positive input.	ADC0	SCB1
CM2	In	SCB 2 / high side of current monitor / comparator. Positive input.	ADC1	SCB2
CM3	In	SCB 3 / high side of current monitor / comparator. Positive input.	ADC1	SCB3
CM4	In	SCB 4 / high side of current monitor / comparator. Positive input.	ADC2	SCB4

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the *SmartFusion Programmable Analog User's Guide*.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

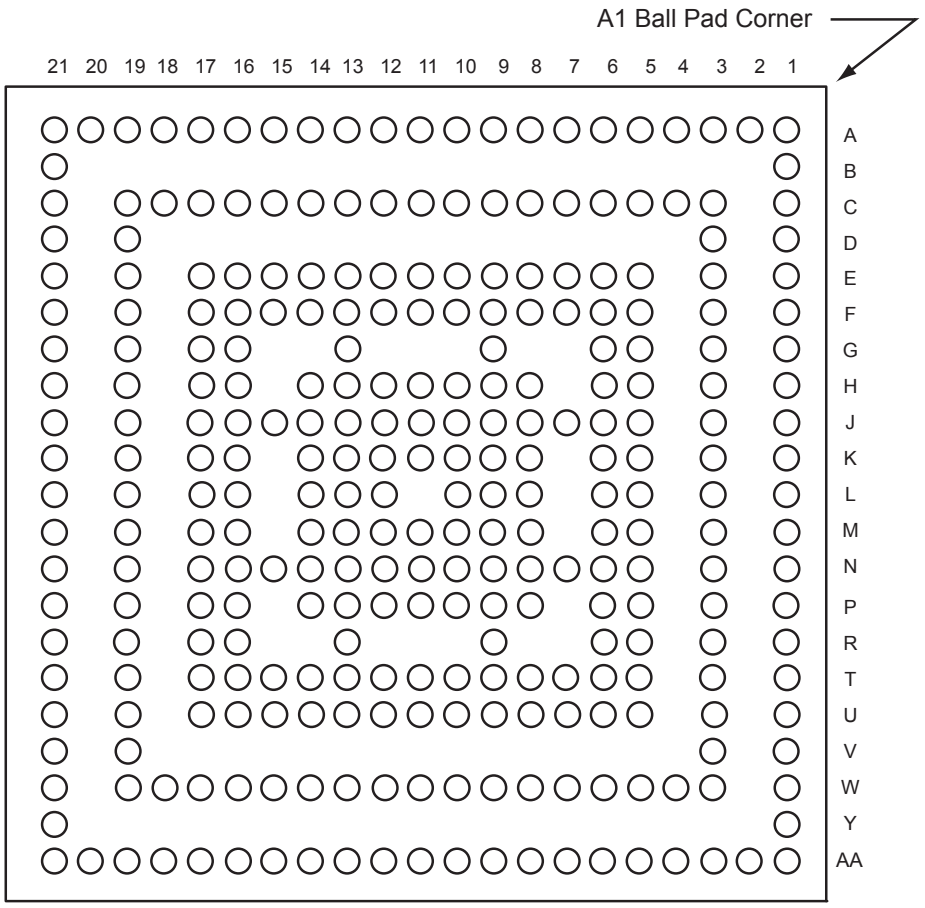
Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

TQ144	
Pin Number	**A2F060 Function**
109	VPP
110	GNDQ
111	GCA1/IO20PDB0V0
112	GCA0/IO20NDB0V0
113	GCB1/IO19PDB0V0
114	GCB0/IO19NDB0V0
115	GCC1/IO18PDB0V0
116	GCC0/IO18NDB0V0
117	VCCFPGAIOB0
118	GND
119	VCC
120	IO14PDB0V0
121	IO14NDB0V0
122	IO13NSB0V0
123	IO11PDB0V0
124	IO11NDB0V0
125	IO09PDB0V0
126	IO09NDB0V0
127	VCCFPGAIOB0
128	GND
129	IO07PDB0V0
130	IO07NDB0V0
131	IO06PDB0V0
132	IO06NDB0V0
133	IO05PDB0V0
134	IO05NDB0V0
135	IO03PDB0V0
136	IO03NDB0V0
137	VCCFPGAIOB0
138	GND
139	VCC
140	IO01PDB0V0
141	IO01NDB0V0
142	IO00PDB0V0
143	IO00NDB0V0
144	GNDQ

CS288

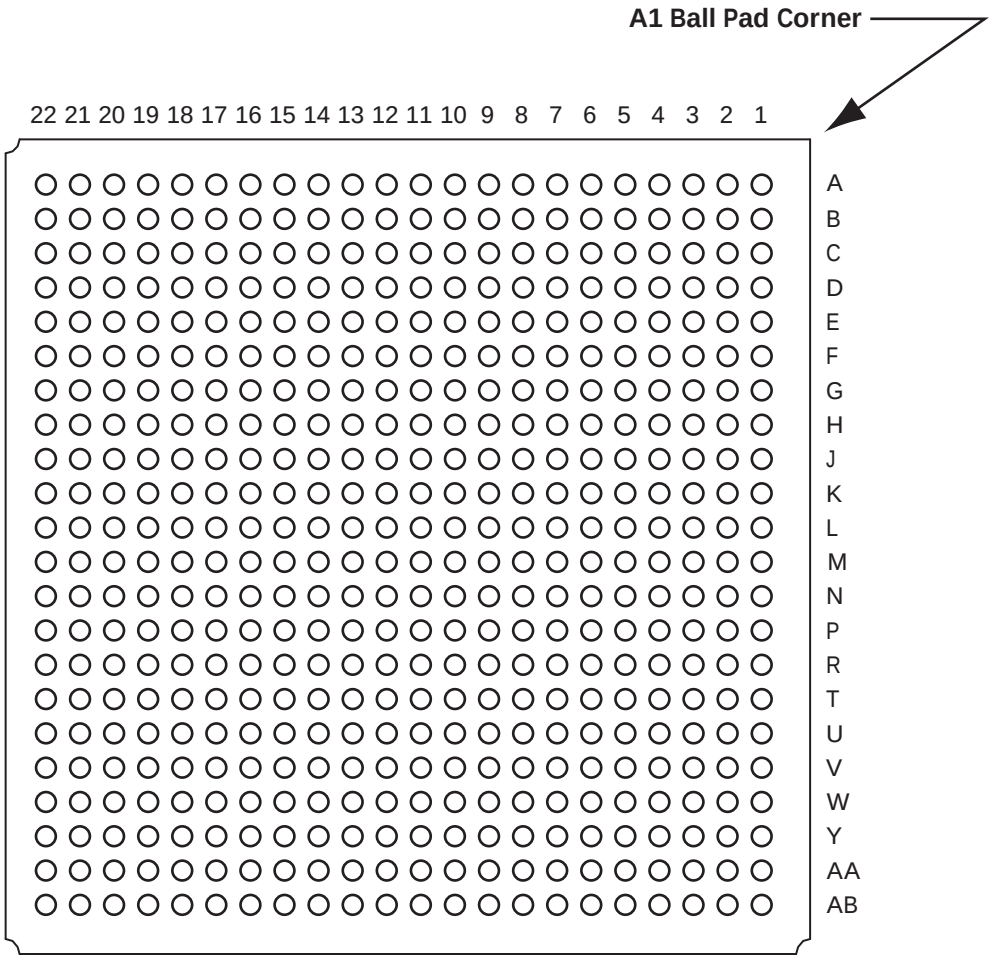


Note: Bottom view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
A1	GND	GND
A2	NC	NC
A3	NC	NC
A4	GND	GND
A5	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
A6	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
A7	GND	GND
A8	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A9	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A10	GND	GND
A11	NC	NC
A12	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
A13	GND	GND
A14	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
A15	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
A16	GND	GND
A17	NC	IO16NDB0V0
A18	NC	IO16PDB0V0
A19	GND	GND
A20	NC	NC
A21	NC	NC
A22	GND	GND
AA1	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
AA2	GPIO_12/IO37RSB4V0	GPIO_12/IO46RSB4V0
AA3	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
AA4	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
AA5	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
AA6	ABPS0	ABPS0
AA7	TM1	TM1
AA8	ADC1	ADC1
AA9	GND15ADC1	GND15ADC1
AA10	GND33ADC1	GND33ADC1
AA11	CM3	CM3
AA12	GNDTM1	GNDTM1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 3 (continued)	In Table 2-3 • Recommended Operating Conditions[5,6], the VDDBAT recommended operating range was changed from "2.97 to 3.63" to "2.7 to 3.63" (SAR 25246). Recommended operating range was changed to "3.15 to 3.45" for the following voltages: VCC33A VCC33ADCx VCC33AP VCC33SDDx VCCMAINXTAL VCCLPXTAL Two notes were added to the table (SAR 27109): 1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* 2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	2-3
	In Table 2-3 • Recommended Operating Conditions[5,6], the description for VCCLPXTAL was corrected to change "32 Hz" to "32 KHz" (SAR 27110).	2-3
	The "Power Supply Sequencing Requirement" section is new (SAR 27178).	2-4
	Table 2-8 • Power Supplies Configuration was revised to change most on/off entries to voltages. Note 5 was added, stating that "on" means proper voltage is applied. The values of 6 µA and 16 µA were removed for IDC1 and IDC2 for 3.3 V. A note was added for IDC1 and IDC2: "Power mode and Sleep mode are consuming higher current than expected in the current version of silicon. These specifications will be updated when new version of the silicon is available" (SAR 27926).	2-10
	The "Power-Down and Sleep Mode Implementation" section is new (SAR 27178).	2-11
	A note was added to Table 2-86 • SmartFusion CCC/PLL Specification, pertaining to f_{out_CCC}, stating that "one of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software" (SAR 26388).	2-63
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised. Values were included for A2F200 and A2F500, for –1 and Std. speed grades. A note was added to define 6:1:1:1 and 5:1:1:1 (SAR 26166).	2-76
	The units were corrected (mV instead of V) for input referred offset voltage, GDEC[1:0] = 00 in Table 2-96 • ABPS Performance Specifications (SAR 25381).	2-82
	The test condition values for operating current (ICC33A, typical) were changed in Table 2-99 • Voltage Regulator (SAR 26465).	2-87
	Figure 2-45 • Typical Output Voltage was revised to add legends for the three curves, stating the load represented by each (SAR 25247).	2-88
	The "SmartFusion Programming" chapter was moved to this document from the SmartFusion Subsystem Microcontroller User's Guide (SAR 26542). The "Typical Programming and Erase Times" section was added to this chapter.	4-7
	Figure 4-1 • TRSTB Logic was revised to change 1.5 V to "VJTAG (1.5 V to 3.3 V nominal)" (SAR 24694).	4-8