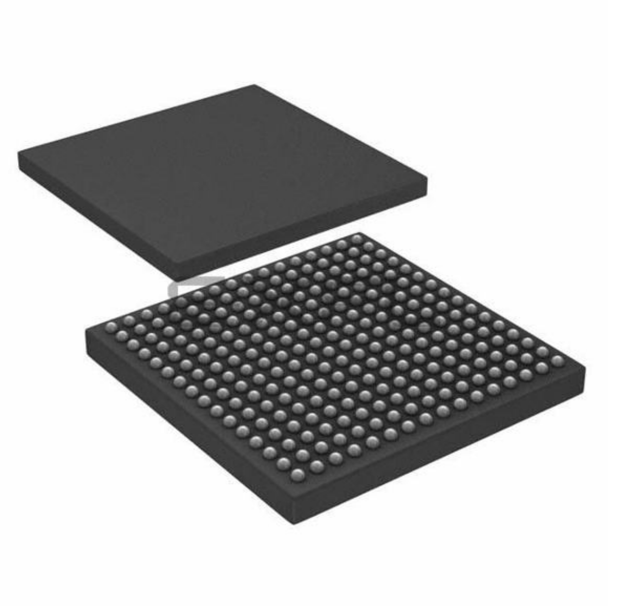
Microchip Technology - A2F200M3F-1FG256I Datasheet



Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

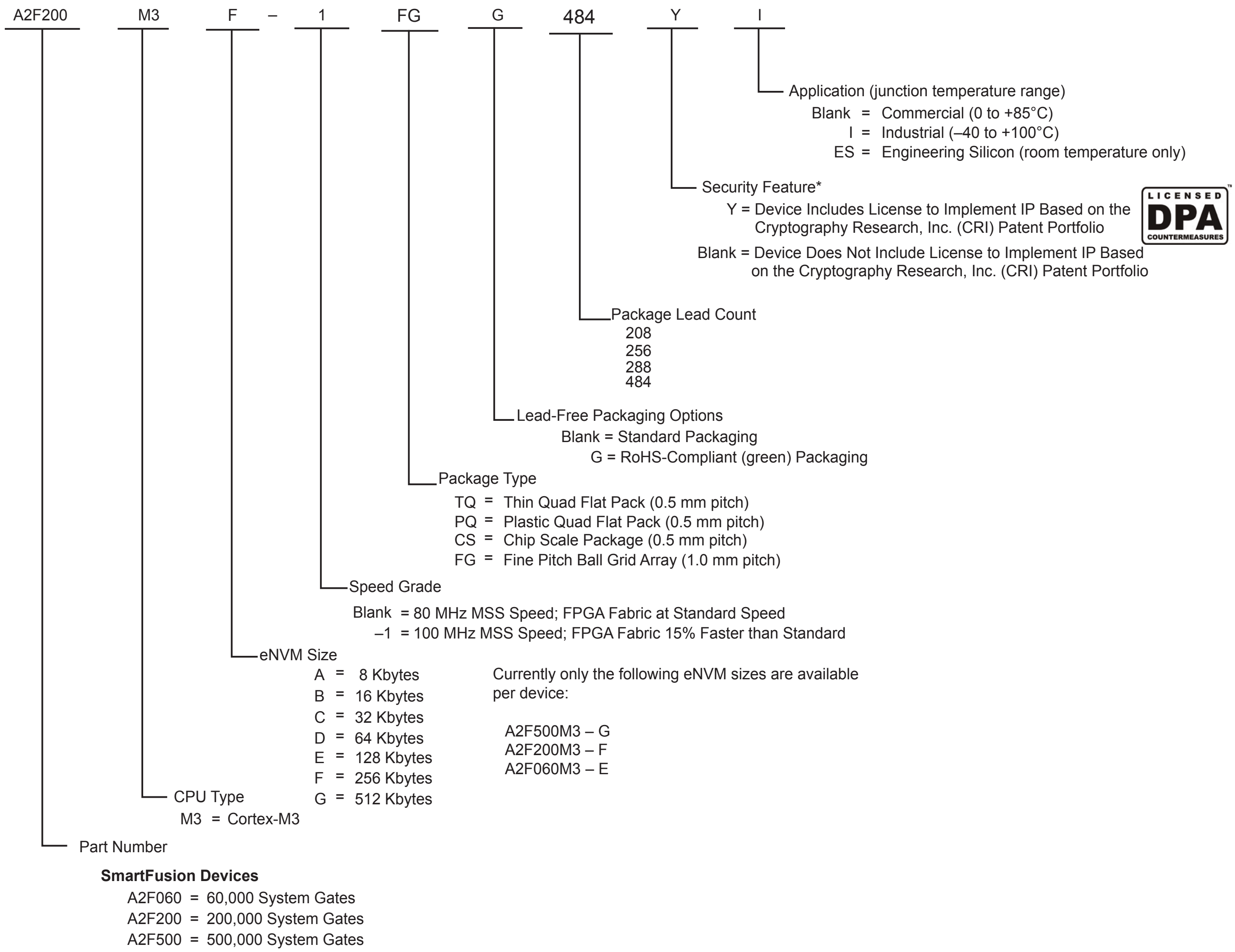
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1fg256i

Product Ordering Codes



A2F200 M3 F – 1 FG G 484 Y I

Application (junction temperature range)
Blank = Commercial (0 to +85°C)
I = Industrial (–40 to +100°C)
ES = Engineering Silicon (room temperature only)

Security Feature*
Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Package Lead Count
208
256
288
484

Lead-Free Packaging Options
Blank = Standard Packaging
G = RoHS-Compliant (green) Packaging

Package Type
TQ = Thin Quad Flat Pack (0.5 mm pitch)
PQ = Plastic Quad Flat Pack (0.5 mm pitch)
CS = Chip Scale Package (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)

Speed Grade
Blank = 80 MHz MSS Speed; FPGA Fabric at Standard Speed
–1 = 100 MHz MSS Speed; FPGA Fabric 15% Faster than Standard

eNVM Size
A = 8 Kbytes
B = 16 Kbytes
C = 32 Kbytes
D = 64 Kbytes
E = 128 Kbytes
F = 256 Kbytes
G = 512 Kbytes

Currently only the following eNVM sizes are available per device:

A2F500M3 – G
A2F200M3 – F
A2F060M3 – E

CPU Type
M3 = Cortex-M3

Part Number

SmartFusion Devices
A2F060 = 60,000 System Gates
A2F200 = 200,000 System Gates
A2F500 = 500,000 System Gates

Note: **Most devices in the SmartFusion cSoC family can be ordered with the Y suffix. Devices with a package size greater or equal to 5x5 mm are supported. Contact your local Microsemi SoC Products Group sales representative for more information.*

Temperature Grade Offerings

SmartFusion cSoC	A2F060	A2F200	A2F500
TQ144	C, I	–	–
PQ208	–	C, I	C, I
CS288	C, I	C, I	C, I
FG256	C, I	C, I	C, I
FG484	–	C, I	C, I

Notes:
1. *C = Commercial Temperature Range: 0°C to 85°C Junction*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction*

This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

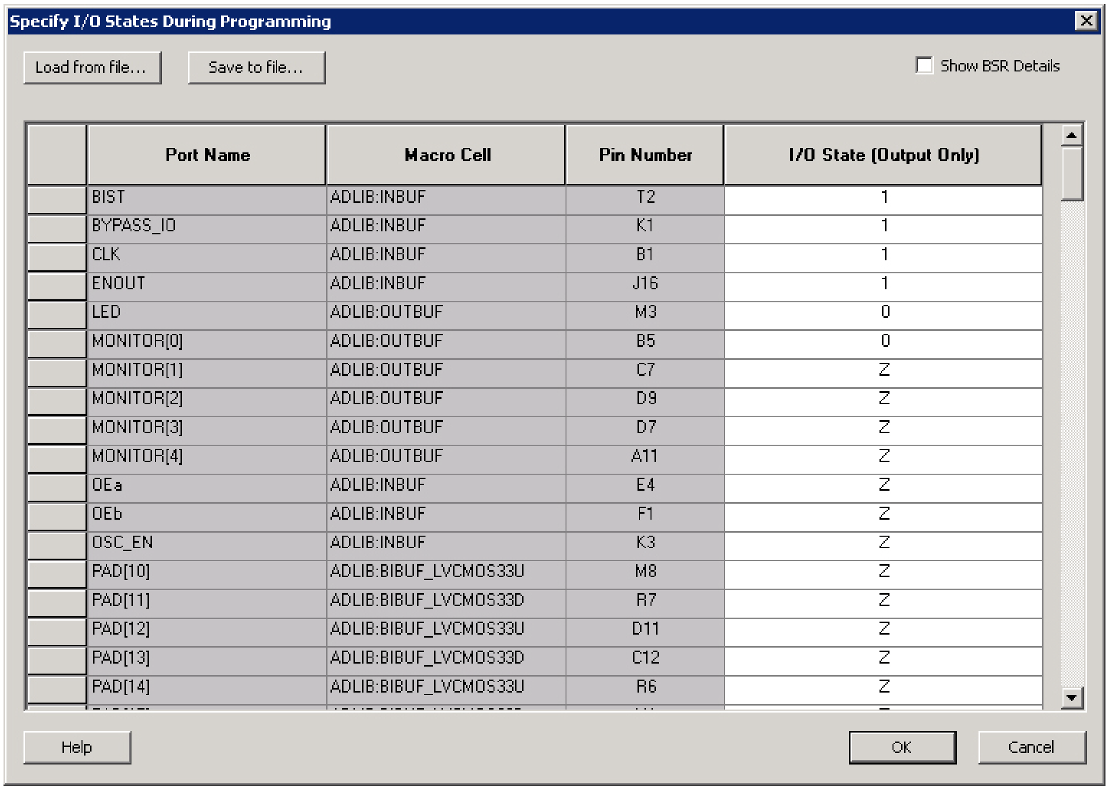
1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated



Port Name	Macro Cell	Pin Number	I/O State (Output Only)
BIST	ADLIB:INBUF	T2	1
BYPASS_IO	ADLIB:INBUF	K1	1
CLK	ADLIB:INBUF	B1	1
ENOUT	ADLIB:INBUF	J16	1
LED	ADLIB:OUTBUF	M3	0
MONITOR[0]	ADLIB:OUTBUF	B5	0
MONITOR[1]	ADLIB:OUTBUF	C7	Z
MONITOR[2]	ADLIB:OUTBUF	D9	Z
MONITOR[3]	ADLIB:OUTBUF	D7	Z
MONITOR[4]	ADLIB:OUTBUF	A11	Z
OEa	ADLIB:INBUF	E4	Z
OEb	ADLIB:INBUF	F1	Z
OSC_EN	ADLIB:INBUF	K3	Z
PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

Figure 1-1 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

***Table 2-7 •* Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 85°C, worst-case VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.86	0.91	0.93	0.98	1.00	1.02
1.500	0.81	0.86	0.88	0.93	0.95	0.96
1.575	0.78	0.83	0.85	0.90	0.91	0.93

Table 2-14 • **Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03			mW
PAC25	ABPS Power Contribution	See Table 2-96 on page 2-82	–	0.70			mW
PAC26	Sigma-Delta DAC Power Contribution[2]	See Table 2-98 on page 2-85	–	0.58			mW
PAC27	Comparator Power Contribution	See Table 2-97 on page 2-84	–	1.02			mW
PAC28	Voltage Regulator Power Contribution[3]	See Table 2-99 on page 2-87	–	36.30			mW

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Assumes Input = Half Scale Operation mode.*
3. *Assumes 100 mA load on 1.5 V domain.*

Table 2-15 • **Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F200	
PDC1	Core static power contribution in SoC mode	VCC	1.5 V	11.10	23.70	37.95	mW
PDC2	Device static power contribution in Standby Mode	See Table 2-8 on page 2-10	–	11.10	23.70	37.95	mW
PDC3	Device static power contribution in Time Keeping mode	See Table 2-8 on page 2-10	3.3 V	33.00	33.00	33.00	µW
PDC7	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11.				
PDC8	Static contribution per output pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11.				
PDC9	Static contribution per PLL	VCC	1.5 V	2.55	2.55	2.55	mW

Table 2-16 • **eNVM Dynamic Power Consumption**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
eNVM System	eNVM array operating power	Idle		795		µA
		Read operation	See Table 2-14 on page 2-12.			
		Erase		900		µA
		Write		900		µA
PNVMCTRL	eNVM controller operating power			20		µW/MHz

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

***Table 2-35* • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	**VIL**		**VIH**		**VOL**	**VOH**	**I_{OL}**	**I_{OH}**	**I_{OSL}**	**I_{OSH}**	**I_{IL}**	**I_{IH}**
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA^1**	**Max. mA^1**	**µA^2**	**µA^2**
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

***Table 2-36* • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	**VIL**		**VIH**		**VOL**	**VOH**	**I_{OL}**	**I_{OH}**	**I_{OSL}**	**I_{OSH}**	**I_{IL}**	**I_{IH}**
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA^1**	**Max. mA^1**	**µA^2**	**µA^2**
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

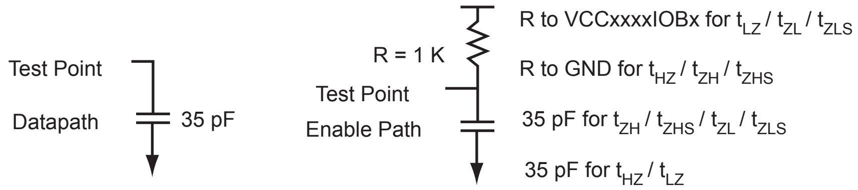


***Figure 2-6* • AC Loading**

***Table 2-37* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**V_{REF} (typ.) (V)**	**C_{LOAD} (pF)**
0	3.3	1.4	–	35

Note: **Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-50 • 1.8 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.06	0.04	1.14	0.39	8.61	11.06	2.61	1.59	10.67	13.12	ns
	–1	0.50	9.22	0.03	0.95	0.32	7.17	9.22	2.18	1.33	8.89	10.93	ns
4 mA	Std.	0.60	6.46	0.04	1.14	0.39	5.53	6.46	3.04	2.66	7.59	8.51	ns
	–1	0.50	5.38	0.03	0.95	0.32	4.61	5.38	2.54	2.22	6.33	7.10	ns
6 mA	Std.	0.60	4.16	0.04	1.14	0.39	3.99	4.16	3.34	3.18	6.05	6.22	ns
	–1	0.50	3.47	0.03	0.95	0.32	3.32	3.47	2.78	2.65	5.04	5.18	ns
8 mA	Std.	0.60	3.69	0.04	1.14	0.39	3.76	3.67	3.40	3.31	5.81	5.73	ns
	–1	0.50	3.07	0.03	0.95	0.32	3.13	3.06	2.84	2.76	4.85	4.78	ns
12 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
16 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-51 • 1.8 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	14.24	0.04	1.14	0.39	13.47	14.24	2.62	1.54	15.53	16.30	ns
	–1	0.50	11.87	0.03	0.95	0.32	11.23	11.87	2.18	1.28	12.94	13.59	ns
4 mA	Std.	0.60	9.74	0.04	1.14	0.39	9.92	9.62	3.05	2.57	11.98	11.68	ns
	–1	0.50	8.11	0.03	0.95	0.32	8.26	8.02	2.54	2.14	9.98	9.74	ns
6 mA	Std.	0.60	7.67	0.04	1.14	0.39	7.81	7.24	3.34	3.08	9.87	9.30	ns
	–1	0.50	6.39	0.03	0.95	0.32	6.51	6.03	2.79	2.56	8.23	7.75	ns
8 mA	Std.	0.60	7.15	0.04	1.14	0.39	7.29	6.75	3.41	3.21	9.34	8.80	ns
	–1	0.50	5.96	0.03	0.95	0.32	6.07	5.62	2.84	2.68	7.79	7.34	ns
12 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns
16 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-56 • 1.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.425 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 m	Std.	0.60	7.79	0.04	1.34	0.39	6.43	7.79	3.19	2.59	8.49	9.85	ns
	–1	0.50	6.49	0.03	1.12	0.32	5.36	6.49	2.66	2.16	7.08	8.21	ns
4 mA	Std.	0.60	4.95	0.04	1.34	0.39	4.61	4.96	3.53	3.19	6.67	7.02	ns
	–1	0.50	4.13	0.03	1.12	0.32	3.85	4.13	2.94	2.66	5.56	5.85	ns
6 mA	Std.	0.60	4.36	0.04	1.34	0.39	4.34	4.36	3.60	3.34	6.40	6.42	ns
	–1	0.50	3.64	0.03	1.12	0.32	3.62	3.64	3.00	2.78	5.33	5.35	ns
8 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
12 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-57 • 1.5 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.96	0.04	1.34	0.39	12.18	11.70	3.20	2.47	14.24	13.76	ns
	–1	0.50	9.96	0.03	1.12	0.32	10.15	9.75	2.67	2.06	11.86	11.46	ns
4 mA	Std.	0.60	9.51	0.04	1.34	0.39	9.68	8.76	3.54	3.07	11.74	10.82	ns
	–1	0.50	7.92	0.03	1.12	0.32	8.07	7.30	2.95	2.56	9.79	9.02	ns
6 mA	Std.	0.60	8.86	0.04	1.34	0.39	9.03	8.17	3.61	3.22	11.08	10.23	ns
	–1	0.50	7.39	0.03	1.12	0.32	7.52	6.81	3.01	2.68	9.24	8.52	ns
8 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns
12 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-58 • 1.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.22	3.24	0.09	1.28	1.86	0.22	3.30	3.20	2.24	2.21	ns
	–1	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Timing Characteristics

Table 2-80 • A2F500 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.54	1.73	1.84	2.08	ns
t_{RCKH}	Input High Delay for Global Clock	1.53	1.76	1.84	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.23		0.28	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-81 • A2F200 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.74	0.99	0.88	1.19	ns
t_{RCKH}	Input High Delay for Global Clock	0.76	1.05	0.91	1.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.29		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

FPGA Fabric SRAM and FIFO Characteristics

FPGA Fabric SRAM

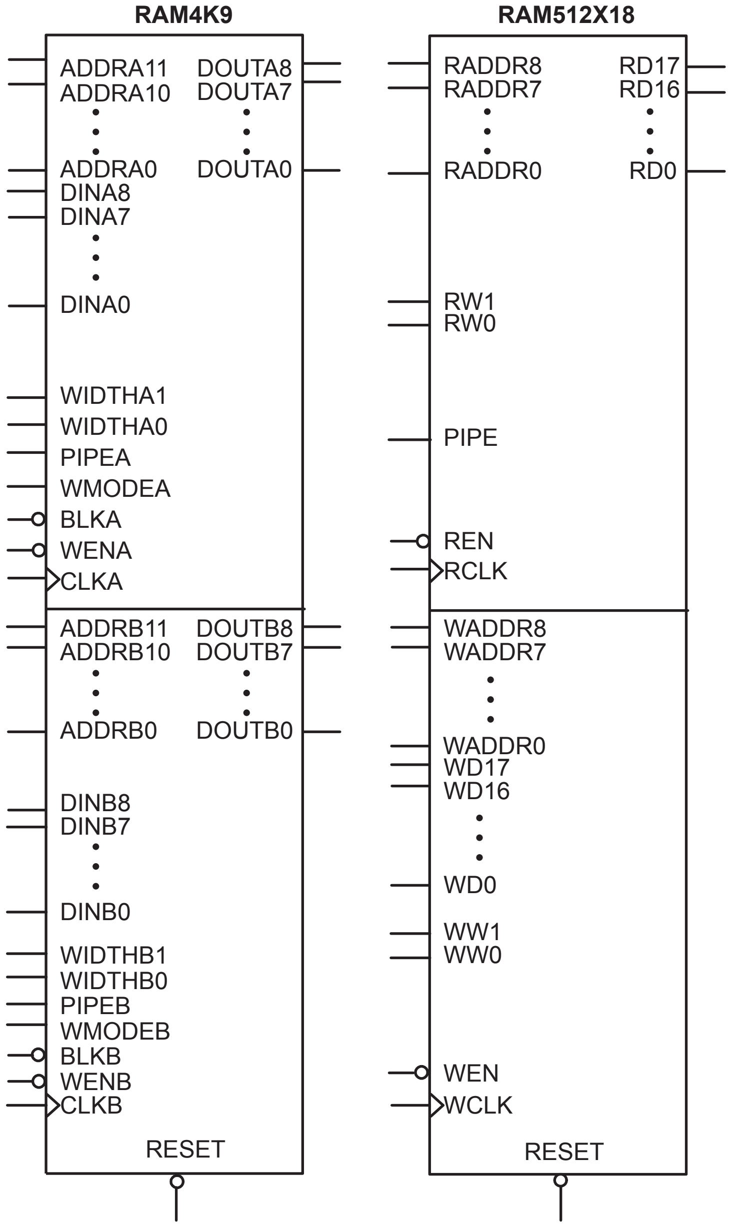


Figure 2-29 • **RAM Models**

***Table 2-88* • RAM512X18**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.22	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.19	2.63	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.91	1.09	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.38	0.43	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.44	0.50	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to data out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.22	ns
t_{CYC}	Clock cycle time	3.28	3.28	ns
F_{MAX}	Maximum clock frequency	305	305	MHz

Notes:

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

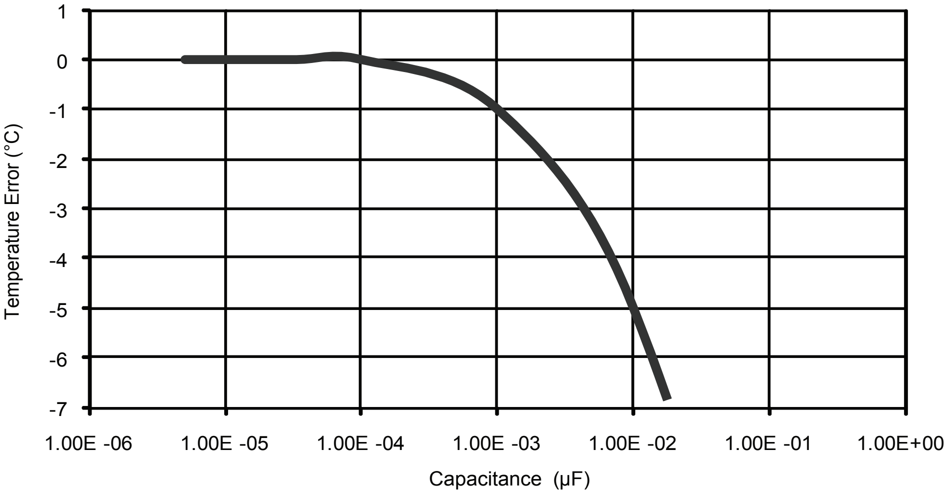


***Figure 2-43* • Temperature Error Versus External Capacitance**

Table 2-95 • **ADC Specifications (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: *All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.*

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-96 • **ABPS Performance Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%

Note: **FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-47 on page 2-90.

***Table 2-100* • SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp1	SPI_x_CLK minimum period				
	SPI_x_CLK = PCLK/2	20	NA	20	ns
	SPI_x_CLK = PCLK/4	40	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [1]	4.7	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [1]	3.4	3.4	3.4	ns

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

User-Defined Supply Pins

Name	Type	Polarity/ Bus Size	Description
VAREF0	Input	1	Analog reference voltage for first ADC. The SmartFusion cSoC can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the *SmartFusion Programmable Analog User's Guide* for more information. The SoC Products Group recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, the VAREFOUT pin must be connected to the appropriate ADC VAREFx input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1 and VAREF2 together, if ADC0, ADC1, and ADC2 all are used.
VAREF1	Input	1	Analog reference voltage for second ADC See "VAREF0" above for more information.
VAREF2	Input	1	Analog reference voltage for third ADC See "VAREF0" above for more.
VAREFOUT	Out	1	Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.

Pin No.	CS288		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
C21	IO17NDB0V0	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
D1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
D3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D19	GND	GND	GND
D21	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E3	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E5	GNDQ	GNDQ	GNDQ
E6	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
E7	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
E8	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
E9	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
E10	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
E11	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
E12	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
E13	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
E14	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
E15	GCC0/IO18NPB0V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
E16	GCA1/IO20PPB0V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E17	GCC1/IO18PPB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
E19	GCB2/IO22PPB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
E21	IO21NDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
F1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F5	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
F6	EMC_DB[11]/IO43PDB5V0	EMC_DB[11]/IO69PDB5V0	EMC_DB[11]/IO86PDB5V0
F7	GND	GND	GND
F8	NC	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
F9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
F10	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
F11	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

PQ208

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 5 (continued)	Available values for the Std. speed were added to the timing tables from Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew to Table 2-92 • JTAG 1532 (SAR 29331). One or more values changed for the –1 speed in tables covering 3.3 V LVCMOS, 2.5 V LVCMOS, 1.8 V LVCMOS, 1.5 V LVCMOS, Combinatorial Cell Propagation Delays, and A2F200 Global Resources.	2-31 to 2-76
	Table 2-80 • A2F500 Global Resource is new.	2-60
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised (SAR 27585).	2-76
	The programmable analog specifications tables were revised with updated information.	2-78 to 2-87
	Table 4-1 • Supported JTAG Programming Hardware was revised by adding a note to indicate "planned support" for several of the items in the table.	4-7
	The note on JTAGSEL in the "In-System Programming" section was revised to state that SoftConsole selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care" (SAR 29261).	4-7
	The "CS288" and "FG256" pin tables for A2F060 are new, comparing the A2F060 function with the A2F200 function (SAR 29353).	5-24
	The "Handling When Unused" column was removed from the "FG256" pin table for A2F200 and A2F500 (SAR 29691).	5-42
Revision 4 (September 2010)	Table 2-8 • Power Supplies Configuration was revised. VCCRCOSC was moved to a column of its own with new values. VCCENVM was added to the table. Standby mode for VJTAG and VPP was changed from 0 V to N/A. "Disable" was changed to "Off" in the eNVM column. The column for RCOSC was deleted.	2-10
	The "Power-Down and Sleep Mode Implementation" section was revised to include VCCROSC.	2-11
Revision 3 (September 2010)	The "I/Os and Operating Voltage" section was revised to list "single 3.3 V power supply with on-chip 1.5 V regulator" and "external 1.5 V is allowed" (SAR 27663).	I
	The CS288 package was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 27101), "Product Ordering Codes" table, and "Temperature Grade Offerings" table (SAR 27044). The number of direct analog inputs for the FG256 package in A2F060 was changed from 8 to 6.	III, VI, VI
	Two notes were added to the "SmartFusion cSoC Family Product Table" indicating limitations for features of the A2F500 device: *Two PLLs are available in CS288 and FG484 (one PLL in FG256).* *[ADCs, DACs, SCBs, comparators, current monitors, and bipolar high voltage monitors are] Available on FG484 only. FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.* Table cells were merged in rows containing the same values for easier reading (SAR 24748).	II
	The security feature option was added to the "Product Ordering Codes" table.	VI

Revision	Changes	Page
Revision 0 (continued)	"SmartFusion Development Tools" section was replaced with new content.	3-1
	The pin description tables were revised by adding additional pins to reflect the pinout for A2F500.	5-1 through 5-16
	The descriptions for "GNDSDD1" and "VCC33SDD1" were revised.	5-1, 5-2
	The description for "VCC33A" was revised.	5-2
	The pin tables for the "FG256" and "FG484" were replaced with tables that compare pin functions across densities for each package.	5-42
Draft B (December 2009)	The "Digital I/Os" section was renamed to the "I/Os and Operating Voltage" section and information was added regarding digital and analog VCC.	I
	The "SmartFusion cSoC Family Product Table" and "Package I/Os: MSS + FPGA I/Os" section were revised.	II
	The terminology for the analog blocks was changed to "programmable analog," consisting of two blocks: the analog front-end and analog compute engine. This is reflected throughout the text and in the "SmartFusion cSoC Block Diagram".	IV
	The "Product Ordering Codes" table was revised to add G as an ordering code for eNVM size.	VI
	Timing tables were populated with information that has become available for speed grade –1.	N/A
	All occurrences of the VMV parameter were removed.	N/A
	The SDD[n] voltage parameter was removed from Table 2-2 • Analog Maximum Ratings.	2-2
	Table 36-4 • Flash Programming Limits – Retention, Storage and Operating Temperature was replaced with Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits.	2-4
	The "Thermal Characteristics" section was revised extensively.	2-7
	Table 2-8 • Power Supplies Configuration was revised significantly.	2-10
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs were updated.	2-12
	Figure 2-2 • Timing Model was updated.	2-19
	The temperature associated with the reliability for LVTTL/LVCMOS in Table 2-34 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was changed from 110º to 100º.	2-29
	The values in Table 2-78 • Combinatorial Cell Propagation Delays were updated.	2-57
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator is new. Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator was revised.	2-62
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V and Table 2-91 • FlashROM Access Time, Worse Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V are new.	2-76
	The performance tables in the "Programmable Analog Specifications" section were revised, including new data available. Table 2-98 • Analog Sigma-Delta DAC is new.	2-78
	The "256-Pin FBGA" table for A2F200 is new.	4-15