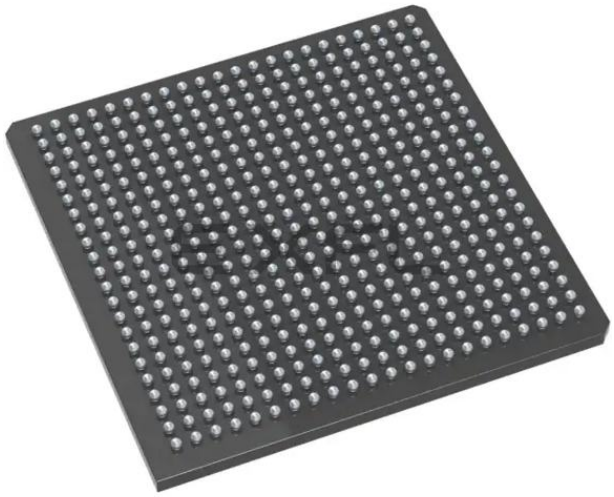

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What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1fg484

SmartFusion Family Overview

SmartFusion DC and Switching Characteristics

SmartFusion Development Tools

SmartFusion Programming

Pin Descriptions

Datasheet Information

Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings* Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.74	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	155.65
2.5 V LVCMOS	10	2.5	–	88.23
1.8 V LVCMOS	10	1.8	–	45.03
1.5 V LVCMOS (JESD8-11)	10	1.5	–	31.01

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
2.5 V LVCMOS	12 mA	High	35	–	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
1.8 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
1.5 V LVCMOS	12 mA	High	35	–	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
3.3 V PCI	Per PCI spec	High	10	25[1]	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25[1]	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
LVDS	24 mA	High	–	–	0.50	1.53	0.03	1.55	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.50	1.46	0.03	1.46	–	–	–	–	–	–	–	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns
2.5 V LVCMOS	8 mA	High	10	–	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns
1.8 V LVCMOS	4 mA	High	10	–	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns
1.5 V LVCMOS	2 mA	High	10	–	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-35 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-36 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

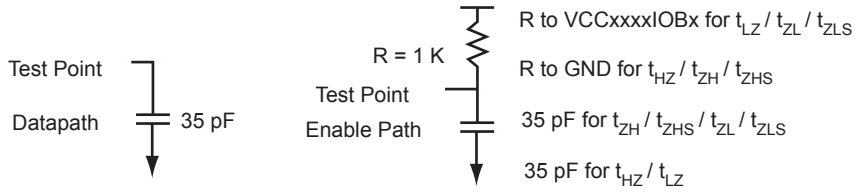

Figure 2-6 • AC Loading

Table 2-37 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

*Note: *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-41 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-42 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

2.5 V LVCMOS	VIL		V_{IH}		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max., mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

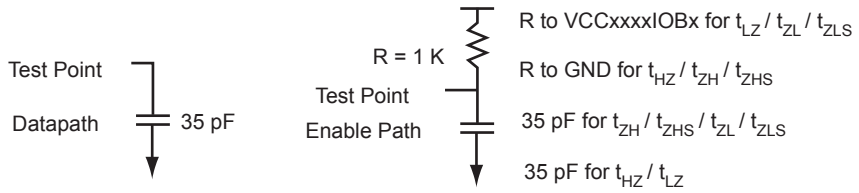

Figure 2-7 • AC Loading

Table 2-43 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Table 2-63 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}[1]	Output lower current	0.65	0.91	1.16	mA
I_{OH}[1]	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}[2]	Input high leakage current			15	µA
I_{IL}[2]	Input low leakage current			15	µA
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. *I_{OL}/I_{OH} defined by V_{ODIFF}/(resistor network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-65 • LVDS
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.83	0.04	1.87	ns
–1	0.50	1.53	0.03	1.55	ns

Notes:

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

***Table 2-69* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-14 on page 2-44 for more information.*

***Table 2-70* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* *See Figure 2-15 on page 2-46 for more information.*

Input Register

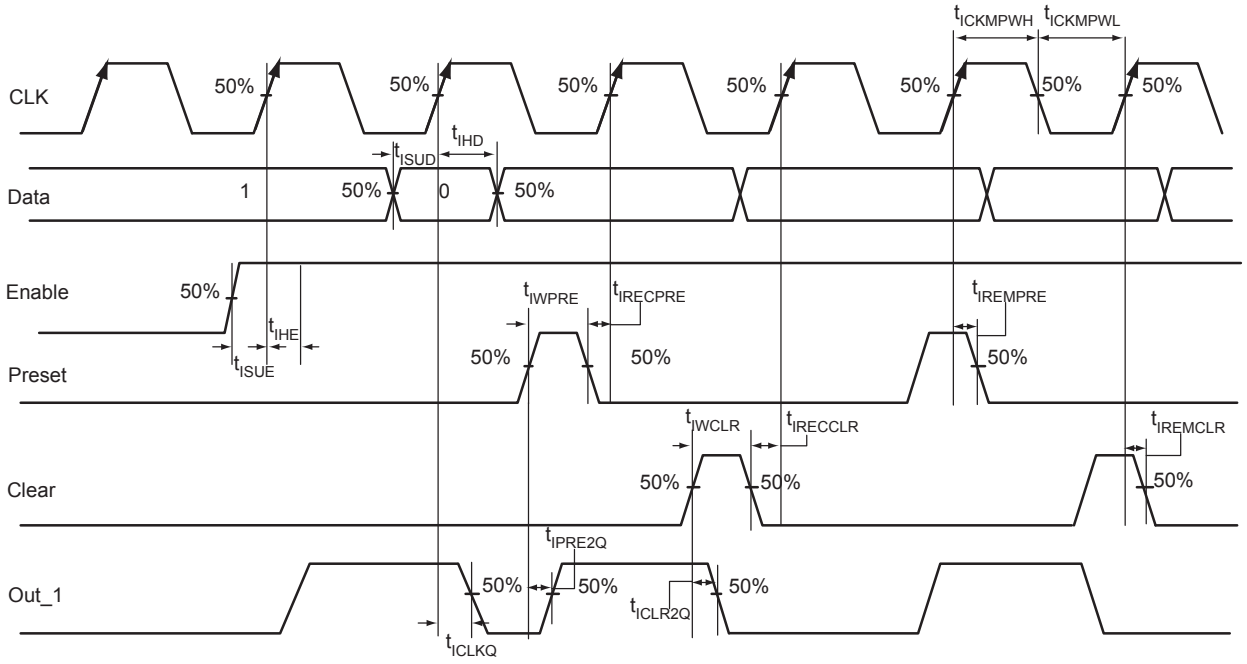

Figure 2-16 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-71 • **Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.55	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.55	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

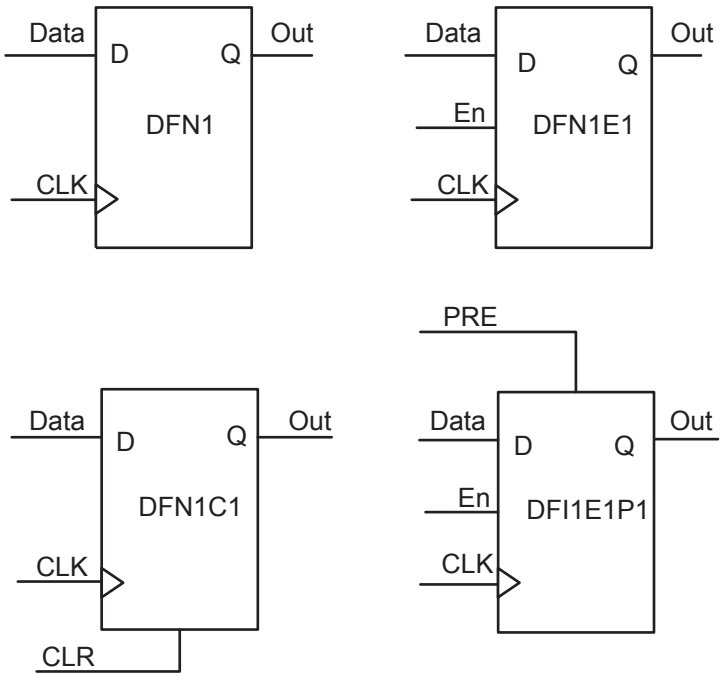

Figure 2-25 • Sample of Sequential Cells

Global Resource Characteristics

A2F200 Clock Tree Topology

Clock delays are device-specific. Figure 2-27 is an example of a global tree used for clock routing. The global tree presented in Figure 2-27 is driven by a CCC located on the west side of the A2F200 device. It is used to drive all D-flip-flops in the device.

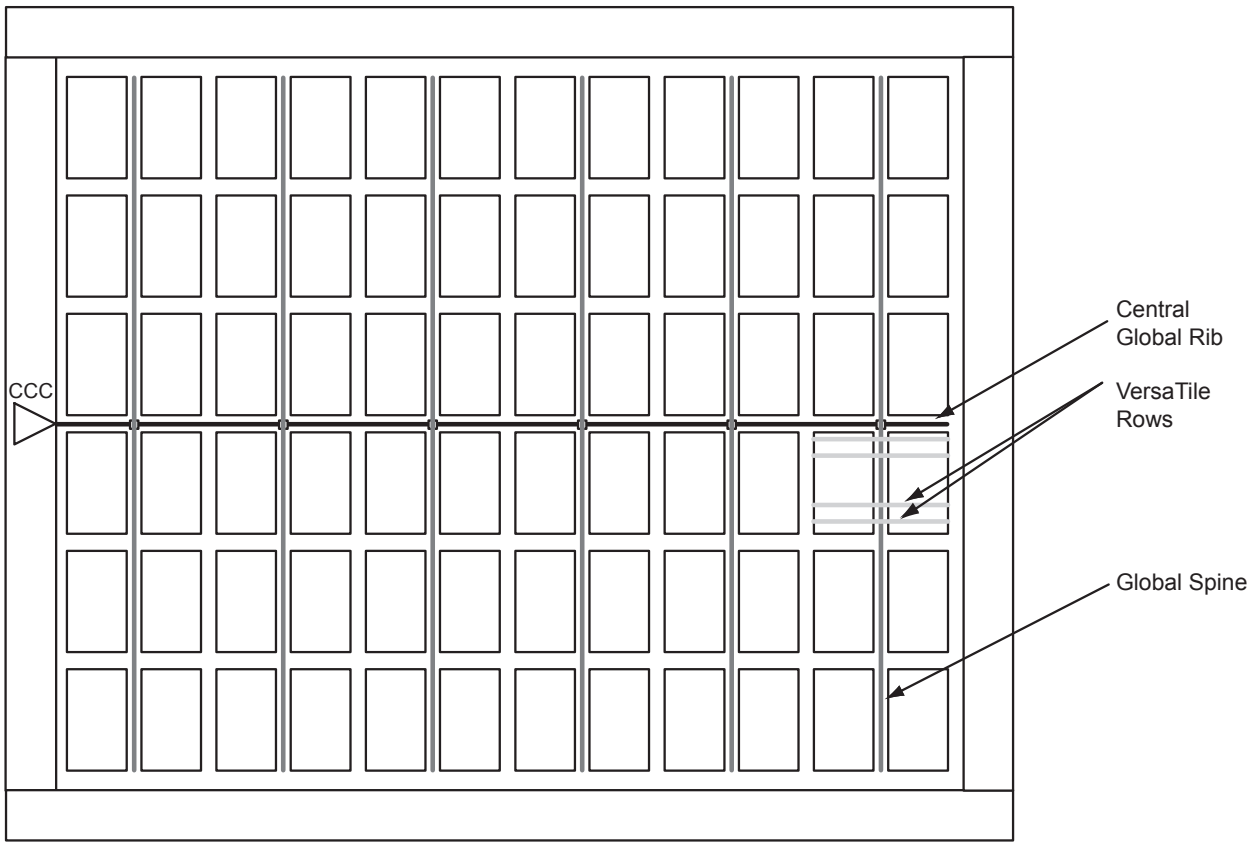

Figure 2-27 • **Example of Global Tree Use in an A2F200 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-63. Table 2-80 through Table 2-82 on page 2-61 present minimum and maximum global clock delays for the SmartFusion cSoCs. Minimum and maximum delays are measured with minimum and maximum loading.

Main and Lower Power Crystal Oscillator

The tables below describes the electrical characteristics of the main and low power crystal oscillator.

***Table 2-84* • Electrical Characteristics of the Main Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency	Using external crystal	0.032		20	MHz
		Using ceramic resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output duty cycle			50		%
	Output jitter	With 10 MHz crystal		1		ns RMS
IDYNXTAL	Operating current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby current of crystal oscillator			10		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	RC [Tested at 3.24Mhz]		300	550	µs
		0.032–0.2 [Tested at 32KHz]		500	3,000	µs
		0.2–2.0 [Tested at 2MHz]		8	12	µs
		2.0–20.0 [Tested at 20MHz]		160	180	µs

***Table 2-85* • Electrical Characteristics of the Low Power Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency			32		KHz
	Output duty cycle			50		%
	Output jitter			30		ns RMS
IDYNXTAL	Operating current	32 KHz		10		µA
ISTBXTAL	Standby current of crystal oscillator			2		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	Test load used: 20 pF		2.5		s
		Test load used: 30 pF		3.7	13	s

Timing Characteristics

Table 2-87 • RAM4K9
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.15	0.17	ns
t_{ENH}	REN, WEN hold time	0.10	0.12	ns
t_{BKS}	BLK setup time	0.24	0.28	ns
t_{BKH}	BLK hold time	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.19	0.22	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.81	2.18	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.39	2.87	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.91	1.09	ns
t_{C2CWWH}[1]	Address collision clk-to-clk delay for reliable write after write on same address—applicable to rising edge	0.23	0.26	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.34	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address— applicable to opening edge	0.37	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	0.94	1.12	ns
	RESET Low to Data Out Low on DOUT (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.22	ns
t_{CYC}	Clock cycle time	3.28	3.28	ns
F_{MAX}	Maximum clock frequency	305	305	MHz

Notes:

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Voltage Regulator

Table 2-99 • **Voltage Regulator**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	T_J = 25°C		1.425	1.5	1.575	V
V_{OS}	Output offset voltage	T_J = 25°C			11		mV
ICC33A	Operation current	T_J = 25°C	I_{LOAD} = 1 mA		3.4		mA
			I_{LOAD} = 100 mA		11		mA
			I_{LOAD} = 0.5 A		21		mA
ΔV_{OUT}	Load regulation	T_J = 25°C	I_{LOAD} = 1 mA to 0.5 A		5.8		mV
ΔV_{OUT}	Line regulation	T_J = 25°C	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA		5.3		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD}= 100 mA		5.3		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500mA		5.3		mV/V
	Dropout voltage[1]	T_J = 25°C	I_{LOAD} = 1 mA		0.63		V
			I_{LOAD} = 100 mA		0.84		V
			I_{LOAD} = 0.5 A		1.35		V
I_{PTBASE}	PTBase current	T_J = 25°C	I_{LOAD} = 1 mA		48		µA
			I_{LOAD} = 100 mA		736		µA
			I_{LOAD} = 0.5 A		12		mA
	Startup time[2]	T_J = 25°C			200		µs

Notes:

1. *Dropout voltage is defined as the minimum VCC33A voltage. The parameter is specified with respect to the output voltage. The specification represents the minimum input-to-output differential voltage required to maintain regulation.*
2. *Assumes 10 µF.*

Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 2-48 on page 2-92.

***Table 2-101* • I^2C Characteristics**
Commercial Case Conditions: T_J = 85ºC, V_{DD} = 1.425 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
V_{IL}	Minimum input low voltage	–	See Table 2-36 on page 2-30	–
	Maximum input low voltage	–	See Table 2-36	–
V_{IH}	Minimum input high voltage	–	See Table 2-36	–
	Maximum input high voltage	–	See Table 2-36	–
V_{OL}	Maximum output voltage low	I_{OL} = 8 mA	See Table 2-36	–
I_{IL}	Input current high	–	See Table 2-36	–
I_{IH}	Input current low	–	See Table 2-36	–
V_{hyst}	Hysteresis of Schmitt trigger inputs	–	See Table 2-33 on page 2-29	V
T_{FALL}	Fall time [2]	VIHmin to VILMax, C_{load} = 400 pF	15.0	ns
		VIHmin to VILMax, C_{load} = 100 pF	4.0	ns
T_{RISE}	Rise time [2]	VILMax to VIHmin, C_{load} = 400pF	19.5	ns
		VILMax to VIHmin, C_{load} = 100pF	5.2	ns
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	8.0	pF
$R_{pull-up}$	Output buffer maximum pull-down Resistance [1]	–	50	Ω
$R_{pull-down}$	Output buffer maximum pull-up Resistance [1]	–	150	Ω
D_{max}	Maximum data rate	Fast mode	400	Kbps
t_{LOW}	Low period of I2C_x_SCL [3]	–	1	pclk cycles
t_{HIGH}	High period of I2C_x_SCL [3]	–	1	pclk cycles
$t_{HD;STA}$	START hold time [3]	–	1	pclk cycles
$t_{SU;STA}$	START setup time [3]	–	1	pclk cycles
$t_{HD;DAT}$	DATA hold time [3]	–	1	pclk cycles
$t_{SU;DAT}$	DATA setup time [3]	–	1	pclk cycles

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
3. *For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I^2C) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (January 2013)	The "SmartFusion cSoC Family Product Table" section has been updated to specify that External Memory Controller support for A2F060-TQ144 is not available (SAR 41555).	II
	The following Note was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 41027): "There are no LVTTL capable direct inputs available on A2F060 devices."	III
	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43218).	VI
	Added a note to Table 2-3 • Recommended Operating Conditions[5,6] (SAR 43428): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-3
	Statements about the state of the I/Os during programming were updated in the following sections: "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" and "User I/O Naming Conventions" (SAR 43380).	2-4, 5-7
	In Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits, the upper value of temperature ranges was corrected from "Min." to "Max." (SAR 41826).	2-4
	Information for A2F200M3F-CS288 was added to Table 2-6 • Package Thermal Resistance. The die size column was removed (SARs 41828, 42168). Also added details for A2F200M3F-PQG208I (SAR 35728).	2-7
	Added the following note to Table 2-65 • LVDS and Table 2-68 • LVPECL: "The above mentioned timing parameters correspond to 24mA drive strength." (SAR 43457)	2-41, 2-43
	The note in Table 2-86 • SmartFusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 34816).	2-63
	The SRAM collision data in Table 2-87 • RAM4K9 and Table 2-88 • RAM512X18 was updated (SAR 38583).	2-69,2-70
	The maximum input bias current for comparators 1, 3, 5, 7, and 9, in Table 2-97 • Comparator Performance Specifications, was revised from 60 to 100 nA (SAR 36008).	2-84

Revision	Changes	Page
Revision 10 (continued)	Corrected the Start-up time unit from "ms" to "µs" in Table 2-99 • Voltage Regulator (SAR 39395).	2-87
	Added the "References" section for "SmartFusion Development Tools" (SAR 43460).	3-1
	Updated the "References" section for Programming (SAR 43304). Added the "Application Notes on IAP Programming Technique" section (SAR 43458).	4-9
	A note was added to the "Supply Pins" table, referring to the *SmartFusion cSoC Board Design Guidelines* application note for details on VCCPLLx capacitor recommendations (SAR 42183).	5-1
	In the "Supply Pins" section, the VPP capacitor value section has been modified to: "For proper programming, 0.01µF, and 0.1µF to 1µF capacitors, (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible." (SAR 43569).	5-1
	In the "User-Defined Supply Pins" section, added description 'These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices.' for GPIO_x (SAR 28595).	5-5
	Updated the MAINXIN and MAINXOUT pin descriptions in the "Special Function Pins" section to read "If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating." (SAR 42807).	5-8
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 9 (September 2012)	The number of signal conditioning blocks (SCBs) for A2F500 in the "SmartFusion cSoC Family Product Table" was corrected to 4. Previously it had incorrectly been listed as 2 (SAR 39536).	II
	The "Product Ordering Codes" section was revised to clarify that only one eNVM size for each device is currently available (SAR 40333).	VI
	Information pertaining to analog I/Os was added to the "Specifying I/O States During Programming" section on page 1-3 (SAR 34836).	1-3
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34757).	2-27
	Maximum values for VIL and VIH were corrected in LVPECL Table 2-66 • Minimum and Maximum DC Input and Output Levels (SAR 37695).	2-43
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 29270).	2-59
	The temperature range for accuracy in Table 2-83 • Electrical Characteristics of the RC Oscillator was changed from "0°C to 85°C" to "–40°C to 100°C" (SAR 33670). The units for jitter were changed from ps to ps RMS (SAR 34270).	2-61
	In Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator, the output jitter for the 10 MHz crystal was corrected from 50 ps RMS to 1 ns RS (SAR 32939). Values for the startup time of VILXTAL were added (SAR 25248).	2-62
	In Table 2-85 • Electrical Characteristics of the Low Power Oscillator, output jitter was changed from 50 ps RMS to 30 ps RMS (SAR 32939). A value for ISTBXTAL standby current was added (SAR 25249). Startup time for a test load of 30 pF was added (SAR 27436).	2-62

Revision	Changes	Page
Revision 8 (continued)	The description of "In-application programming (IAP)" methodology was changed to state the difference for A2F060 and A2F500 compared to A2F200 (SAR 37808).	4-7
	The "Global I/O Naming Conventions" section is new (SARs 28996, 31147). The description for IO "User Pins" was revised accordingly and moved out of the table and into a new section: "User I/O Naming Conventions".	5-6, 5-6
	The descriptions for "MAINXIN" and "MAINXOUT" were revised to state how they should be handled if using an external RC network or clock input (SAR 32594).	5-8
	The description and type was revised for the "MSS_RESET_N" pin (SAR 34133).	5-9
	The "TQ144" section and pin table for A2F060 are new (SAR 36246).	5-18
Revision 7 (August 2011)	The title of the datasheet was changed from SmartFusion Intelligent Mixed Signal FPGAs to SmartFusion Customizable System-on-Chip (cSoC). Terminology throughout was changed accordingly. The term cSoC defines a category of devices that include at least FPGA fabric and a processor subsystem of some sort. It can also include any of the following: analog, SerDes, ASIC blocks, customer specific IP, or application-specific IP. SmartFusion is Microsemi's first cSoC (SAR 33071).	N/A
	The "SmartFusion cSoC Family Product Table" was revised to remove the note stating that the A2F060 device is under definition and subject to change (SAR 33070). A note was added for EMC, stating that it is not available on A2F500 for the PQ208 package (SAR 33041).	II
	The "SmartFusion cSoC Device Status" table was revised. The status for A2F060 CS288 and FG256 moved from Advance to Preliminary. A2F200 PQ208 and A2F500 PQ208 moved from Advance to Production (SAR 33069).	III
	The "Package I/Os: MSS + FPGA I/Os" table was revised. The number of direct analog inputs for A2F060 packages increased from 6 to 11. The number of MSS I/Os for the A2F060 FG256 package increased from 25 to 26 (SAR 33070). A note was added stating that EMC is not available for the A2F500 PQ208 package (SAR 33041).	III
	The note associated with the "SmartFusion cSoC System Architecture" diagram was corrected from "Architecture for A2F500" to "Architecture for A2F200" (SAR 32578).	V
	The Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 32151).	VI
	The "Security" section and "Secure Programming" section were updated to clarify that although no existing security measures can give an absolute guarantee, SmartFusion cSoCs implement the best security available in the industry (SAR 32865).	1-2, 4-9
	Storage temperature, T_{STG}, and junction temperature, T_J, were added to Table 2-1 • Absolute Maximum Ratings (SAR 30863).	2-1
	AC/DC characteristics for A2F060 were added to the "SmartFusion DC and Switching Characteristics" chapter (SAR 33132). The following tables were updated: Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V Table 2-98 • Analog Sigma-Delta DAC Table 2-100 • SPI Characteristics	 2-12 2-13 2-76 2-85 2-89