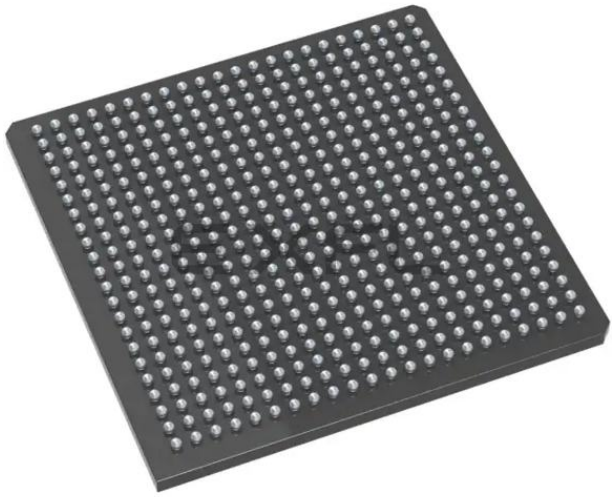

Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1fg484i

Table 2-2 • **Analog Maximum Ratings**

Parameter	Conditions	Min.	Max.	Units
ABPS[n] pad voltage (relative to ground)	GDEC[1:0] = 00 (±15.36 V range)			
	Absolute maximum	–11.5	14.4	V
	Recommended	–11	14	V
	GDEC[1:0] = 01 (±10.24 V range)	–11.5	12	V
	GDEC[1:0] = 10 (±5.12 V range)	–6	6	V
	GDEC[1:0] = 11 (±2.56 V range)	–3	3	V
CM[n] pad voltage relative to ground)	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 0 (comparator off, for the associated even-numbered comparator)			
	Absolute maximum	–0.3	14.4	V
	Recommended	–0.3	14	V
	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
TM[n] pad voltage (relative to ground)	TMB_DI_ON = 0 (ADC isolated) COMP_EN = 1(comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
ADC[n] pad voltage (relative to ground)		–0.3	3.6	V

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-47 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	16	16	74	91	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

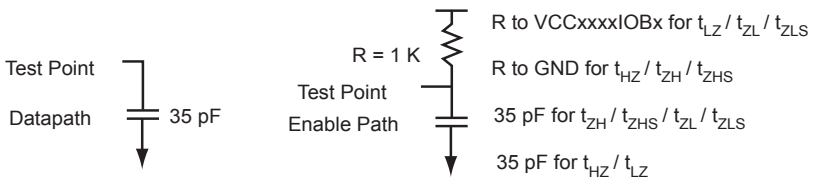

Figure 2-8 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Table 2-52 • 1.8 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	Std.	0.22	2.77	0.09	1.09	1.64	0.22	2.82	2.72	2.21	2.25	ns
	–1	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A † B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A † B † C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

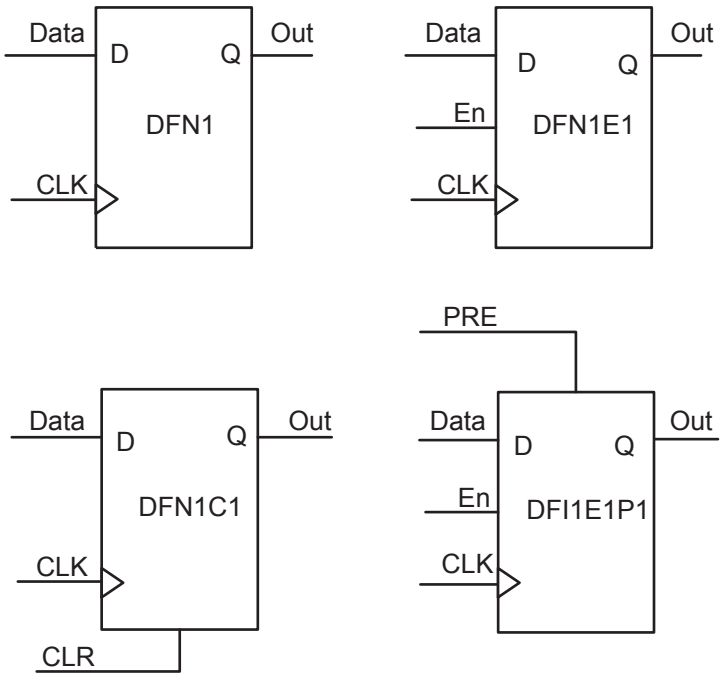

Figure 2-25 • Sample of Sequential Cells

Timing Characteristics

Table 2-80 • A2F500 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.54	1.73	1.84	2.08	ns
t_{RCKH}	Input High Delay for Global Clock	1.53	1.76	1.84	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.23		0.28	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-81 • A2F200 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.74	0.99	0.88	1.19	ns
t_{RCKH}	Input High Delay for Global Clock	0.76	1.05	0.91	1.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.29		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-86* • SmartFusion CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350[1]	MHz
Delay Increments in Programmable Delay Blocks[2,3,4]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		5.15	%
Delay Range in Block: Programmable Delay 1[2,3]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[2,3]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[2,3]		2.2		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6,7]	Maximum Peak-to-Peak Period Jitter			
	SSO d2		**SSO d4**		**SSO d8**		**SSO d16**	
	FG/CS	**PQ**	**FG/CS**	**PQ**	**FG/CS**	**PQ**	**FG/CS**	**PQ**
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*

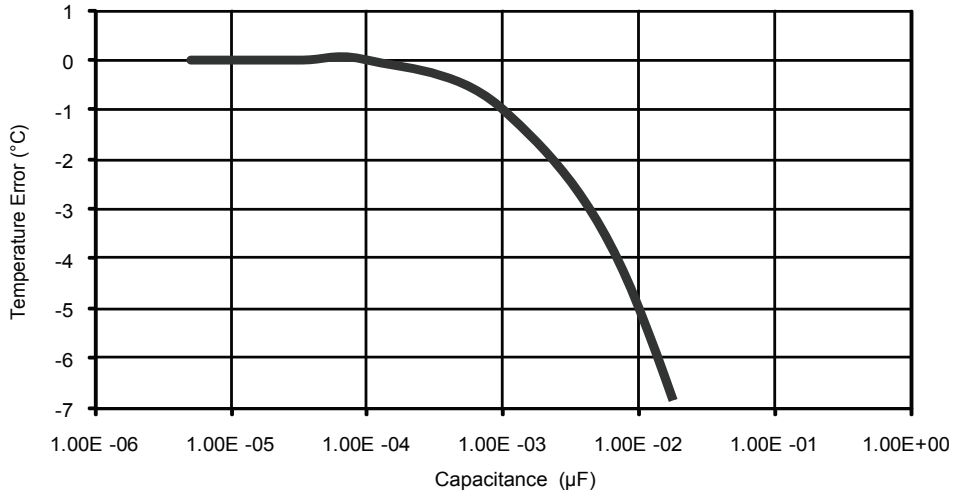

Figure 2-43 • **Temperature Error Versus External Capacitance**

***Table 2-98* • Analog Sigma-Delta DAC (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Sigma-delta DAC power supply current requirements (not including VAREFx)	Input = 0, EN = 1 (operational mode)				
	VCC33SDDx		30	35	µA
	VCC15A		3	5	µA
	Input = Half scale, EN = 1 (operational mode)				
	VCC33SDDx		160	165	µA
	VCC15A		33	35	µA
	Input = Full scale, EN = 1 (operational mode)				
	VCC33SDDx		280	285	µA
	VCC15A		70	75	µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

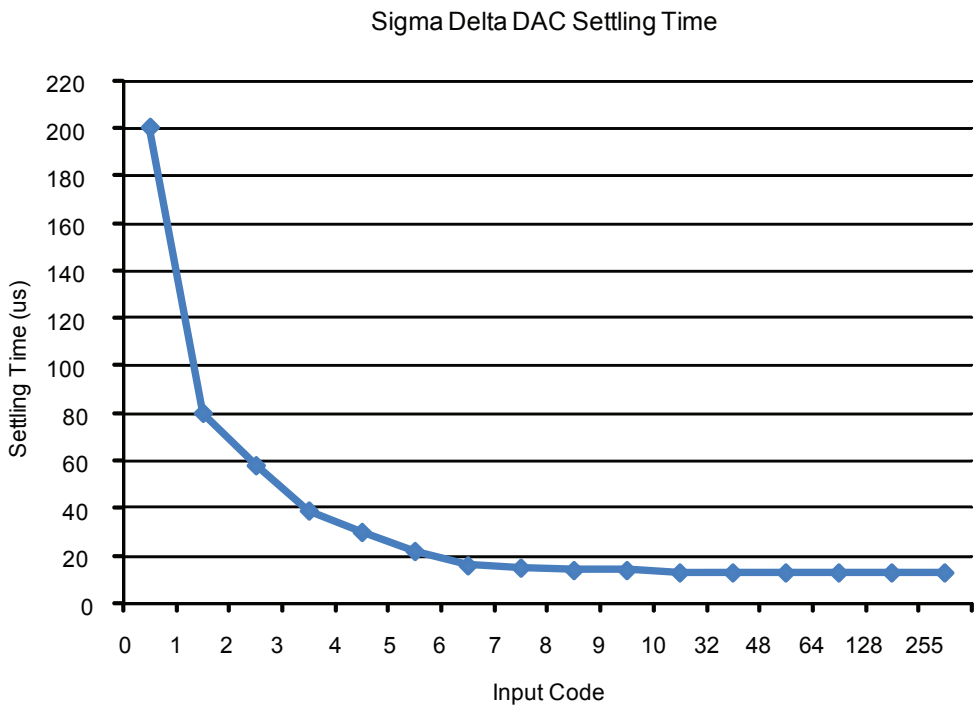

***Figure 2-44* • Sigma-Delta DAC Setting Time**

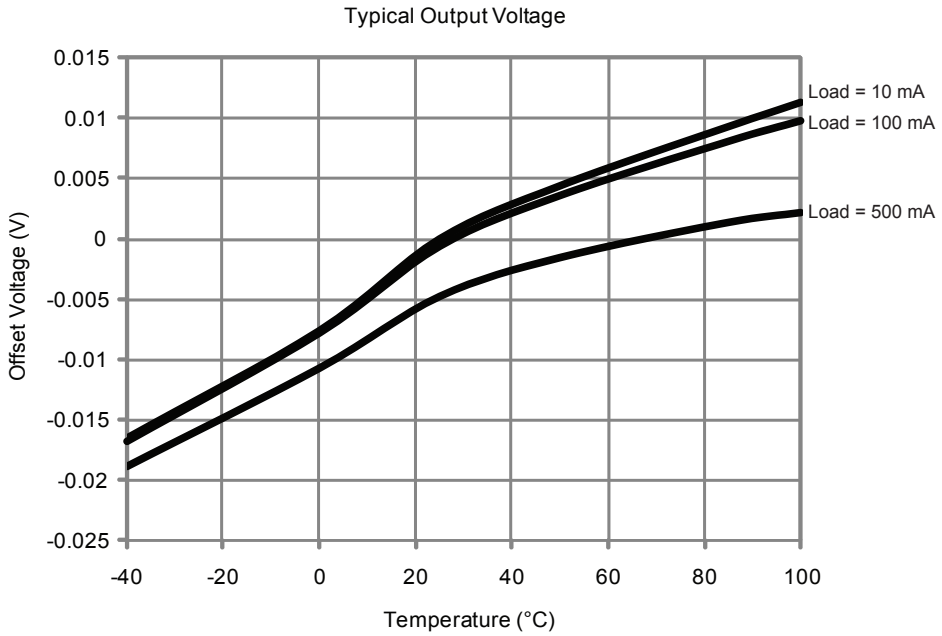

Figure 2-45 • **Typical Output Voltage**

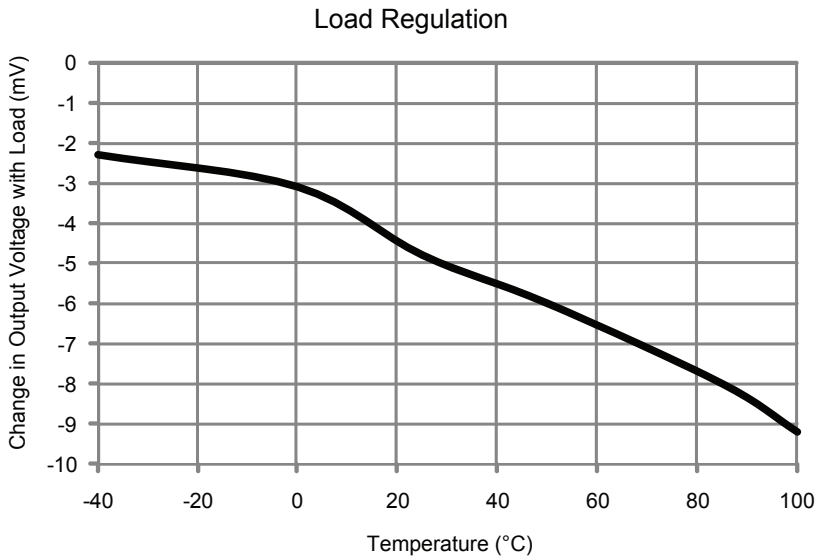

Figure 2-46 • **Load Regulation**

Table 2-100 • SPI Characteristics
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp6	Data from master (SPI_x_DO) setup time [2]	1	1	1	pclk cycles
sp7	Data from master (SPI_x_DO) hold time [2]	1	1	1	pclk cycles
sp8	SPI_x_DI setup time [2]	1	1	1	pclk cycles
sp9	SPI_x_DI hold time [2]	1	1	1	pclk cycles

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

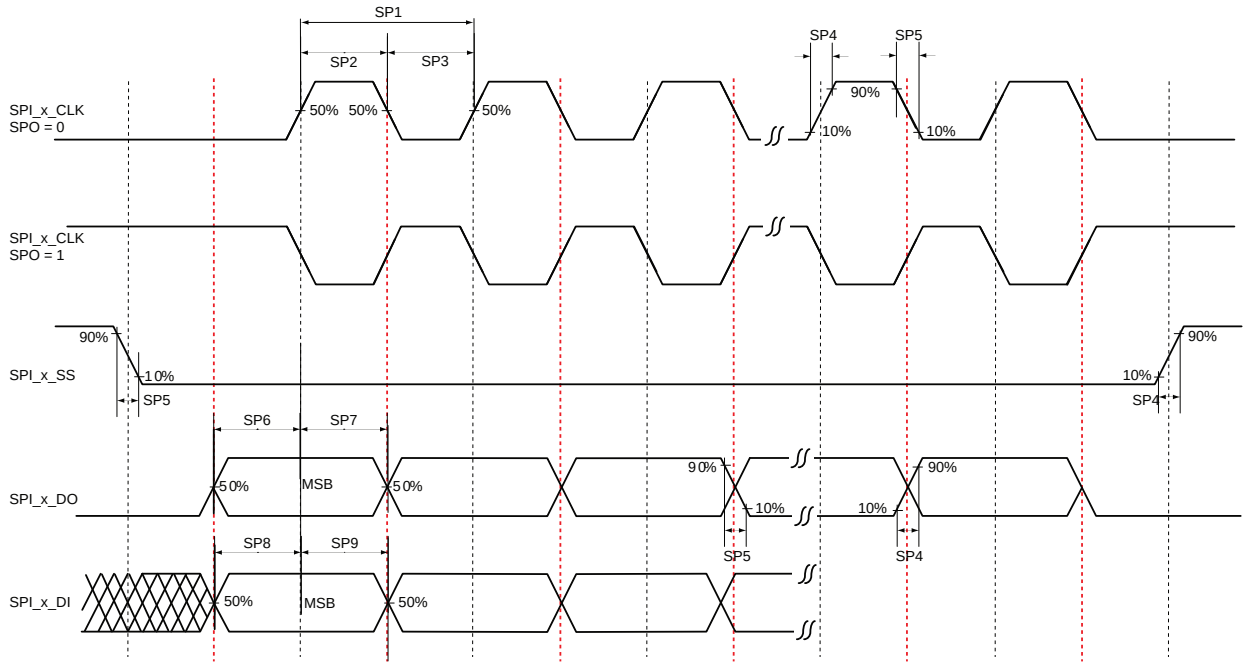

Figure 2-47 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Name	Type	Description
VCC15A	Supply	Clean analog 1.5 V supply to the analog circuitry. Always power this pin.
VCC15ADC0	Supply	Analog 1.5 V supply to the first ADC. Always power this pin.
VCC15ADC1	Supply	Analog 1.5 V supply to the second ADC. Always power this pin.
VCC15ADC2	Supply	Analog 1.5 V supply to the third ADC. Always power this pin.
VCC33A	Supply	Clean 3.3 V analog supply to the analog circuitry. VCC33A is also used to feed the 1.5 V voltage regulator for designs that do not provide an external supply to VCC. Refer to the Voltage Regulator (VR), Power Supply Monitor (PSM), and Power Modes section in the *SmartFusion Microcontroller Subsystem User's Guide* for more information.
VCC33ADC0	Supply	Analog 3.3 V supply to the first ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33ADC1	Supply	Analog 3.3 V supply to the second ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33ADC2	Supply	Analog 3.3 V supply to the third ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33AP	Supply	Analog clean 3.3 V supply to the charge pump. To avoid high current draw, VCC33AP should be powered up simultaneously with or after VCC33A. Can be pulled down if unused.[1]
VCC33N	Supply	–3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to GND. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
VCC33SDD0	Supply	Analog 3.3 V supply to the first sigma-delta DAC
VCC33SDD1	Supply	Common analog 3.3 V supply to the second and third sigma-delta DACs
VCCENVM	Supply	Digital 1.5 V power supply to the embedded nonvolatile memory blocks. To avoid high current draw, VCC should be powered up before or simultaneously with VCCENVM.
VCCESRAM	Supply	Digital 1.5 V power supply to the embedded SRAM blocks. Available only on the 208PQFP package. It should be connected to VCC (in other packages, it is internally connected to VCC).
VCCFPGAIOB0	Supply	Digital supply to the FPGA fabric I/O bank 0 (north FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB1	Supply	Digital supply to the FPGA fabric I/O bank 1 (east FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
AA11	ADC9	ADC6	ADC6
AA12	ABPS1	ABPS7	ABPS7
AA13	ADC6	TM2	TM2
AA14	NC	ABPS4	ABPS4
AA15	NC	SDD1	SDD1
AA16	GNDVAREF	GNDVAREF	GNDVAREF
AA17	VAREFOUT	VAREFOUT	VAREFOUT
AA18	PU_N	PU_N	PU_N
AA19	VCC33A	VCC33A	VCC33A
AA20	PTEM	PTEM	PTEM
AA21	GND	GND	GND
B1	GND	GND	GND
B21	IO17PDB0V0	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
C1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
C3	VCOMPLA0	VCOMPLA	VCOMPLA0
C4	VCCPLL0	VCCPLL	VCCPLL0
C5	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C6	EMC_AB[1]/IO04PPB0V0	EMC_AB[1]/IO04PPB0V0	EMC_AB[1]/IO06PPB0V0
C7	GND	GND	GND
C8	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
C9	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
C10	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
C11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C12	EMC_AB[9]/IO08PPB0V0	EMC_AB[9]/IO08PPB0V0	EMC_AB[9]/IO13PPB0V0
C13	EMC_AB[15]/IO11PPB0V0	EMC_AB[15]/IO11PPB0V0	EMC_AB[15]/IO15PPB0V0
C14	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C15	GND	GND	GND
C16	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C17	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C18	NC	NC	VCCPLL1
C19	NC	NC	VCOMPLA1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
K17	GNDLPXTAL	GNDLPXTAL	GNDLPXTAL
K19	GNDMAINXTAL	GNDMAINXTAL	GNDMAINXTAL
K21	MAINXIN	MAINXIN	MAINXIN
L1	GNDRCOSC	GNDRCOSC	GNDRCOSC
L3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
L5	EMC_DB[2]/IO37NPB5V0	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
L6	NC	GNDQ	GNDQ
L8	VCC	VCC	VCC
L9	GND	GND	GND
L10	VCC	VCC	VCC
L12	VCC	VCC	VCC
L13	GND	GND	GND
L14	VCC	VCC	VCC
L16	VCCLPXTAL	VCCLPXTAL	VCCLPXTAL
L17	VDDBAT	VDDBAT	VDDBAT
L19	LPXIN	LPXIN	LPXIN
L21	MAINXOUT	MAINXOUT	MAINXOUT
M1	VCCRCOSC	VCCRCOSC	VCCRCOSC
M3	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
M5	GPIO_5/IO28RSB4V0	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
M6	GND	GND	GND
M8	GND	GND	GND
M9	VCC	VCC	VCC
M10	GND	GND	GND
M11	VCC	VCC	VCC
M12	GND	GND	GND
M13	VCC	VCC	VCC
M14	GND	GND	GND
M16	TMS	TMS	TMS
M17	VJTAG	VJTAG	VJTAG
M19	TDO	TDO	TDO

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
32	VCCRCOSC	VCCRCOSC
33	MSS_RESET_N	MSS_RESET_N
34	VCCESRAM	VCCESRAM
35	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
36	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
37	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
38	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
39	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
40	GND	GND
41	VCCMSSIOB4	VCCMSSIOB4
42	VCC	VCC
43	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
44	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
45	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
46	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
47	MAC_CLK	MAC_CLK
48	GNDSDD0	GNDSDD0
49	VCC33SDD0	VCC33SDD0
50	VCC15A	VCC15A
51	PCAP	PCAP
52	NCAP	NCAP
53	VCC33AP	VCC33AP
54	VCC33N	VCC33N
55	SDD0	SDD0
56	GNDA	GNDA
57	GNDAQ	GNDAQ
58	ABPS0	ABPS0
59	ABPS1	ABPS1
60	CM0	CM0
61	TM0	TM0
62	GNDTM0	GNDTM0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
125	TMS	TMS
126	TDO	TDO
127	TRSTB	TRSTB
128	VJTAG	VJTAG
129	VDDBAT	VDDBAT
130	VCCLPXTAL	VCCLPXTAL
131	LPXOUT	LPXOUT
132	LPXIN	LPXIN
133	GNDLPXTAL	GNDLPXTAL
134	GNDMAINXTAL	GNDMAINXTAL
135	MAINXOUT	MAINXOUT
136	MAINXIN	MAINXIN
137	VCCMAINXTAL	VCCMAINXTAL
138	GND	GND
139	VCC	VCC
140	VPP	VPP
141	VCCFPGAIOB1	VCCFPGAIOB1
142	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
143	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
144	GDC0/IO29NSB1V0	GDC0/IO38NSB1V0
145	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
146	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
147	VCCFPGAIOB1	VCCFPGAIOB1
148	GND	GND
149	VCC	VCC
150	IO25NDB1V0	IO30NDB1V0
151	GCC2/IO25PDB1V0	GBC2/IO30PDB1V0
152	IO23NDB1V0	IO28NDB1V0
153	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
154	GBC2/IO21PSB1V0	GBB2/IO27NDB1V0
155	GBA2/IO20PSB1V0	GBA2/IO27PDB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
M11	ADC6	TM2	TM2
M12	ADC5	CM2	CM2
M13	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
M14	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
M15	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
M16	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
N1	GPIO_8/IO25RSB4V0	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
N2	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
N3	VCC15A	VCC15A	VCC15A
N4	VCC33AP	VCC33AP	VCC33AP
N5	NC	ABPS3	ABPS3
N6	ADC4	TM1	TM1
N7	NC	GND33ADC0	GND33ADC0
N8	VCC33ADC0	VCC33ADC1	VCC33ADC1
N9	ADC8	ADC5	ADC5
N10	CM0	CM3	CM3
N11	GNDAQ	GNDAQ	GNDAQ
N12	VAREFOUT	VAREFOUT	VAREFOUT
N13	NC	GNDSDD1	GNDSDD1
N14	NC	VCC33SDD1	VCC33SDD1
N15	GND	GND	GND
N16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
P1	GNDSDD0	GNDSDD0	GNDSDD0
P2	VCC33SDD0	VCC33SDD0	VCC33SDD0
P3	VCC33N	VCC33N	VCC33N
P4	GNDA	GNDA	GNDA
P5	GNDAQ	GNDAQ	GNDAQ
P6	NC	CM1	CM1
P7	NC	ADC2	ADC2
P8	NC	VCC15ADC0	VCC15ADC0
P9	ADC9	ADC6	ADC6

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
C15	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO19NPB0V0	GBA0/IO23NPB0V0
C20	NC	NC
C21	GBC2/IO21PDB1V0	GBC2/IO30PDB1V0
C22	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
D1	GND	GND
D2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC	NC
D5	NC	NC
D6	GND	GND
D7	NC	IO00NPB0V0
D8	NC	IO03NPB0V0
D9	GND	GND
D10	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
D14	GND	GND
D15	GBC1/IO17PPB0V0	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
D17	GND	GND
D18	GBA1/IO19PPB0V0	GBA1/IO23PPB0V0
D19	NC	NC
D20	NC	NC
D21	IO21NDB1V0	IO30NDB1V0
D22	GND	GND
E1	GFC2/IO67PPB5V0	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5	VCCFPGAIOB5
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
J19	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
J20	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
J21	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
J22	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
K1	GND	GND
K2	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
K4	NC	IO74PPB5V0
K5	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
K6	NC	IO75PDB5V0
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC
K11	GND	GND
K12	VCC	VCC
K13	GND	GND
K14	VCC	VCC
K15	GND	GND
K16	VCCFPGAIOB1	VCCFPGAIOB1
K17	NC	IO37NDB1V0
K18	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
K19	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
K20	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
K21	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
K22	GND	GND
L1	NC	IO73PDB5V0
L2	NC	IO73NDB5V0
L3	NC	IO72PPB5V0
L4	GND	GND
L5	NC	IO74NPB5V0
L6	NC	IO75NDB5V0
L7	VCCFPGAIOB5	VCCFPGAIOB5
L8	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 3 (continued)	Two notes were added to the "Supply Pins" table (SAR 27109): 1. *The following supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* 2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	5-1
	The descriptions for the "VCC33N", "NCAP", and "PCAP" pins were revised to include information on what to do if analog SCB features and SDDs are not used (SAR 26744).	5-2, 5-9, 5-9
	Information was added to the "User Pins" table regarding tristating of used and unused GPIO pins. The IO portion of the table was revised to state that unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor (SAR 26890). Information was added regarding behavior of used I/O pins during power-up.	5-6
	The type for "EMC_RW_N" was changed from In/out to Out (SAR 25113).	5-12
	A note was added to the "Analog Front-End (AFE)" table stating that unused analog inputs should be grounded (SAR 26744).	5-14
	The "TQ144" section is new, with pin tables for A2F200 and A2F500 (SAR 27044).	5-18
	The "FG256" pin table was replaced and now includes "Handling When Unused" information (SAR 27709).	5-42
Revision 2 (May 2010)	Embedded nonvolatile flash memory (eNVM) was changed from "64 to 512 Kbytes" to "128 to 512 Kbytes" in the "Microcontroller Subsystem (MSS)" section and "SmartFusion cSoC Family Product Table" (SAR 26005).	I, II
	The main oscillator range of values was changed to "32 KHz to 20 MHz" in the "Microcontroller Subsystem (MSS)" section and the "SmartFusion cSoC Family Product Table" (SAR 24906).	I, II
	The value for t_{PD} was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the "Analog Front-End (AFE)" section (SAR 26005).	I
	The number of PLLs for A2F200 was changed from 2 to 1 in the "SmartFusion cSoC Family Product Table" (SAR 25093).	II
	Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the "Package I/Os: MSS + FPGA I/Os" table. The Max. column was removed from the table (SAR 26005).	III
	The Speed Grade section of the "Product Ordering Codes" table was revised (SAR 25257).	VI
Revision 1 (March 2010)	The "Product Ordering Codes" table was revised to add "blank" as an option for lead-free packaging and application (junction temperature range).	VI
	Table 2-3 • Recommended Operating Conditions[5,6] was revised. Ta (ambient temperature) was replaced with T_J (junction temperature).	2-3
	PDC5 was deleted from Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs.	2-13
	The formulas in the footnotes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised.	2-27
	The values for input biased current were revised in Table 2-93 • Current Monitor Performance Specification.	2-78
Revision 0 (March 2010)	The "Analog Front-End (AFE)" section was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps.	I