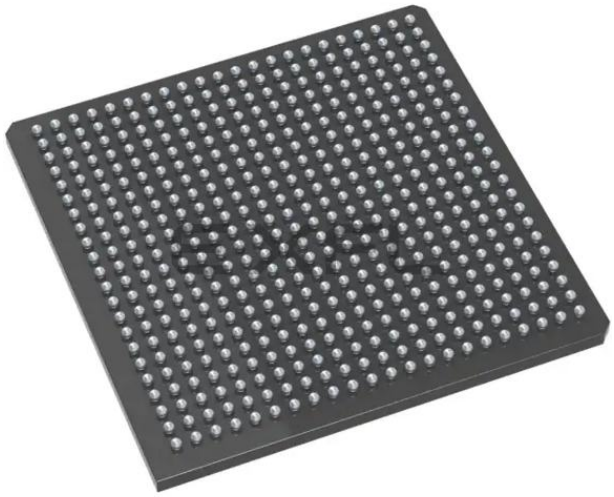
Microchip Technology - A2F200M3F-1FGG484 Datasheet



Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

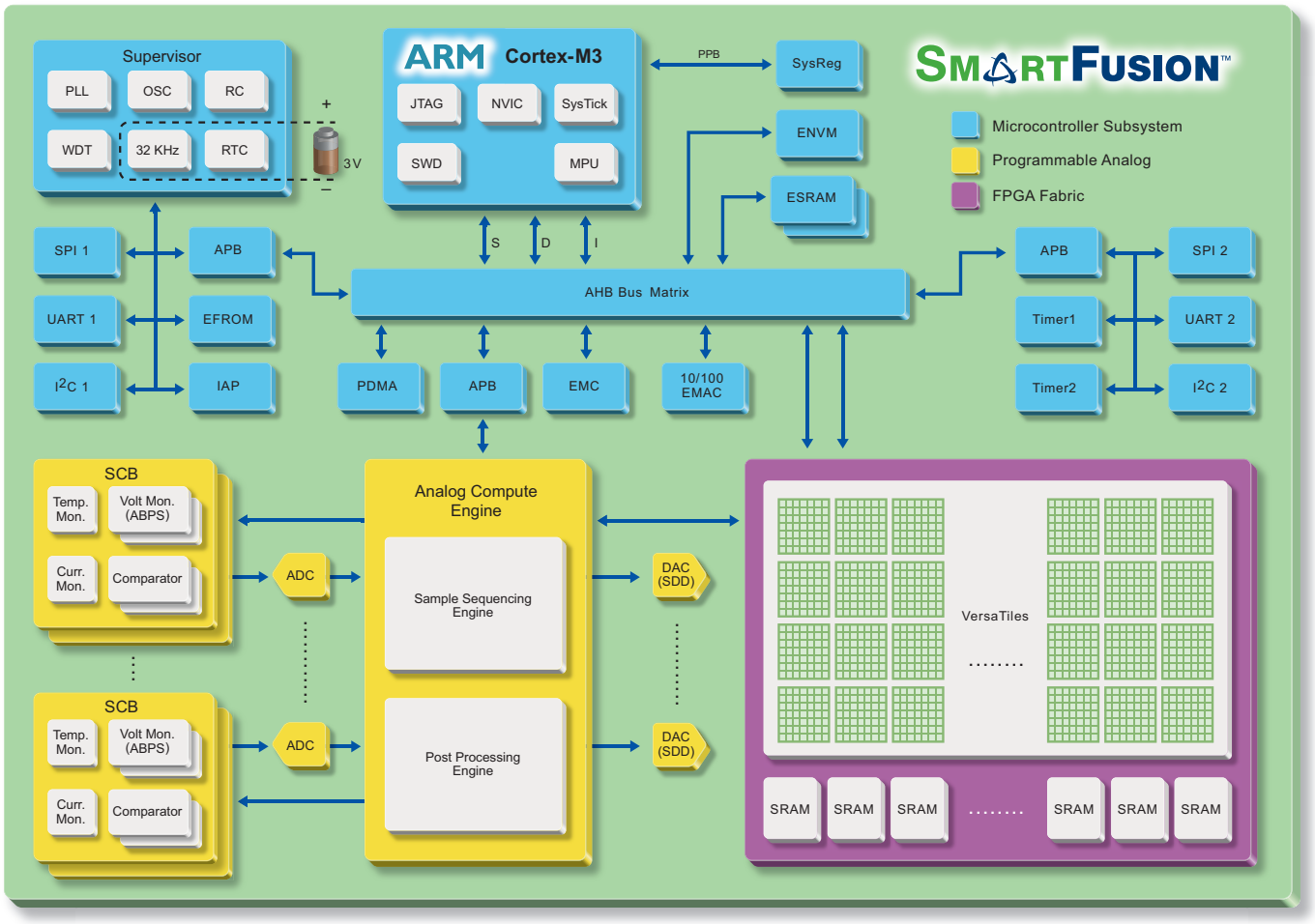
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1fgg484

SmartFusion cSoC Block Diagram



Legend:

SDD – Sigma-delta DAC
SCB – Signal conditioning block
PDMA – Peripheral DMA
IAP – In-application programming
ABPS – Active bipolar prescaler
WDT – Watchdog Timer
SWD – Serial Wire Debug

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of eNVM blocks used in the design
- The analog block used in the design, including the temperature monitor, current monitor, ABPS, sigma-delta DAC, comparator, low power crystal oscillator, RC oscillator and the main crystal oscillator
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-17 on page 2-18.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate to the eNVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

SoC Mode, Standby Mode, and Time Keeping Mode.

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

SoC Mode

$P_{STAT} = P_{DC1} + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = P_{DC2}$

Time Keeping Mode

$P_{STAT} = P_{DC3}$

Total Dynamic Power Consumption—P_{DYN}

SoC Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{eNVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB} + P_{LPXTAL\text{-}OSC} + P_{MSS}$

Standby Mode and Time Keeping Mode

P_{NET} = 0 W

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

SoC Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

P_{INPUTS} = 0 W

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

SoC Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-18.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-18 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{OUTPUTS}$ = 0 W

FPGA Fabric SRAM Dynamic Contribution—P_{MEMORY}

SoC Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

Where:

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-18 on page 2-18.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 2-18 on page 2-18.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

Standby Mode and Time Keeping Mode

P_{MEMORY} = 0 W

PLL/CCC Dynamic Contribution—P_{PLL}

SoC Mode

$P_{PLL} = P_{AC13} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Standby Mode and Time Keeping Mode

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

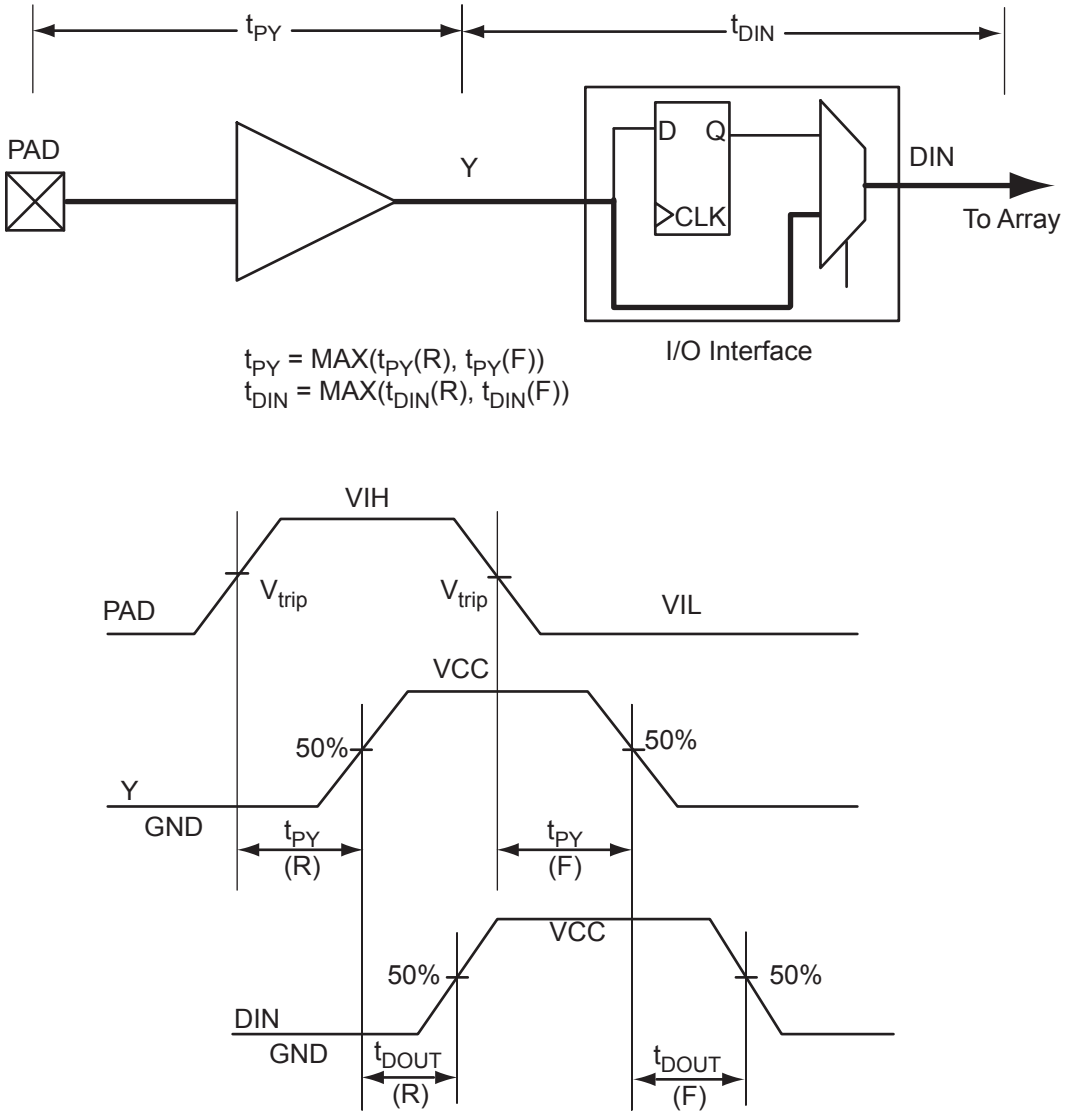


Figure 2-3 • **Input Buffer Timing Model and Delays (example)**

Timing Characteristics

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	7.20	0.04	0.97	0.39	7.34	6.18	2.52	2.46	9.39	8.23	ns
	–1	0.50	6.00	0.03	0.81	0.32	6.11	5.15	2.10	2.05	7.83	6.86	ns
8 mA	Std.	0.60	4.64	0.04	0.97	0.39	4.73	3.84	2.85	3.02	6.79	5.90	ns
	–1	0.50	3.87	0.03	0.81	0.32	3.94	3.20	2.37	2.52	5.65	4.91	ns
12 mA	Std.	0.60	3.37	0.04	0.97	0.39	3.43	2.67	3.07	3.39	5.49	4.73	ns
	–1	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
16 mA	Std.	0.60	3.18	0.04	0.97	0.39	3.24	2.43	3.11	3.48	5.30	4.49	ns
	–1	0.50	2.65	0.03	0.81	0.32	2.70	2.03	2.59	2.90	4.42	3.74	ns
24 mA	Std.	0.60	2.93	0.04	0.97	0.39	2.99	2.03	3.17	3.83	5.05	4.09	ns
	–1	0.50	2.45	0.03	0.81	0.32	2.49	1.69	2.64	3.19	4.21	3.41	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	9.75	0.04	0.97	0.39	9.93	8.22	2.52	2.31	11.99	10.28	ns
	–1	0.50	8.12	0.03	0.81	0.32	8.27	6.85	2.10	1.93	9.99	8.57	ns
8 mA	Std.	0.60	6.96	0.04	0.97	0.39	7.09	5.85	2.84	2.87	9.15	7.91	ns
	–1	0.50	5.80	0.03	0.81	0.32	5.91	4.88	2.37	2.39	7.62	6.59	ns
12 mA	Std.	0.60	5.35	0.04	0.97	0.39	5.45	4.58	3.06	3.23	7.51	6.64	ns
	–1	0.50	4.46	0.03	0.81	0.32	4.54	3.82	2.55	2.69	6.26	5.53	ns
16 mA	Std.	0.60	5.01	0.04	0.97	0.39	5.10	4.30	3.11	3.32	7.16	6.36	ns
	–1	0.50	4.17	0.03	0.81	0.32	4.25	3.58	2.59	2.77	5.97	5.30	ns
24 mA	Std.	0.60	4.67	0.04	0.97	0.39	4.75	4.28	3.16	3.66	6.81	6.34	ns
	–1	0.50	3.89	0.03	0.81	0.32	3.96	3.57	2.64	3.05	5.68	5.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-40 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.31	0.09	0.94	1.30	0.22	2.35	1.86	2.20	2.45	ns
	–1	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-41 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-42 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

2.5 V LVCMOS	VIL		V_{IH}		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max., mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

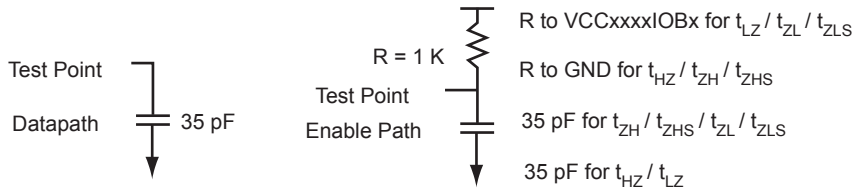


Figure 2-7 • AC Loading

Table 2-43 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

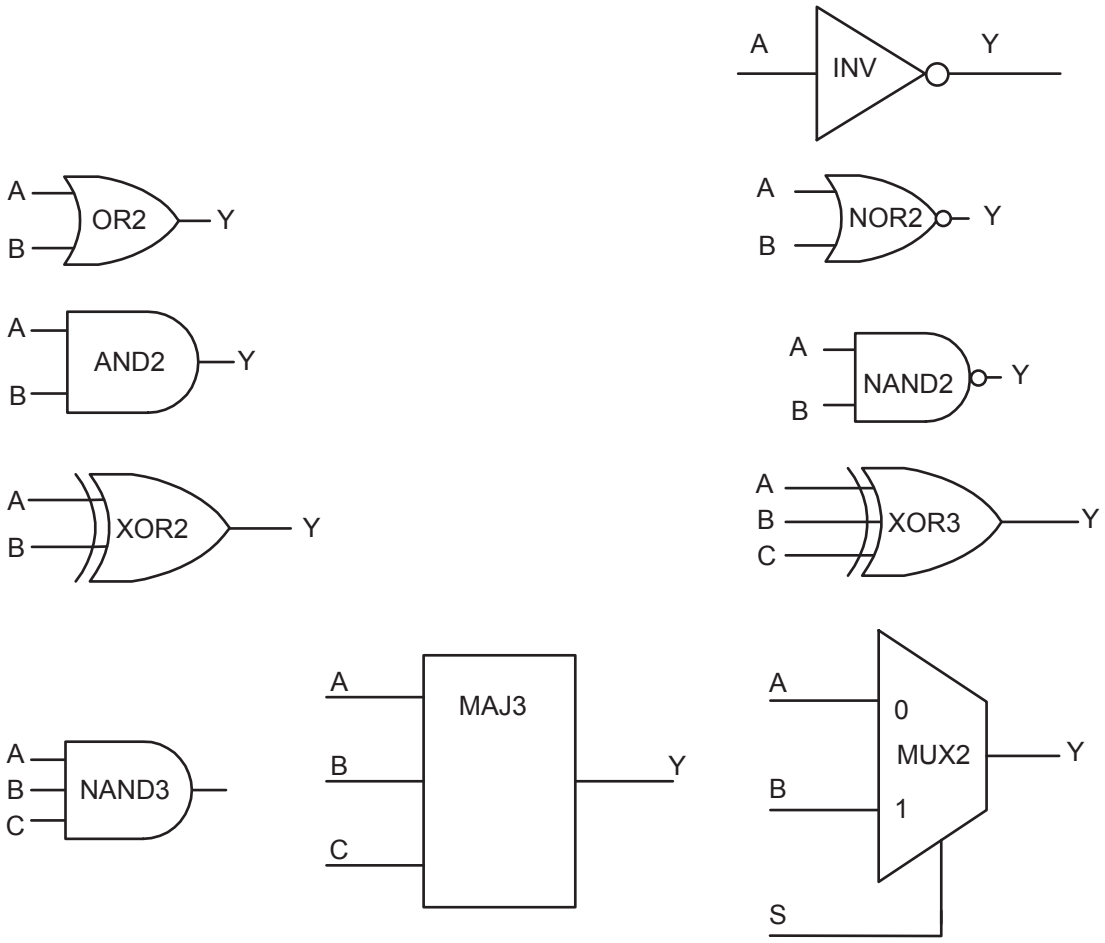


Figure 2-23 • **Sample of Combinatorial Cells**

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

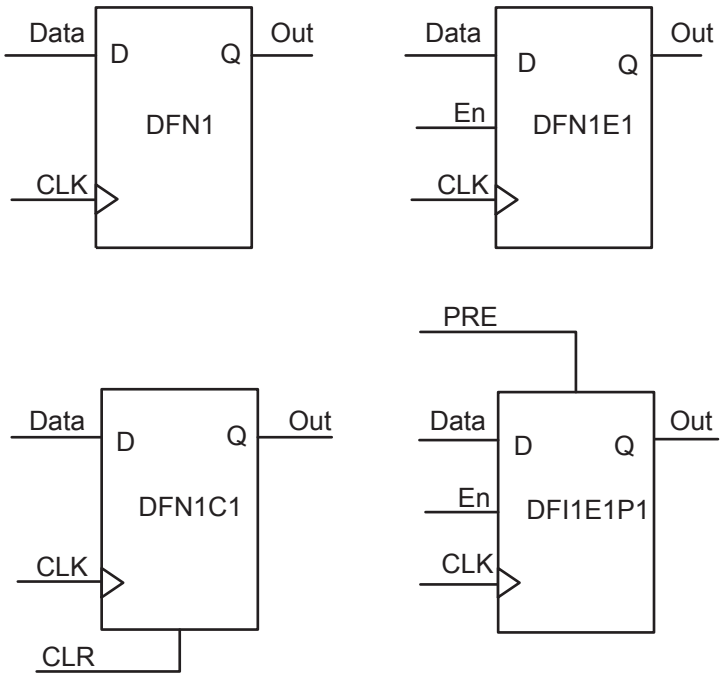


Figure 2-25 • Sample of Sequential Cells

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-96 • ABPS Performance Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

3 – SmartFusion Development Tools

Designing with SmartFusion cSoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity.

Types of Design Tools

Microsemi has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project (Figure 3-1).

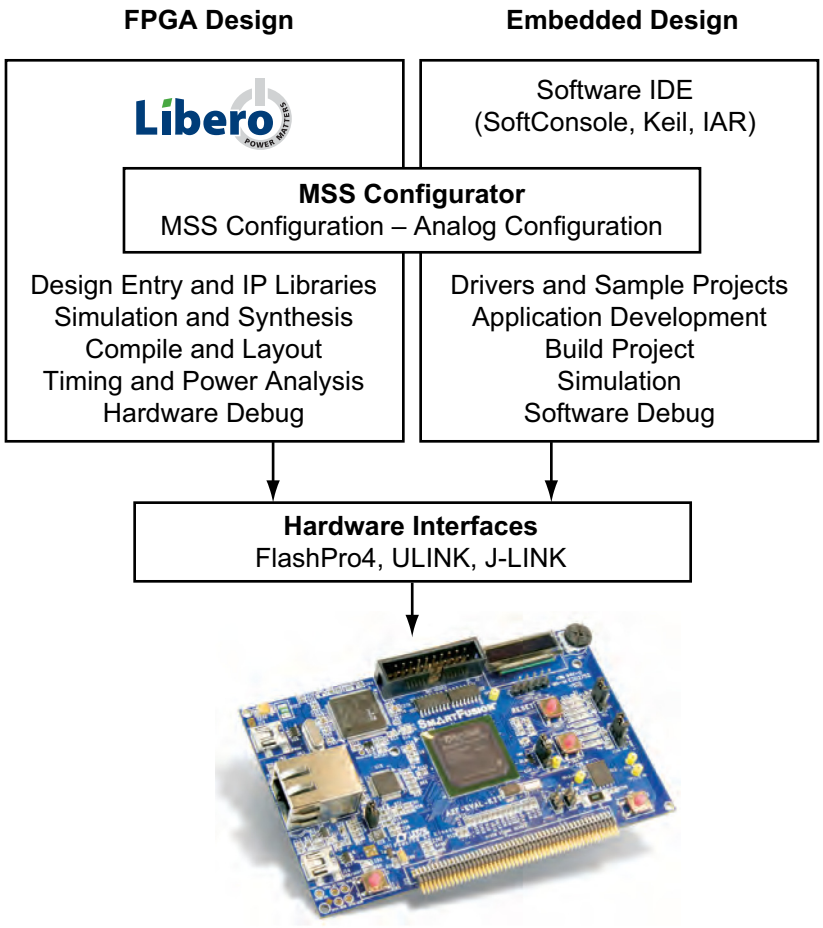


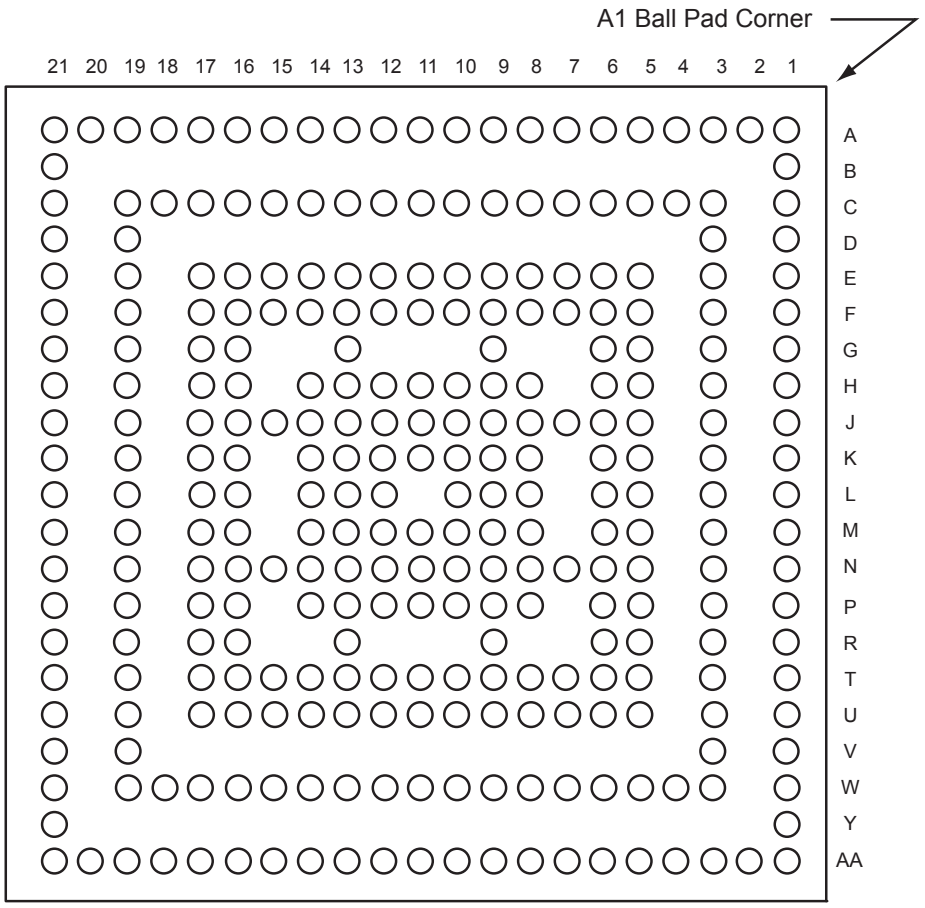
Figure 3-1 • **Three Design Roles**

FPGA Design

Libero System-on-Chip (SoC) software is Microsemi's comprehensive software toolset for designing with all Microsemi FPGAs and cSoCs. Libero SoC includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics®, as well as innovative timing and power optimization and analysis.

TQ144	
Pin Number	**A2F060 Function**
73	VCC33A
74	PTEM
75	PTBASE
76	SPI_0_DO/GPIO_16
77	SPI_0_DI/GPIO_17
78	SPI_0_CLK/GPIO_18
79	SPI_0_SS/GPIO_19
80	UART_0_RXD/GPIO_21
81	UART_0_TXD/GPIO_20
82	UART_1_RXD/GPIO_29
83	UART_1_TXD/GPIO_28
84	VCC
85	VCCMSSIOB2
86	GND
87	I2C_1_SDA/GPIO_30
88	I2C_1_SCL/GPIO_31
89	I2C_0_SDA/GPIO_22
90	I2C_0_SCL/GPIO_23
91	GNDENVM
92	VCCENVM
93	JTAGSEL
94	TCK
95	TDI
96	TMS
97	TDO
98	TRSTB
99	VJTAG
100	VDDBAT
101	VCCLPXTAL
102	LPXOUT
103	LPXIN
104	GNDLPXTAL
105	GNDMAINXTAL
106	MAINXOUT
107	MAINXIN
108	VCCMAINXTAL

CS288



Note: Bottom view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	PQ208	
	A2F200	A2F500
1	VCCPLL	VCCPLL0
2	VCOMPLA	VCOMPLA0
3	GNDQ	GNDQ
4	EMC_DB[15]/GAA2/IO71PDB5V0	GAA2/IO88PDB5V0
5	EMC_DB[14]/GAB2/IO71NDB5V0	GAB2/IO88NDB5V0
6	EMC_DB[13]/GAC2/IO70PDB5V0	GAC2/IO87PDB5V0
7	EMC_DB[12]/IO70NDB5V0	IO87NDB5V0
8	VCC	VCC
9	GND	GND
10	VCCFPGAIOB5	VCCFPGAIOB5
11	EMC_DB[11]/IO69PDB5V0	IO86PDB5V0
12	EMC_DB[10]/IO69NDB5V0	IO86NDB5V0
13	GFA2/IO68PSB5V0	GFA2/IO85PSB5V0
14	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0
15	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
16	EMC_DB[9]/GEC1/IO63PDB5V0	GEC1/IO80PDB5V0
17	EMC_DB[8]/GEC0/IO63NDB5V0	GEC0/IO80NDB5V0
18	EMC_DB[7]/GEB1/IO62PDB5V0	GEB1/IO79PDB5V0
19	EMC_DB[6]/GEB0/IO62NDB5V0	GEB0/IO79NDB5V0
20	EMC_DB[5]/GEA1/IO61PDB5V0	GEA1/IO78PDB5V0
21	EMC_DB[4]/GEA0/IO61NDB5V0	GEA0/IO78NDB5V0
22	VCC	VCC
23	GND	GND
24	VCCFPGAIOB5	VCCFPGAIOB5
25	EMC_DB[3]/GEC2/IO60PDB5V0	GEC2/IO77PDB5V0
26	EMC_DB[2]/IO60NDB5V0	IO77NDB5V0
27	EMC_DB[1]/GEB2/IO59PDB5V0	GEB2/IO76PDB5V0
28	EMC_DB[0]/GEA2/IO59NDB5V0	GEA2/IO76NDB5V0
29	VCC	VCC
30	GND	GND
31	GNDRCOSC	GNDRCOSC

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
156	GNDQ	GNDQ
157	GNDQ	GNDQ
158	VCCFPGAIOB0	VCCFPGAIOB0
159	GBA1/IO19PDB0V0	GBA1/IO23PDB0V0
160	GBA0/IO19NDB0V0	GBA0/IO23NDB0V0
161	VCCFPGAIOB0	VCCFPGAIOB0
162	GND	GND
163	VCC	VCC
164	EMC_AB[25]/IO16PDB0V0	IO21PDB0V0
165	EMC_AB[24]/IO16NDB0V0	IO21NDB0V0
166	EMC_AB[23]/IO15PDB0V0	IO20PDB0V0
167	EMC_AB[22]/IO15NDB0V0	IO20NDB0V0
168	EMC_AB[21]/IO14PDB0V0	IO19PDB0V0
169	EMC_AB[20]/IO14NDB0V0	IO19NDB0V0
170	EMC_AB[19]/IO13PDB0V0	IO18PDB0V0
171	EMC_AB[18]/IO13NDB0V0	IO18NDB0V0
172	EMC_AB[17]/IO12PDB0V0	IO17PDB0V0
173	EMC_AB[16]/IO12NDB0V0	IO17NDB0V0
174	VCCFPGAIOB0	VCCFPGAIOB0
175	GND	GND
176	VCC	VCC
177	EMC_AB[15]/IO11PDB0V0	IO14PDB0V0
178	EMC_AB[14]/IO11NDB0V0	IO14NDB0V0
179	EMC_AB[13]/IO10PDB0V0	IO13PDB0V0
180	EMC_AB[12]/IO10NDB0V0	IO13NDB0V0
181	EMC_AB[11]/IO09PDB0V0	IO12PDB0V0
182	EMC_AB[10]/IO09NDB0V0	IO12NDB0V0
183	EMC_AB[9]/IO08PDB0V0	IO11PDB0V0
184	EMC_AB[8]/IO08NDB0V0	IO11NDB0V0
185	EMC_AB[7]/IO07PDB0V0	IO10PDB0V0
186	EMC_AB[6]/IO07NDB0V0	IO10NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
187	VCCFPGAIOB0	VCCFPGAIOB0
188	GND	GND
189	VCC	VCC
190	EMC_AB[5]/IO06PDB0V0	IO08PDB0V0
191	EMC_AB[4]/IO06NDB0V0	IO08NDB0V0
192	EMC_AB[3]/IO05PDB0V0	GAC1/IO07PDB0V0
193	EMC_AB[2]/IO05NDB0V0	GAC0/IO07NDB0V0
194	EMC_AB[1]/IO04PDB0V0	IO04PDB0V0
195	EMC_AB[0]/IO04NDB0V0	IO04NDB0V0
196	EMC_OEN1_N/IO03PDB0V0	IO03PDB0V0
197	EMC_OEN0_N/IO03NDB0V0	IO03NDB0V0
198	EMC_BYTEN[1]/GAC1/IO02PDB0V0	GAA1/IO02PDB0V0
199	EMC_BYTEN[0]/GAC0/IO02NDB0V0	GAA0/IO02NDB0V0
200	VCCFPGAIOB0	VCCFPGAIOB0
201	GND	GND
202	VCC	VCC
203	EMC_CS1_N/GAB1/IO01PDB0V0	IO01PDB0V0
204	EMC_CS0_N/GAB0/IO01NDB0V0	IO01NDB0V0
205	EMC_RW_N/GAA1/IO00PDB0V0	IO00PDB0V0
206	EMC_CLK/GAA0/IO00NDB0V0	IO00NDB0V0
207	VCCFPGAIOB0	VCCFPGAIOB0
208	GNDQ	GNDQ

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
B16	GNDQ	GNDQ	GNDQ
C1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	VCCPLL0	VCCPLL	VCCPLL0
C3	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
C4	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C5	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
C6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
C7	GND	GND	GND
C8	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C9	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
C10	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C11	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C12	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C13	GND	GND	GND
C14	GCC0/IO18NPB0V0	GBA2/IO20PPB1V0	GBA2/IO27PPB1V0
C15	GCB0/IO19NDB0V0	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
C16	GCB1/IO19PDB0V0	IO23NDB1V0	IO28NDB1V0
D1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D2	VCOMPLA0	VCOMPLA	VCOMPLA0
D3	GND	GND	GND
D4	GNDQ	GNDQ	GNDQ
D5	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
D6	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
D7	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
D8	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
D9	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D10	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
D11	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
D12	GNDQ	GNDQ	GNDQ
D13	GCC1/IO18PPB0V0	GBB2/IO20NPB1V0	GBB2/IO27NPB1V0
D14	GCA0/IO20NDB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
B3	NC	NC
B4	NC	NC
B5	VCCFPGAIOB0	VCCFPGAIOB0
B6	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
B7	NC	IO04PPB0V0
B8	VCCFPGAIOB0	VCCFPGAIOB0
B9	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
B10	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B11	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
B12	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
B13	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
B14	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
B15	VCCFPGAIOB0	VCCFPGAIOB0
B16	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B17	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
B18	VCCFPGAIOB0	VCCFPGAIOB0
B19	GBB0/IO18NDB0V0	GBB0/IO24NDB0V0
B20	GBB1/IO18PDB0V0	GBB1/IO24PDB0V0
B21	GND	GND
B22	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
C1	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	NC	NC
C3	NC	NC
C4	NC	IO01NDB0V0
C5	NC	IO01PDB0V0
C6	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
C7	NC	IO03PPB0V0
C8	NC	IO04NPB0V0
C9	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
C10	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
C11	GND	GND
C12	VCCFPGAIOB0	VCCFPGAIOB0
C13	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C14	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
	The A2F060 device was added to product information tables.	N/A
	The "Product Ordering Codes" table was updated to removed Std. speed and add speed grade 1. Pre-production was removed from the application ordering code category.	VI
	The "SmartFusion cSoC Block Diagram" was revised.	IV
	The "Datasheet Categories" section was updated, referencing the "SmartFusion cSoC Block Diagram" table, which is new.	1-4, IV
	The "VCCI" parameter was renamed to "VCCxxxxIOBx." "Advanced I/Os" were renamed to "FPGA I/Os." Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREFx designates VAREF0, VAREF1, and VAREF2. Modes were renamed as follows: Operating mode was renamed to SoC mode. 32KHz Active mode was renamed to Standby mode. Battery mode was renamed to Time Keeping mode. Table entries have been filled with values as data has become available.	N/A
	Table 2-1 • Absolute Maximum Ratings, Table 2-2 • Analog Maximum Ratings, and Table 2-3 • Recommended Operating Conditions[5,6] were revised extensively.	2-1 through 2-3
	Device names were updated in Table 2-6 • Package Thermal Resistance.	2-7
	Table 2-8 • Power Supplies Configuration was revised extensively.	2-10
	Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings was revised extensively.	2-11
	Removed "Example of Power Calculation."	N/A
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs was revised extensively.	2-12
	Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs was revised extensively.	2-13
	The "Power Calculation Methodology" section was revised.	2-14
	Table 2-83 • Electrical Characteristics of the RC Oscillator was revised extensively.	2-61
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator was revised extensively.	2-62
	The parameter t_{RSTBQ} was changed to T_{C2CWRH} in Table 2-87 • RAM4K9.	2-69
	The 12-bit mode row for integral non-linearity was removed from Table 2-95 • ADC Specifications. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear.	2-81
	Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted.	N/A
	Table 2-99 • Voltage Regulator was revised extensively.	2-87
	The "Serial Peripheral Interface (SPI) Characteristics" section and "Inter-Integrated Circuit (I^2C) Characteristics" section are new.	2-89, 2-91