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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

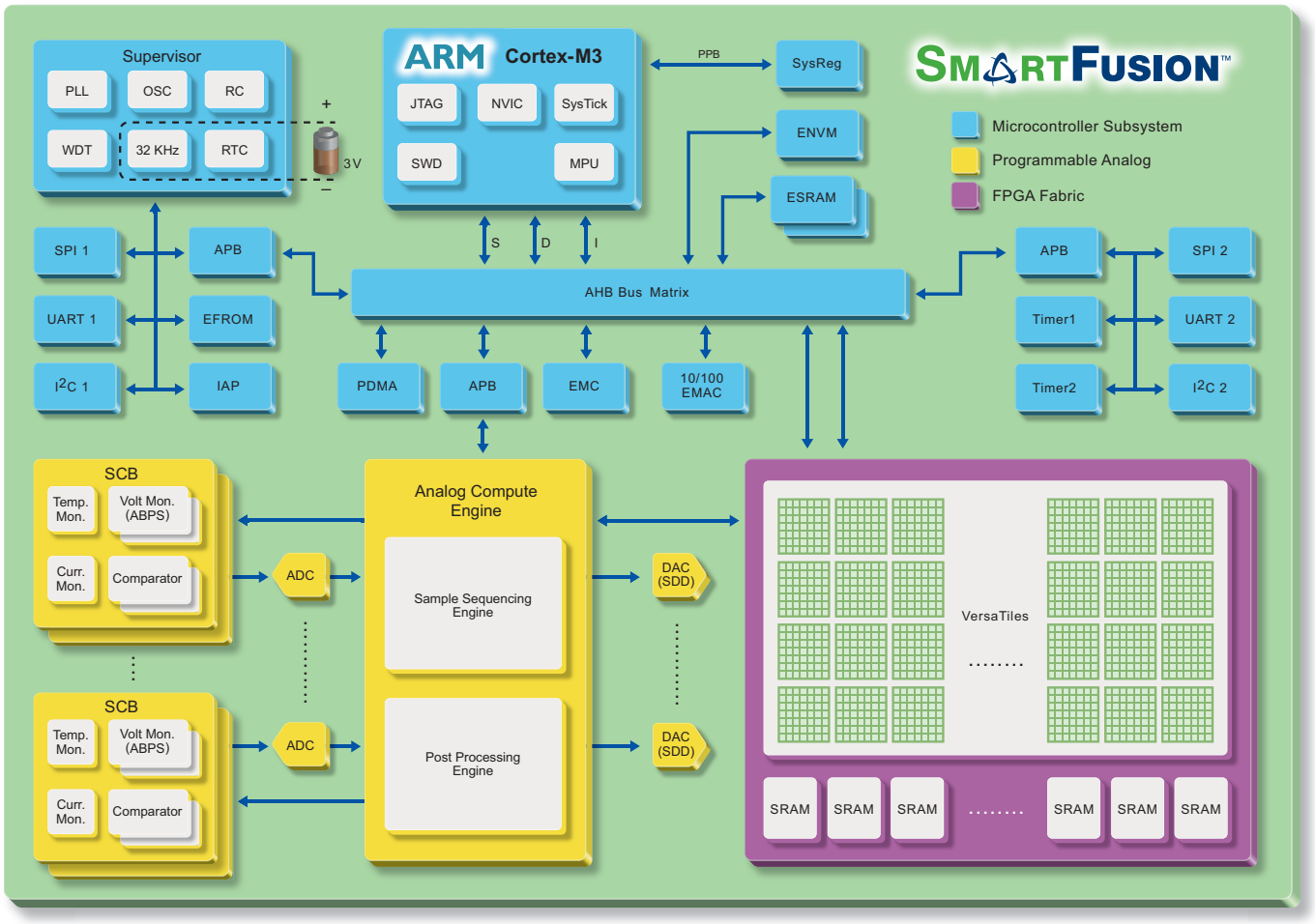
Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-1pq208i

SmartFusion cSoC Family Product Table

FPGA Fabric	A2F060			A2F200				A2F500			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
System Gates	60,000			200,000				500,000			
Tiles (D-flip-flops)	1,536			4,608				11,520			
RAM Blocks (4,608 bits)	8			8				24			
Microcontroller Subsystem (MSS)	**A2F060**			**A2F200**				**A2F500**			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Flash (Kbytes)	128			256				512			
SRAM (Kbytes)	16			64				64			
Cortex-M3 processor with MPU	Yes			Yes				Yes			
10/100 Ethernet MAC	No			Yes				Yes			
External Memory Controller (EMC)	–	26-/16-bit address/data		26-bit address,16-bit data				–	26-/16-bit address/data		
DMA	8 Ch			8 Ch				8 Ch			
I^2C	2			2				2			
SPI	1	2		1	2			1	2		
16550 UART	2			2				2			
32-Bit Timer	2			2				2			
PLL	1			1				1	2	1	2
32 KHz Low Power Oscillator	1			1				1			
100 MHz On-Chip RC Oscillator	1			1				1			
Main Oscillator (32 KHz to 20 MHz)	1			1				1			
Programmable Analog	**A2F060**			**A2F200**				**A2F500**			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
ADCs (8-/10-/12-bit SAR)	1			2				2			3
DACs (8-/16-/24-bit sigma-delta)	1			2				2			3
Signal Conditioning Blocks (SCBs)	1			4				4			5
Comparator*	2			8				8			10
Current Monitors*	1			4				4			5
Temperature Monitors*	1			4				4			5
Bipolar High Voltage Monitors*	2			8				8			10

*Note: *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130925 for details.*

SmartFusion cSoC Block Diagram



Legend:

SDD – Sigma-delta DAC
SCB – Signal conditioning block
PDMA – Peripheral DMA
IAP – In-application programming
ABPS – Active bipolar prescaler
WDT – Watchdog Timer
SWD – Serial Wire Debug

Power Consumption of Various Internal Resources

***Table 2-14* • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	3.39	3.40	5.05	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	1.14	1.83	2.50	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	1.15	1.15	1.15	µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.12	0.12	0.12	µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07	0.07	0.07	µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	1.04	0.79	0.79	µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11				
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11				
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00			µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00			µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60			µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00			µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88			mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80			µW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98			mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30			mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00			mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25			mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00			mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00			µW
PAC22	MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1]	VCC	1.5 V	67.50			mW
PAC23	Temperature Monitor Power Contribution	See Table 2-94 on page 2-79	–	1.23			mW

P_{PLL} = 0 W

Embedded Nonvolatile Memory Dynamic Contribution—P_{eNVM}

SoC Mode

The eNVM dynamic power consumption is a piecewise linear function of frequency.

$P_{eNVM} = N_{eNVM\text{-}BLOCKS} * \beta_4 * P_{AC15} * F_{READ\text{-}eNVM}$ when $F_{READ\text{-}eNVM} \leq 33$ MHz,

$P_{eNVM} = N_{eNVM\text{-}BLOCKS} * \beta_4 * (P_{AC16} + P_{AC17} * F_{READ\text{-}eNVM})$ when $F_{READ\text{-}eNVM} > 33$ MHz

Where:

$N_{eNVM\text{-}BLOCKS}$ is the number of eNVM blocks used in the design.

β_4 is the eNVM enable rate for read operations. Default is 0 (eNVM mainly in idle state).

$F_{READ\text{-}eNVM}$ is the eNVM read clock frequency.

Standby Mode and Time Keeping Mode

P_{eNVM} = 0 W

Main Crystal Oscillator Dynamic Contribution—$P_{XTL\text{-}OSC}$

SoC Mode

$P_{XTL\text{-}OSC} = P_{AC18}$

Standby Mode

$P_{XTL\text{-}OSC}$ = 0 W

Time Keeping Mode

$P_{XTL\text{-}OSC}$ = 0 W

Low Power Oscillator Crystal Dynamic Contribution—$P_{LPXTAL\text{-}OSC}$

Operating, Standby, and Time Keeping Mode

$P_{LPXTAL\text{-}OSC} = P_{AC21}$

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

SoC Mode

$P_{RC\text{-}OSC} = P_{AC19A} + P_{AC19B}$

Standby Mode and Time Keeping Mode

$P_{RC\text{-}OSC}$ = 0 W

Analog System Dynamic Contribution—P_{AB}

SoC Mode

$P_{AB} = P_{AC23} * N_{TM} + P_{AC24} * N_{CM} + P_{AC25} * N_{ABPS} + P_{AC26} * N_{SDD} + P_{AC27} * N_{COMP} + P_{ADC} * N_{ADC} + P_{VR}$

Where:

N_{CM} is the number of current monitor blocks

N_{TM} is the number of temperature monitor blocks

N_{SDD} is the number of sigma-delta DAC blocks

N_{ABPS} is the number of ABPS blocks

N_{ADC} is the number of ADC blocks

N_{COMP} is the number of comparator blocks

$P_{VR} = P_{AC28}$

$P_{ADC} = P_{AC20A} + P_{AC20B}$

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
2.5 V LVCMOS	12 mA	High	35	–	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
1.8 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
1.5 V LVCMOS	12 mA	High	35	–	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
3.3 V PCI	Per PCI spec	High	10	25[1]	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25[1]	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
LVDS	24 mA	High	–	–	0.50	1.53	0.03	1.55	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.50	1.46	0.03	1.46	–	–	–	–	–	–	–	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns
2.5 V LVCMOS	8 mA	High	10	–	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns
1.8 V LVCMOS	4 mA	High	10	–	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns
1.5 V LVCMOS	2 mA	High	10	–	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-41 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-42 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

2.5 V LVCMOS	VIL		V_{IH}		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max., mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

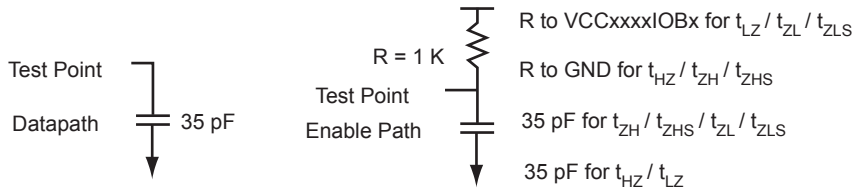


Figure 2-7 • AC Loading

Table 2-43 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-44 • 2.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	8.10	0.04	1.23	0.39	7.37	8.10	2.54	2.17	9.43	10.15	ns
	–1	0.46	6.75	0.03	1.03	0.32	6.14	6.75	2.12	1.81	7.85	8.46	ns
8 mA	Std.	0.55	4.85	0.04	1.23	0.39	4.76	4.85	2.90	2.83	6.82	6.91	ns
	–1	0.46	4.04	0.03	1.03	0.32	3.97	4.04	2.42	2.36	5.68	5.76	ns
12 mA	Std.	0.60	3.28	0.04	1.23	0.39	3.46	3.23	3.15	3.24	5.52	5.29	ns
	–1	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
16 mA	Std.	0.60	3.09	0.04	1.23	0.39	3.27	2.88	3.20	3.35	5.33	4.94	ns
	–1	0.50	2.57	0.03	1.03	0.32	2.72	2.40	2.67	2.79	4.44	4.12	ns
24 mA	Std.	0.60	2.95	0.04	1.23	0.39	3.01	2.31	3.27	3.76	5.07	4.37	ns
	–1	0.50	2.46	0.03	1.03	0.32	2.51	1.93	2.73	3.13	4.22	3.64	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-45 • 2.5 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	10.50	0.04	1.23	0.39	10.69	10.50	2.54	2.07	12.75	12.56	ns
	–1	0.46	8.75	0.03	1.03	0.32	8.91	8.75	2.12	1.73	10.62	10.47	ns
8 mA	Std.	0.55	7.61	0.04	1.23	0.39	7.46	7.19	2.81	2.66	9.52	9.25	ns
	–1	0.46	6.34	0.03	1.03	0.32	6.22	5.99	2.34	2.22	7.93	7.71	ns
12 mA	Std.	0.60	5.92	0.04	1.23	0.39	5.79	5.45	3.04	3.06	7.85	7.51	ns
	–1	0.50	4.93	0.03	1.03	0.32	4.83	4.54	2.53	2.55	6.54	6.26	ns
16 mA	Std.	0.60	5.53	0.04	1.23	0.39	5.40	5.09	3.09	3.16	7.46	7.14	ns
	–1	0.50	4.61	0.03	1.03	0.32	4.50	4.24	2.58	2.64	6.22	5.95	ns
24 mA	Std.	0.60	5.18	0.04	1.23	0.39	5.28	5.14	3.27	3.64	7.34	7.20	ns
	–1	0.50	4.32	0.03	1.03	0.32	4.40	4.29	2.72	3.03	6.11	6.00	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-46 • 2.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.35	0.09	1.18	1.39	0.22	2.40	2.18	2.19	2.32	ns
	–1	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Output Register

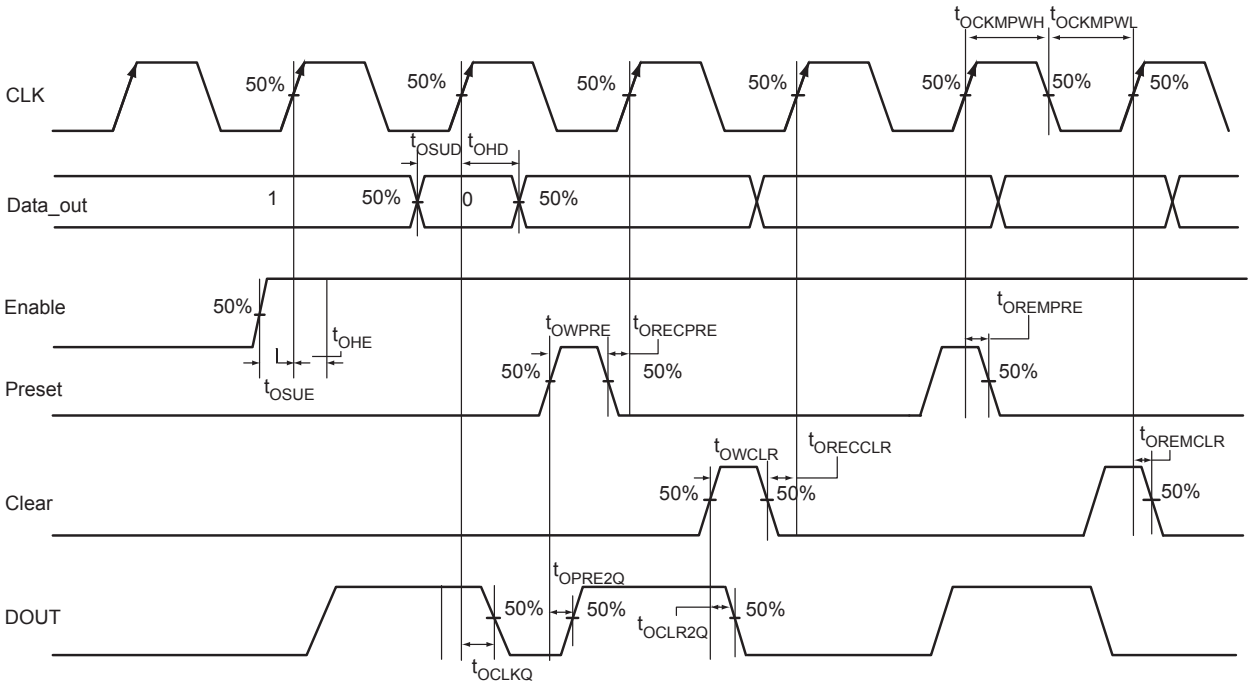


Figure 2-17 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-72 • **Output Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.72	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.38	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.98	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.98	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

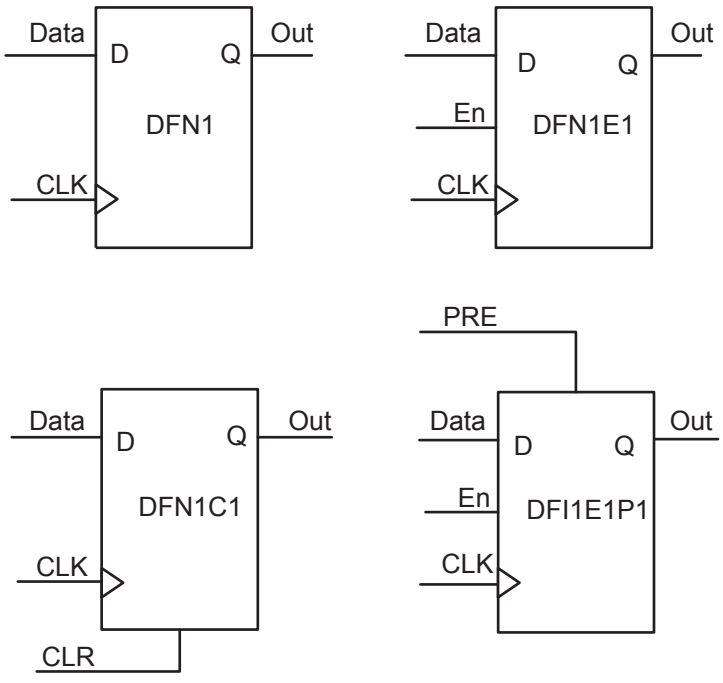


Figure 2-25 • Sample of Sequential Cells

Global Resource Characteristics

A2F200 Clock Tree Topology

Clock delays are device-specific. Figure 2-27 is an example of a global tree used for clock routing. The global tree presented in Figure 2-27 is driven by a CCC located on the west side of the A2F200 device. It is used to drive all D-flip-flops in the device.

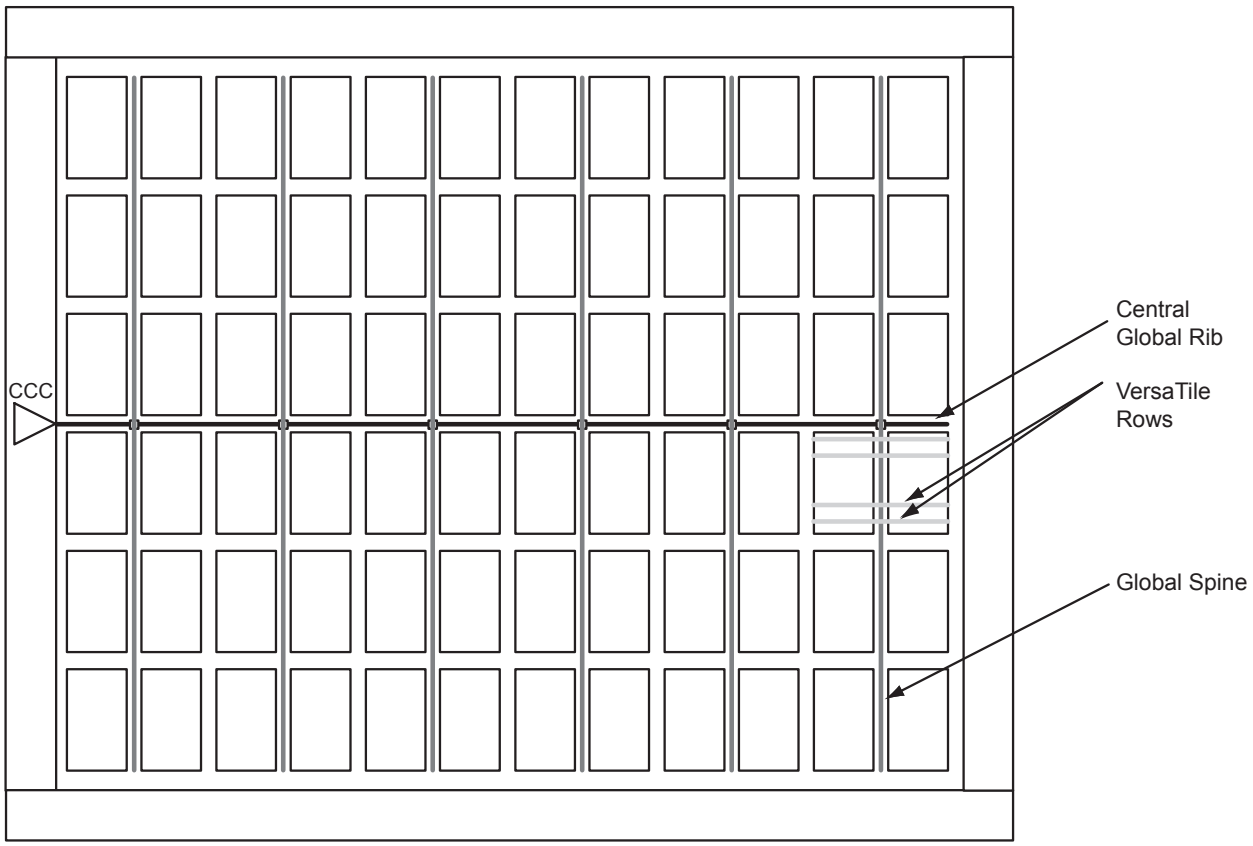
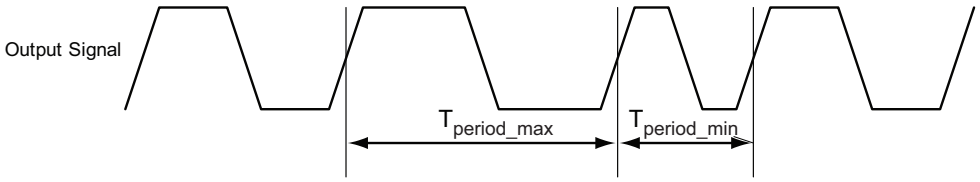


Figure 2-27 • **Example of Global Tree Use in an A2F200 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-63. Table 2-80 through Table 2-82 on page 2-61 present minimum and maximum global clock delays for the SmartFusion cSoCs. Minimum and maximum delays are measured with minimum and maximum loading.



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-28 • **Peak-to-Peak Jitter Definition**

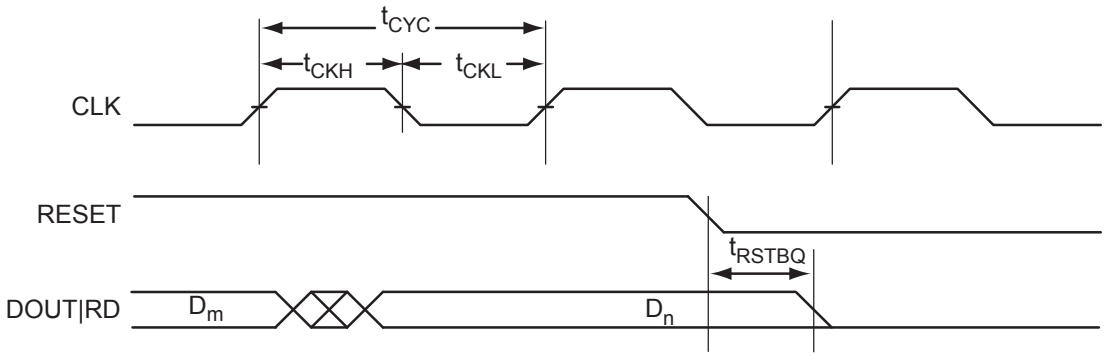


***Figure 2-34* • RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

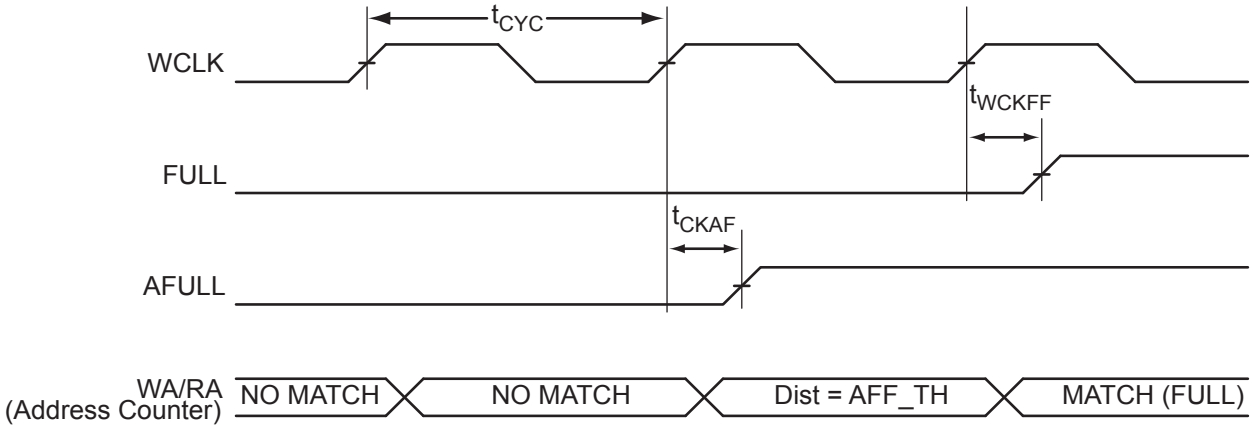


Figure 2-40 • **FIFO FULL Flag and AFULL Flag Assertion**

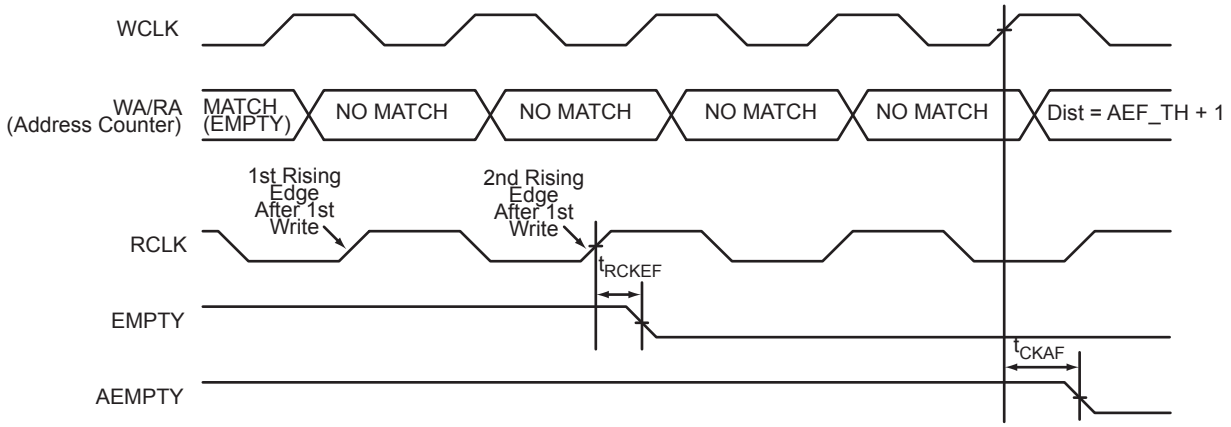


Figure 2-41 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

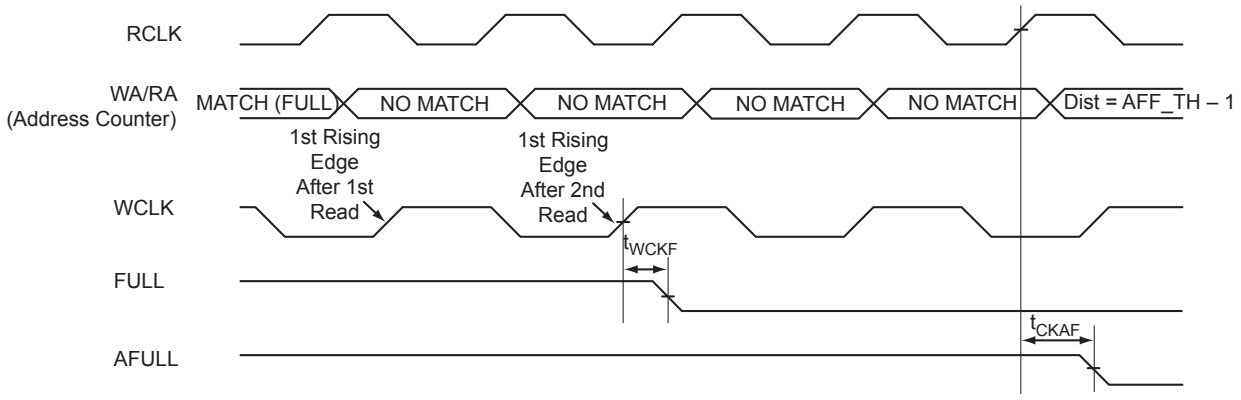


Figure 2-42 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Table 2-89 • FIFO
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.40	1.68	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.19	0.19	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.19	0.22	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.39	2.87	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.91	1.09	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.74	2.09	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.66	1.99	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	6.29	7.54	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.72	2.06	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.22	7.47	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to Data Out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET Recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.22	0.22	ns
t_{CYC}	Clock Cycle Time	3.28	3.28	ns
F_{MAX}	Maximum Frequency for FIFO	305	305	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Global I/O Naming Conventions

Gmn (Gxxx) refers to Global I/Os. These Global I/Os are used to connect the input to global networks. Global networks have high fanout and low skew. The naming convention for Global I/Os is as follows:

G = Global

m = Global pin location associated with each CCC on the device:

- A (northwest corner)
- B (northeast corner)
- C (east middle)
- D (southeast corner)
- E (southwest corner)
- F (west middle)

n = Global input MUX and pin number of the associated Global location m—A0, A1, A2, B0, B1, B2, C0, C1, or C2.

Global (GL) I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities.

Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the clocking resources chapter of the *SmartFusion FPGA Fabric User's Guide* and the clock conditioning circuitry chapter of the *SmartFusion Microcontroller Subsystem User's Guide*.

All inputs other than GC/GF are direct inputs into the quadrant clocks. The inputs to the global network are multiplexed, and only one input can be used as a global input. For example, if GAA0 is used as a quadrant global input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs other than GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. For more details, refer to the Global Input Selections section of the SmartFusion Fabric User Guide.

User Pins

Name	Type	Polarity/Bus Size	Description
GPIO_x	In/out	32	Microcontroller Subsystem (MSS) General Purpose I/O (GPIO). The MSS GPIO pin functions as an input, output, tristate, or bidirectional buffer with configurable interrupt generation and Schmitt trigger support. Input and output signal levels are compatible with the I/O standard selected. Unused GPIO pins are tristated and do not include pull-up or pull-down resistors. During power-up, the used GPIO pins are tristated with no pull-up or pull-down resistors until Sys boot configures them. Some of these pins are also multiplexed with integrated peripherals in the MSS (SPI, I^2C, and UART). These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices. GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. This allows GPIO pins to be multiplexed as either I/Os for the FPGA fabric, the ARM® Cortex-M3 or for given integrated MSS peripherals. The MSS peripherals are not multiplexed with each other; they are multiplexed only with the GPIO block. For more information, see the General Purpose I/O Block (GPIO) section in the *SmartFusion Microcontroller Subsystem User's Guide*.
IO	In/out		FPGA user I/O

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
F12	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
F13	GND	GND	GND
F14	GCB1/IO19PPB0V0	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
F15	GNDQ	GNDQ	GNDQ
F16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
F17	GCB0/IO19NPB0V0	IO24NDB1V0	IO33NDB1V0
F19	IO23NDB1V0	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
F21	GCA2/IO21PDB1V0	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
G1	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G3	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	NC	GFB1/IO65PDB5V0	GFB1/IO82PDB5V0
G6	EMC_DB[10]/IO43NDB5V0	EMC_DB[10]/IO69NDB5V0	EMC_DB[10]/IO86NDB5V0
G9	NC	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
G13	GCA0/IO20NPB0V0	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
G16	NC	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
G17	IO22NPB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
G19	GCC2/IO23PDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
G21	GND	GND	GND
H1	EMC_DB[9]/IO40PPB5V0	EMC_DB[9]/GEC1/IO63PPB5V0	EMC_DB[9]/GEC1/IO80PPB5V0
H3	GND	GND	GND
H5	NC	GFB0/IO65NDB5V0	GFB0/IO82NDB5V0
H6	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H8	GND	GND	GND
H9	VCC	VCC	VCC
H10	GND	GND	GND
H11	VCC	VCC	VCC
H12	GND	GND	GND
H13	VCC	VCC	VCC
H14	GND	GND	GND
H16	NC	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
H17	NC	GDC2/IO32PPB1V0	GDC2/IO41PPB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
M11	ADC6	TM2	TM2
M12	ADC5	CM2	CM2
M13	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
M14	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
M15	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
M16	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
N1	GPIO_8/IO25RSB4V0	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
N2	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
N3	VCC15A	VCC15A	VCC15A
N4	VCC33AP	VCC33AP	VCC33AP
N5	NC	ABPS3	ABPS3
N6	ADC4	TM1	TM1
N7	NC	GND33ADC0	GND33ADC0
N8	VCC33ADC0	VCC33ADC1	VCC33ADC1
N9	ADC8	ADC5	ADC5
N10	CM0	CM3	CM3
N11	GNDAQ	GNDAQ	GNDAQ
N12	VAREFOUT	VAREFOUT	VAREFOUT
N13	NC	GNDSDD1	GNDSDD1
N14	NC	VCC33SDD1	VCC33SDD1
N15	GND	GND	GND
N16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
P1	GNDSDD0	GNDSDD0	GNDSDD0
P2	VCC33SDD0	VCC33SDD0	VCC33SDD0
P3	VCC33N	VCC33N	VCC33N
P4	GNDA	GNDA	GNDA
P5	GNDAQ	GNDAQ	GNDAQ
P6	NC	CM1	CM1
P7	NC	ADC2	ADC2
P8	NC	VCC15ADC0	VCC15ADC0
P9	ADC9	ADC6	ADC6

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (January 2013)	The "SmartFusion cSoC Family Product Table" section has been updated to specify that External Memory Controller support for A2F060-TQ144 is not available (SAR 41555).	II
	The following Note was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 41027): "There are no LVTTL capable direct inputs available on A2F060 devices."	III
	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43218).	VI
	Added a note to Table 2-3 • Recommended Operating Conditions[5,6] (SAR 43428): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-3
	Statements about the state of the I/Os during programming were updated in the following sections: "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" and "User I/O Naming Conventions" (SAR 43380).	2-4, 5-7
	In Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits, the upper value of temperature ranges was corrected from "Min." to "Max." (SAR 41826).	2-4
	Information for A2F200M3F-CS288 was added to Table 2-6 • Package Thermal Resistance. The die size column was removed (SARs 41828, 42168). Also added details for A2F200M3F-PQG208I (SAR 35728).	2-7
	Added the following note to Table 2-65 • LVDS and Table 2-68 • LVPECL: "The above mentioned timing parameters correspond to 24mA drive strength." (SAR 43457)	2-41, 2-43
	The note in Table 2-86 • SmartFusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 34816).	2-63
	The SRAM collision data in Table 2-87 • RAM4K9 and Table 2-88 • RAM512X18 was updated (SAR 38583).	2-69,2-70
	The maximum input bias current for comparators 1, 3, 5, 7, and 9, in Table 2-97 • Comparator Performance Specifications, was revised from 60 to 100 nA (SAR 36008).	2-84