Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-cs288

1 – SmartFusion Family Overview

Introduction

The SmartFusion® family of cSoCs builds on the technology first introduced with the Fusion mixed signal FPGAs. SmartFusion cSoCs are made possible by integrating FPGA technology with programmable high-performance analog and hardened ARM Cortex-M3 microcontroller blocks on a flash semiconductor process. The SmartFusion cSoC takes its name from the fact that these three discrete technologies are integrated on a single chip, enabling the lowest cost of ownership and smallest footprint solution to you.

General Description

Microcontroller Subsystem (MSS)

The MSS is composed of a 100 MHz Cortex-M3 processor and integrated peripherals, which are interconnected via a multi-layer AHB bus matrix (ABM). This matrix allows the Cortex-M3 processor, FPGA fabric master, Ethernet media access controller (MAC), when available, and peripheral DMA (PDMA) controller to act as masters to the integrated peripherals, FPGA fabric, embedded nonvolatile memory (eNVM), embedded synchronous RAM (eSRAM), external memory controller (EMC), and analog compute engine (ACE) blocks.

SmartFusion cSoCs of different densities offer various sets of integrated peripherals. Available peripherals include SPI, I^2C, and UART serial ports, embedded FlashROM (EFROM), 10/100 Ethernet MAC, timers, phase-locked loops (PLLs), oscillators, real-time counters (RTC), and peripheral DMA controller (PDMA).

Programmable Analog

Analog Front-End (AFE)

SmartFusion cSoCs offer an enhanced analog front-end compared to Fusion devices. The successive approximation register analog-to-digital converters (SAR ADC) are similar to those found on Fusion devices. SmartFusion cSoC also adds first order sigma-delta digital-to-analog converters (SDD DAC).

SmartFusion cSoCs can handle multiple analog signals simultaneously with its signal conditioning blocks (SCBs). SCBs are made of a combination of active bipolar prescalers (ABPS), comparators, current monitors and temperature monitors. ABPS modules allow larger bipolar voltages to be fed to the ADC. Current monitors take the voltage across an external sense resistor and convert it to a voltage suitable for the ADC input range. Similarly, the temperature monitor reads the current through an external PN-junction (diode or transistor) and converts it internally for the ADC. The SCB also includes comparators to monitor fast signal thresholds without using the ADC. The output of the comparators can be fed to the analog compute engine or the ADC.

Analog Compute Engine (ACE)

The mixed signal blocks found in SmartFusion cSoCs are controlled and connected to the rest of the system via a dedicated processor called the analog compute engine (ACE). The role of the ACE is to offload control of the analog blocks from the Cortex-M3, thus offering faster throughput or better power consumption compared to a system where the main processor is in charge of monitoring the analog resources. The ACE is built to handle sampling, sequencing, and post-processing of the ADCs, DACs, and SCBs.

Table 2-2 • **Analog Maximum Ratings**

Parameter	Conditions	Min.	Max.	Units
ABPS[n] pad voltage (relative to ground)	GDEC[1:0] = 00 (±15.36 V range)			
	Absolute maximum	–11.5	14.4	V
	Recommended	–11	14	V
	GDEC[1:0] = 01 (±10.24 V range)	–11.5	12	V
	GDEC[1:0] = 10 (±5.12 V range)	–6	6	V
	GDEC[1:0] = 11 (±2.56 V range)	–3	3	V
CM[n] pad voltage relative to ground)	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 0 (comparator off, for the associated even-numbered comparator)			
	Absolute maximum	–0.3	14.4	V
	Recommended	–0.3	14	V
	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
TM[n] pad voltage (relative to ground)	TMB_DI_ON = 0 (ADC isolated) COMP_EN = 1(comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
ADC[n] pad voltage (relative to ground)		–0.3	3.6	V

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 85°C, worst-case VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.425	0.86	0.91	0.93	0.98	1.00	1.02
1.500	0.81	0.86	0.88	0.93	0.95	0.96
1.575	0.78	0.83	0.85	0.90	0.91	0.93

Detailed I/O DC Characteristics

***Table 2-26* • Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

***Table 2-27* • I/O Output Buffer Maximum Resistances[1]**
Applicable to FPGA I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website (also generated by the SoC Products Group Libero SoC toolset).*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-47 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	16	16	74	91	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

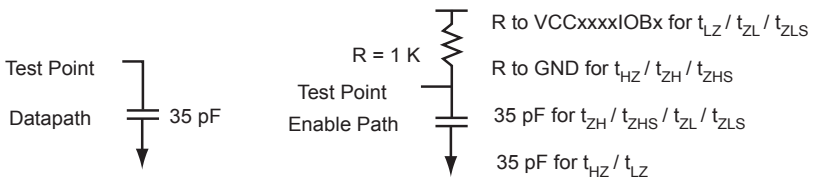

Figure 2-8 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Input Register

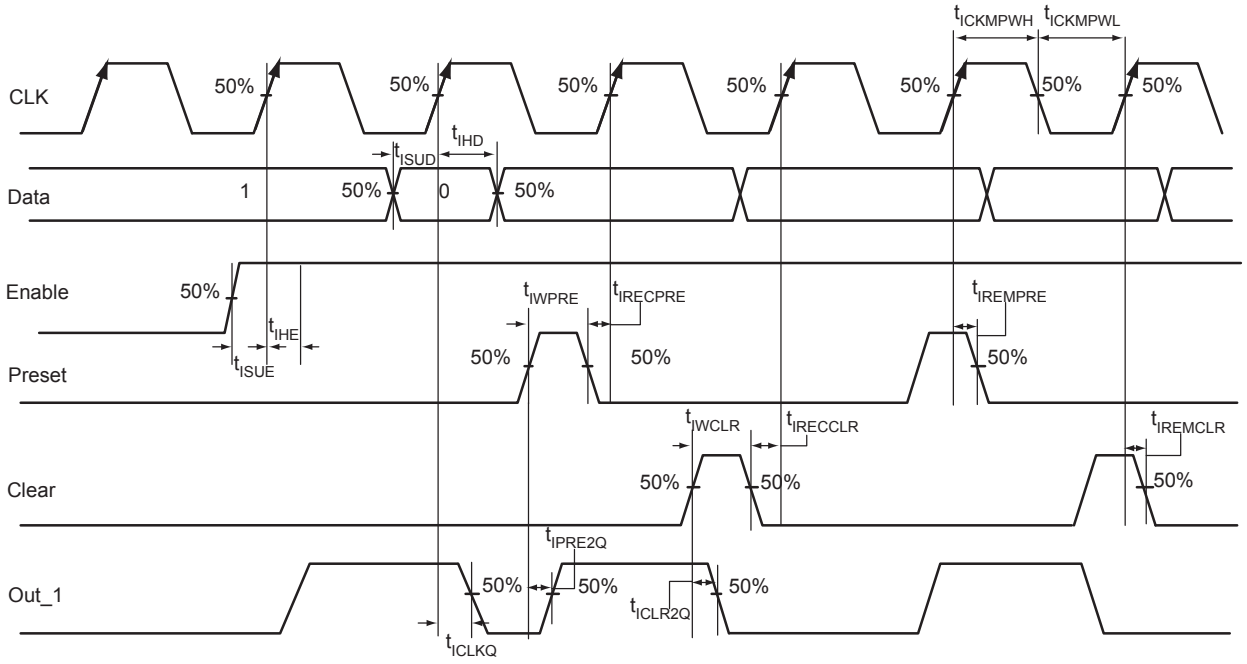

Figure 2-16 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-71 • **Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.55	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.55	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

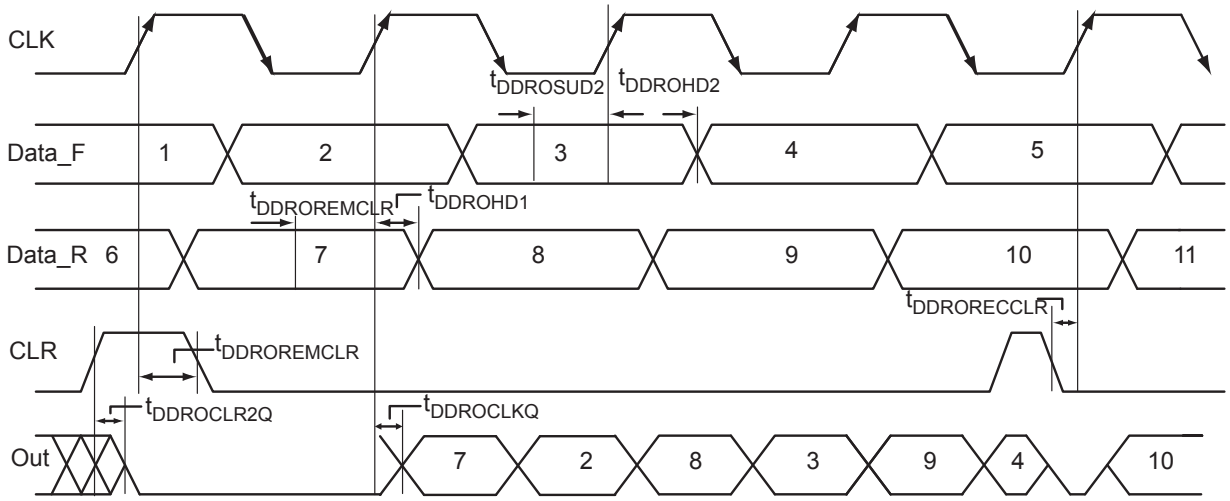

Figure 2-22 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-77 • **Output DDR Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.71	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.81	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

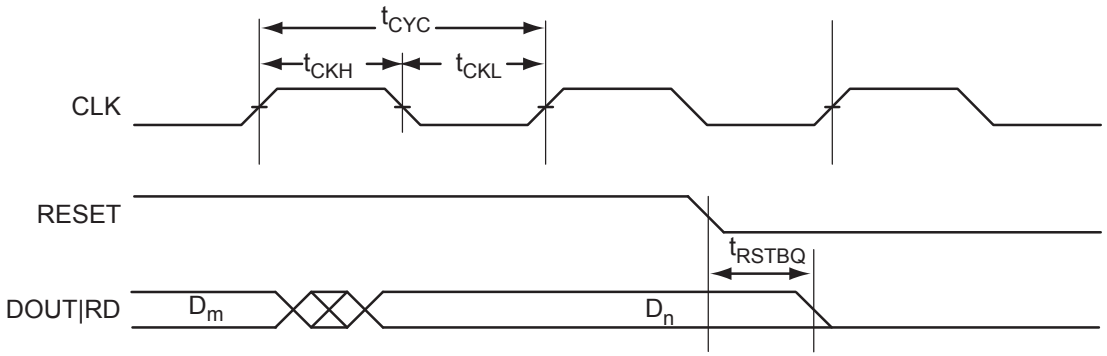

***Figure 2-34* • RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

Timing Waveforms

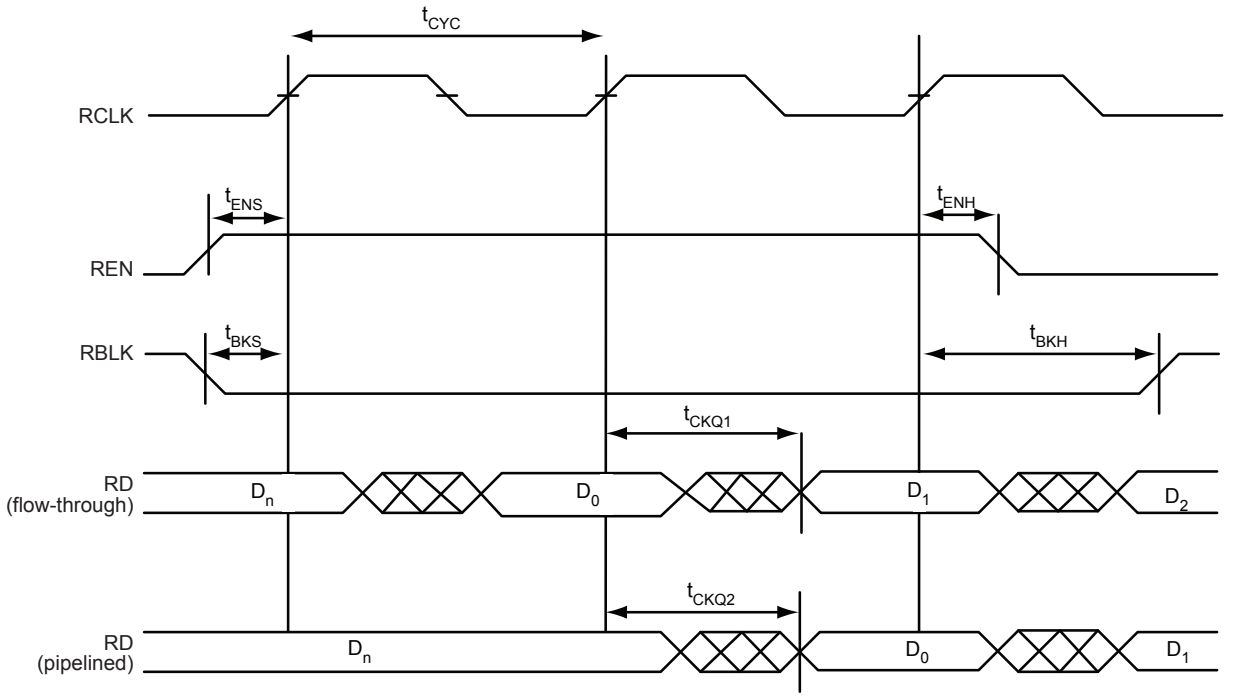

Figure 2-36 • **FIFO Read**

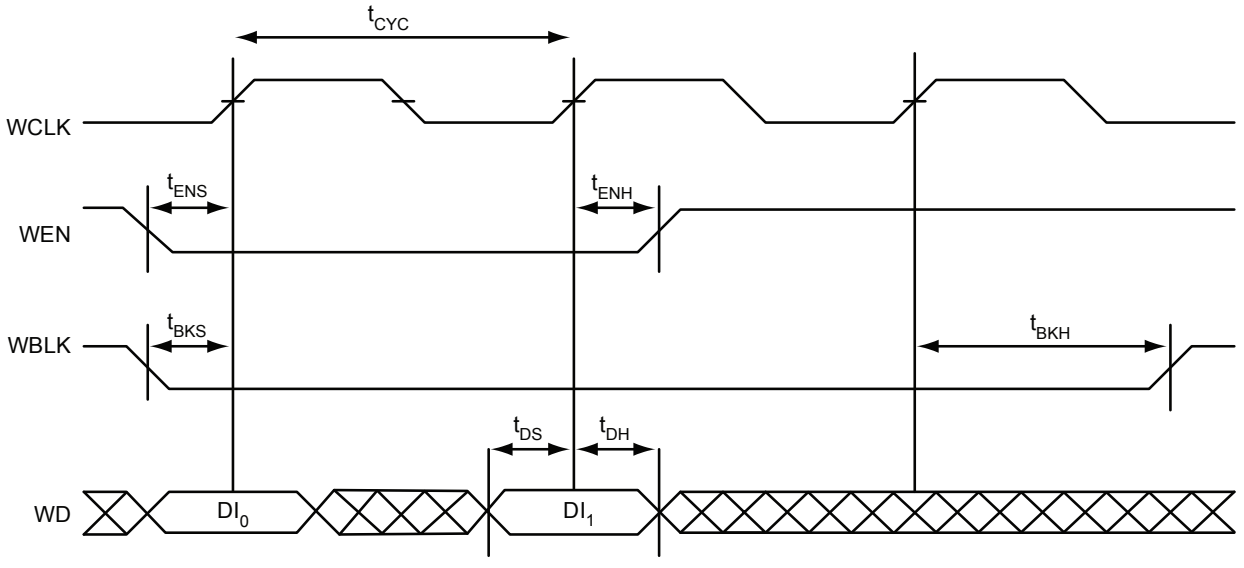

Figure 2-37 • **FIFO Write**

***Table 2-96* • ABPS Performance Specifications (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input referred offset voltage					
	GDEC[1:0] = 11	–0.31	–0.07	0.31	% FS*
	–40ºC to +100ºC	–1.00		1.47	% FS*
	GDEC[1:0] = 10	–0.34	–0.07	0.34	% FS*
	–40ºC to +100ºC	–0.90		1.37	% FS*
	GDEC[1:0] = 01	–0.61	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.05		1.35	% FS*
	GDEC[1:0] = 00	–0.39	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.06		1.38	% FS*
SINAD		53	56		dB
Non-linearity	RMS deviation from BFSL			0.5	% FS*
Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 11*	GDEC[1:0] = 11 (±2.56 range), –1 dBFS input				
	12-bit mode 10 KHz	8.6	9.1		Bits
	12-bit mode 100 KHz	8.6	9.1		Bits
	10-bit mode 10 KHz	8.5	8.9		Bits
	10-bit mode 100 KHz	8.5	8.9		Bits
	8-bit mode 10 KHz	7.7	7.8		Bits
	8-bit mode 100 KHz	7.7	7.8		Bits
Large-signal bandwidth	–1 dBFS input		1		MHz
Analog settling time	To 0.1% of final value (with ADC load)			10	µs
Input resistance			1		MΩ
Power supply rejection ratio	DC (0–1 KHz)	38	40		dB
ABPS power supply current requirements (not including ADC or VAREFx)	ABPS_EN = 1 (operational mode)				
	VCC33A		123	134	µA
	VCC33AP		89	94	µA
	VCC15A		1		µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Comparator

Unless otherwise specified, performance is specified at 25°C with nominal power supply voltages.

***Table 2-97* • Comparator Performance Specifications**

Specification	Test Conditions		Min.	Typ.	Max.	Units
Input voltage range	Minimum			0		V
	Maximum			2.56		V
Input offset voltage	HYS[1:0] = 00 (no hysteresis)			±1	±3	mV
Input bias current	Comparator 1, 3, 5, 7, 9 (measured at 2.56 V)			40	100	nA
	Comparator 0, 2, 4, 6, 8 (measured at 2.56 V)			150	300	nA
Input resistance			10			MΩ
Power supply rejection ratio	DC (0 – 10 KHz)		50	60		dB
Propagation delay	100 mV overdrive					
	HYS[1:0] = 00					
	(no hysteresis)			15	18	ns
	100 mV overdrive					
	HYS[1:0] = 10					
	(with hysteresis)			25	30	ns
Hysteresis (± refers to rising and falling threshold shifts, respectively)	HYS[1:0] = 00	Typical (25°C)	0	0	±5	mV
		Across all corners (–40ºC to +100ºC)	0		±5	mV
	HYS[1:0] = 01	Typical (25°C)	±3	± 16	±30	mV
		Across all corners (–40ºC to +100ºC)	0		±36	mV
	HYS[1:0] = 10	Typical (25°C)	±19	± 31	±48	mV
		Across all corners (–40ºC to +100ºC)	±12		±54	mV
	HYS[1:0] = 11	Typical (25°C)	±80	± 105	±190	mV
		Across all corners (–40ºC to +100ºC)	±80		±194	mV
Comparator current requirements (per comparator)	VCC33A = 3.3 V (operational mode); COMP_EN = 1					
	VCC33A			150	165	µA
	VCC33AP			140	165	µA
	VCC15A			1	3	µA

SmartFusion Ecosystem

The Microsemi SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in Figure 3-3.

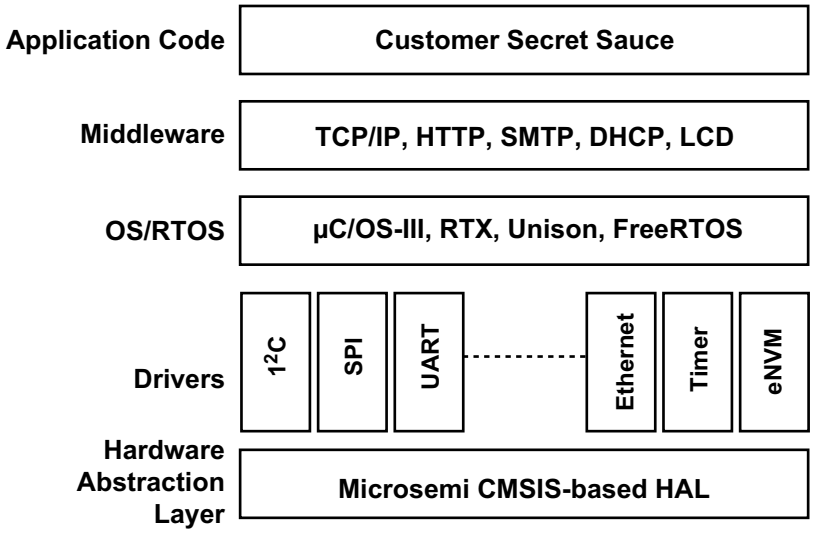

Figure 3-3 • **SmartFusion Ecosystem**

Figure 3-3 shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

ARM

Because an ARM processor was chosen for SmartFusion cSoCs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers* White Paper

Global I/O Naming Conventions

Gmn (Gxxx) refers to Global I/Os. These Global I/Os are used to connect the input to global networks. Global networks have high fanout and low skew. The naming convention for Global I/Os is as follows:

G = Global

m = Global pin location associated with each CCC on the device:

- A (northwest corner)
- B (northeast corner)
- C (east middle)
- D (southeast corner)
- E (southwest corner)
- F (west middle)

n = Global input MUX and pin number of the associated Global location m—A0, A1, A2, B0, B1, B2, C0, C1, or C2.

Global (GL) I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities.

Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the clocking resources chapter of the *SmartFusion FPGA Fabric User's Guide* and the clock conditioning circuitry chapter of the *SmartFusion Microcontroller Subsystem User's Guide*.

All inputs other than GC/GF are direct inputs into the quadrant clocks. The inputs to the global network are multiplexed, and only one input can be used as a global input. For example, if GAA0 is used as a quadrant global input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs other than GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. For more details, refer to the Global Input Selections section of the SmartFusion Fabric User Guide.

User Pins

Name	Type	Polarity/Bus Size	Description
GPIO_x	In/out	32	Microcontroller Subsystem (MSS) General Purpose I/O (GPIO). The MSS GPIO pin functions as an input, output, tristate, or bidirectional buffer with configurable interrupt generation and Schmitt trigger support. Input and output signal levels are compatible with the I/O standard selected. Unused GPIO pins are tristated and do not include pull-up or pull-down resistors. During power-up, the used GPIO pins are tristated with no pull-up or pull-down resistors until Sys boot configures them. Some of these pins are also multiplexed with integrated peripherals in the MSS (SPI, I^2C, and UART). These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices. GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. This allows GPIO pins to be multiplexed as either I/Os for the FPGA fabric, the ARM® Cortex-M3 or for given integrated MSS peripherals. The MSS peripherals are not multiplexed with each other; they are multiplexed only with the GPIO block. For more information, see the General Purpose I/O Block (GPIO) section in the *SmartFusion Microcontroller Subsystem User's Guide*.
IO	In/out		FPGA user I/O

PQ208

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	PQ208	
	A2F200	A2F500
1	VCCPLL	VCCPLL0
2	VCOMPLA	VCOMPLA0
3	GNDQ	GNDQ
4	EMC_DB[15]/GAA2/IO71PDB5V0	GAA2/IO88PDB5V0
5	EMC_DB[14]/GAB2/IO71NDB5V0	GAB2/IO88NDB5V0
6	EMC_DB[13]/GAC2/IO70PDB5V0	GAC2/IO87PDB5V0
7	EMC_DB[12]/IO70NDB5V0	IO87NDB5V0
8	VCC	VCC
9	GND	GND
10	VCCFPGAIOB5	VCCFPGAIOB5
11	EMC_DB[11]/IO69PDB5V0	IO86PDB5V0
12	EMC_DB[10]/IO69NDB5V0	IO86NDB5V0
13	GFA2/IO68PSB5V0	GFA2/IO85PSB5V0
14	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0
15	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
16	EMC_DB[9]/GEC1/IO63PDB5V0	GEC1/IO80PDB5V0
17	EMC_DB[8]/GEC0/IO63NDB5V0	GEC0/IO80NDB5V0
18	EMC_DB[7]/GEB1/IO62PDB5V0	GEB1/IO79PDB5V0
19	EMC_DB[6]/GEB0/IO62NDB5V0	GEB0/IO79NDB5V0
20	EMC_DB[5]/GEA1/IO61PDB5V0	GEA1/IO78PDB5V0
21	EMC_DB[4]/GEA0/IO61NDB5V0	GEA0/IO78NDB5V0
22	VCC	VCC
23	GND	GND
24	VCCFPGAIOB5	VCCFPGAIOB5
25	EMC_DB[3]/GEC2/IO60PDB5V0	GEC2/IO77PDB5V0
26	EMC_DB[2]/IO60NDB5V0	IO77NDB5V0
27	EMC_DB[1]/GEB2/IO59PDB5V0	GEB2/IO76PDB5V0
28	EMC_DB[0]/GEA2/IO59NDB5V0	GEA2/IO76NDB5V0
29	VCC	VCC
30	GND	GND
31	GNDRCOSC	GNDRCOSC

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
A1	GND	GND
A2	NC	NC
A3	NC	NC
A4	GND	GND
A5	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
A6	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
A7	GND	GND
A8	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A9	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A10	GND	GND
A11	NC	NC
A12	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
A13	GND	GND
A14	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
A15	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
A16	GND	GND
A17	NC	IO16NDB0V0
A18	NC	IO16PDB0V0
A19	GND	GND
A20	NC	NC
A21	NC	NC
A22	GND	GND
AA1	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
AA2	GPIO_12/IO37RSB4V0	GPIO_12/IO46RSB4V0
AA3	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
AA4	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
AA5	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
AA6	ABPS0	ABPS0
AA7	TM1	TM1
AA8	ADC1	ADC1
AA9	GND15ADC1	GND15ADC1
AA10	GND33ADC1	GND33ADC1
AA11	CM3	CM3
AA12	GNDTM1	GNDTM1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
Y15	NC	VCC15ADC2
Y16	VCCMAINXTAL	VCCMAINXTAL
Y17	SDD1	SDD1
Y18	PTEM	PTEM
Y19	VCC33A	VCC33A
Y20	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
Y21	VCCMSSIOB2	VCCMSSIOB2
Y22	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (January 2013)	The "SmartFusion cSoC Family Product Table" section has been updated to specify that External Memory Controller support for A2F060-TQ144 is not available (SAR 41555).	II
	The following Note was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 41027): "There are no LVTTL capable direct inputs available on A2F060 devices."	III
	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43218).	VI
	Added a note to Table 2-3 • Recommended Operating Conditions[5,6] (SAR 43428): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-3
	Statements about the state of the I/Os during programming were updated in the following sections: "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" and "User I/O Naming Conventions" (SAR 43380).	2-4, 5-7
	In Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits, the upper value of temperature ranges was corrected from "Min." to "Max." (SAR 41826).	2-4
	Information for A2F200M3F-CS288 was added to Table 2-6 • Package Thermal Resistance. The die size column was removed (SARs 41828, 42168). Also added details for A2F200M3F-PQG208I (SAR 35728).	2-7
	Added the following note to Table 2-65 • LVDS and Table 2-68 • LVPECL: "The above mentioned timing parameters correspond to 24mA drive strength." (SAR 43457)	2-41, 2-43
	The note in Table 2-86 • SmartFusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 34816).	2-63
	The SRAM collision data in Table 2-87 • RAM4K9 and Table 2-88 • RAM512X18 was updated (SAR 38583).	2-69,2-70
	The maximum input bias current for comparators 1, 3, 5, 7, and 9, in Table 2-97 • Comparator Performance Specifications, was revised from 60 to 100 nA (SAR 36008).	2-84

Revision	Changes	Page
	The A2F060 device was added to product information tables.	N/A
	The "Product Ordering Codes" table was updated to removed Std. speed and add speed grade 1. Pre-production was removed from the application ordering code category.	VI
	The "SmartFusion cSoC Block Diagram" was revised.	IV
	The "Datasheet Categories" section was updated, referencing the "SmartFusion cSoC Block Diagram" table, which is new.	1-4, IV
	The "VCCI" parameter was renamed to "VCCxxxxIOBx." "Advanced I/Os" were renamed to "FPGA I/Os." Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREFx designates VAREF0, VAREF1, and VAREF2. Modes were renamed as follows: Operating mode was renamed to SoC mode. 32KHz Active mode was renamed to Standby mode. Battery mode was renamed to Time Keeping mode. Table entries have been filled with values as data has become available.	N/A
	Table 2-1 • Absolute Maximum Ratings, Table 2-2 • Analog Maximum Ratings, and Table 2-3 • Recommended Operating Conditions[5,6] were revised extensively.	2-1 through 2-3
	Device names were updated in Table 2-6 • Package Thermal Resistance.	2-7
	Table 2-8 • Power Supplies Configuration was revised extensively.	2-10
	Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings was revised extensively.	2-11
	Removed "Example of Power Calculation."	N/A
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs was revised extensively.	2-12
	Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs was revised extensively.	2-13
	The "Power Calculation Methodology" section was revised.	2-14
	Table 2-83 • Electrical Characteristics of the RC Oscillator was revised extensively.	2-61
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator was revised extensively.	2-62
	The parameter t_{RSTBQ} was changed to T_{C2CWRH} in Table 2-87 • RAM4K9.	2-69
	The 12-bit mode row for integral non-linearity was removed from Table 2-95 • ADC Specifications. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear.	2-81
	Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted.	N/A
	Table 2-99 • Voltage Regulator was revised extensively.	2-87
	The "Serial Peripheral Interface (SPI) Characteristics" section and "Inter-Integrated Circuit (I^2C) Characteristics" section are new.	2-89, 2-91

Revision	Changes	Page
Revision 0 (continued)	"SmartFusion Development Tools" section was replaced with new content.	3-1
	The pin description tables were revised by adding additional pins to reflect the pinout for A2F500.	5-1 through 5-16
	The descriptions for "GNDSDD1" and "VCC33SDD1" were revised.	5-1, 5-2
	The description for "VCC33A" was revised.	5-2
	The pin tables for the "FG256" and "FG484" were replaced with tables that compare pin functions across densities for each package.	5-42
Draft B (December 2009)	The "Digital I/Os" section was renamed to the "I/Os and Operating Voltage" section and information was added regarding digital and analog VCC.	I
	The "SmartFusion cSoC Family Product Table" and "Package I/Os: MSS + FPGA I/Os" section were revised.	II
	The terminology for the analog blocks was changed to "programmable analog," consisting of two blocks: the analog front-end and analog compute engine. This is reflected throughout the text and in the "SmartFusion cSoC Block Diagram".	IV
	The "Product Ordering Codes" table was revised to add G as an ordering code for eNVM size.	VI
	Timing tables were populated with information that has become available for speed grade –1.	N/A
	All occurrences of the VMV parameter were removed.	N/A
	The SDD[n] voltage parameter was removed from Table 2-2 • Analog Maximum Ratings.	2-2
	Table 36-4 • Flash Programming Limits – Retention, Storage and Operating Temperature was replaced with Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits.	2-4
	The "Thermal Characteristics" section was revised extensively.	2-7
	Table 2-8 • Power Supplies Configuration was revised significantly.	2-10
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs were updated.	2-12
	Figure 2-2 • Timing Model was updated.	2-19
	The temperature associated with the reliability for LVTTL/LVCMOS in Table 2-34 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was changed from 110º to 100º.	2-29
	The values in Table 2-78 • Combinatorial Cell Propagation Delays were updated.	2-57
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator is new. Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator was revised.	2-62
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V and Table 2-91 • FlashROM Access Time, Worse Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V are new.	2-76
	The performance tables in the "Programmable Analog Specifications" section were revised, including new data available. Table 2-98 • Analog Sigma-Delta DAC is new.	2-78
	The "256-Pin FBGA" table for A2F200 is new.	4-15