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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

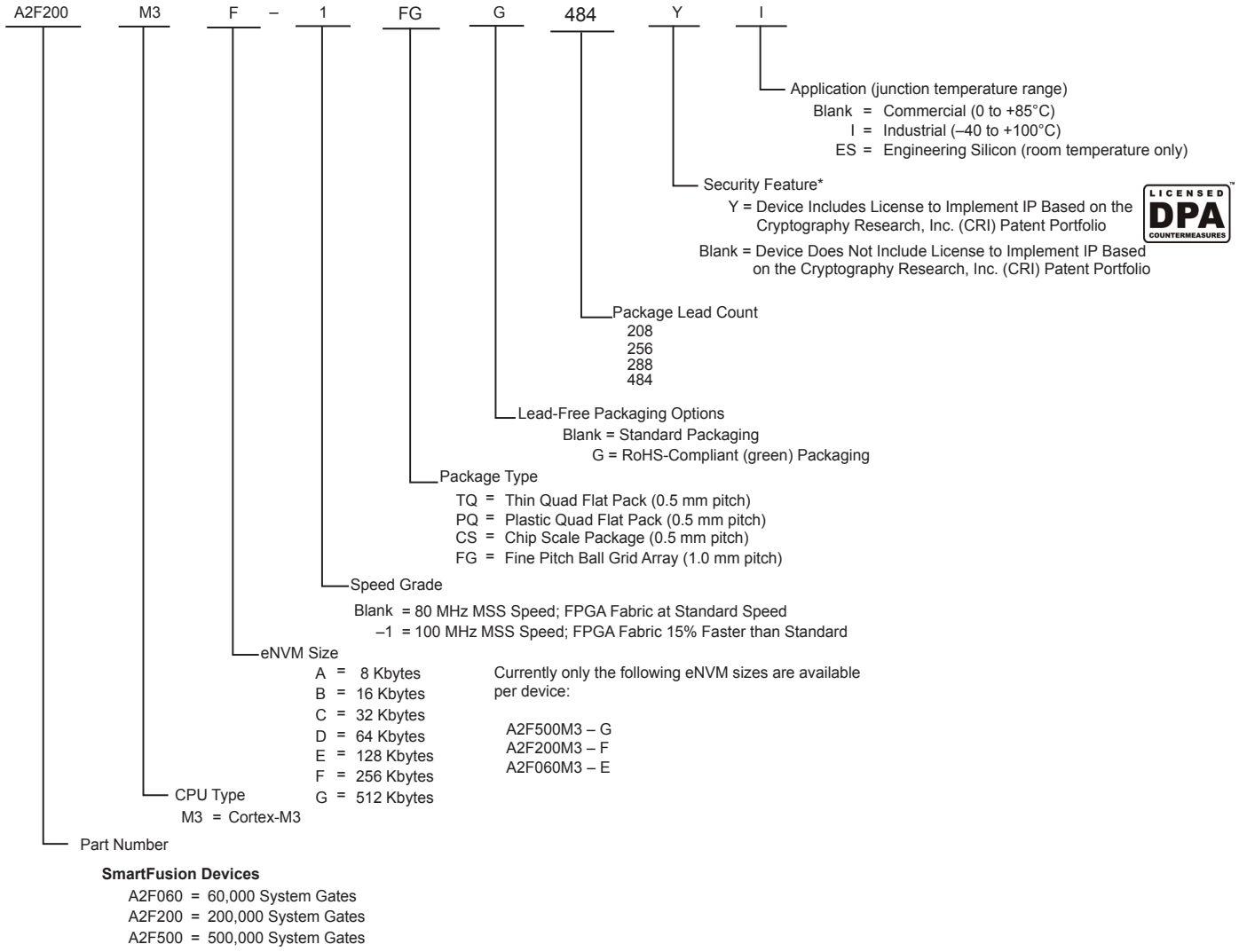
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-cs288i

Product Ordering Codes



*Note: *Most devices in the SmartFusion cSoC family can be ordered with the Y suffix. Devices with a package size greater or equal to 5x5 mm are supported. Contact your local Microsemi SoC Products Group sales representative for more information.*

Temperature Grade Offerings

SmartFusion cSoC	A2F060	A2F200	A2F500
TQ144	C, I	–	–
PQ208	–	C, I	C, I
CS288	C, I	C, I	C, I
FG256	C, I	C, I	C, I
FG484	–	C, I	C, I

Notes:
1. *C = Commercial Temperature Range: 0°C to 85°C Junction*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction*

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 2-6 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
A2F200M3F-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
A2F200M3F-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
A2F200M3F-CS288	26.6	20.2	18.1	7.3	9.4	°C/W
A2F200M3F-PQG208I	38.5	34.6	33.1	0.7	31.6	°C/W

Power Consumption of Various Internal Resources

Table 2-14 • **Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	3.39	3.40	5.05	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	1.14	1.83	2.50	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	1.15	1.15	1.15	µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.12	0.12	0.12	µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07	0.07	0.07	µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	1.04	0.79	0.79	µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11				
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11				
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00			µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00			µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60			µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00			µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88			mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80			µW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98			mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30			mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00			mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25			mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00			mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00			µW
PAC22	MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1]	VCC	1.5 V	67.50			mW
PAC23	Temperature Monitor Power Contribution	See Table 2-94 on page 2-79	–	1.23			mW

User I/O Characteristics

Timing Model

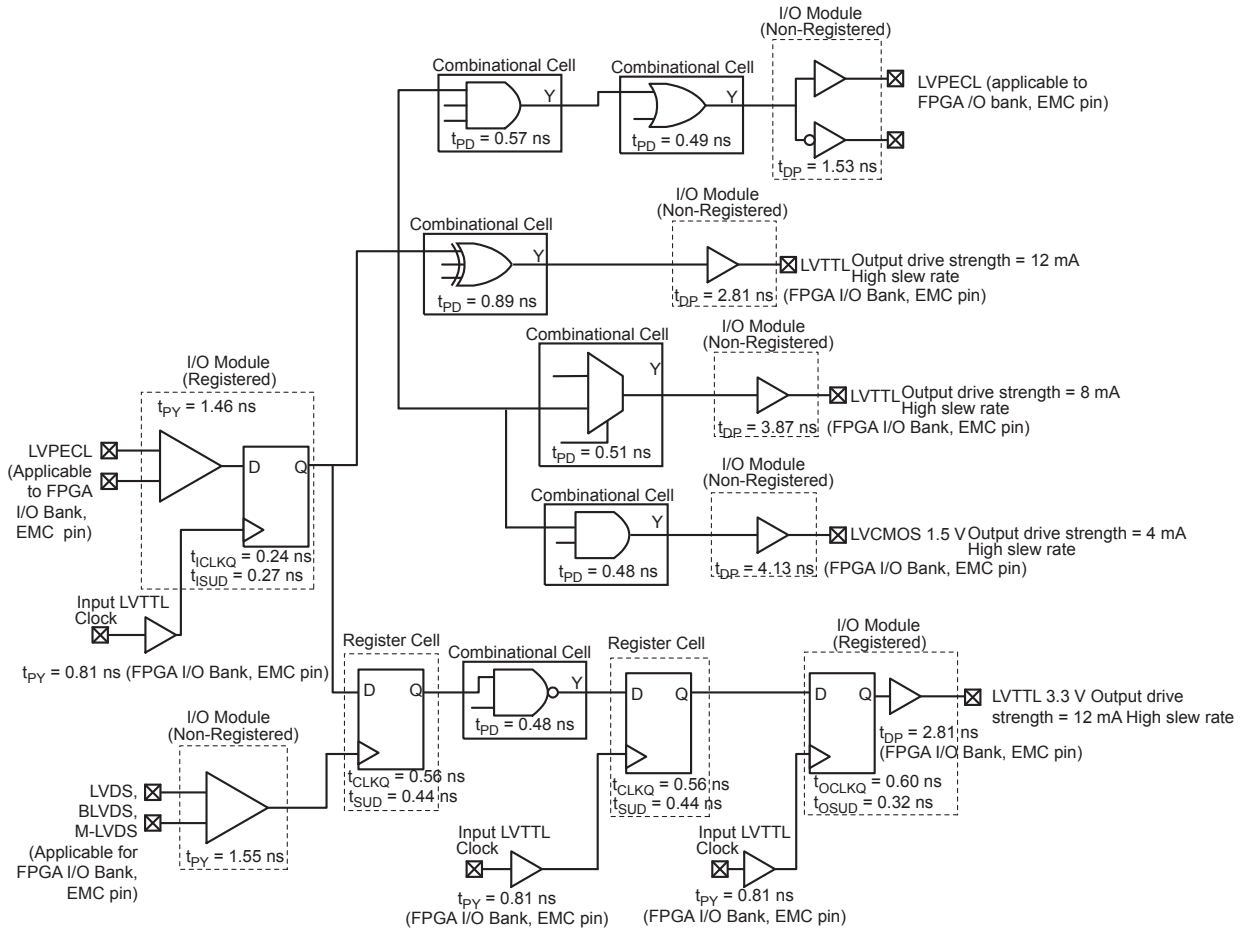


Figure 2-2 • **Timing Model**
Operating Conditions: –1 Speed, Commercial Temperature Range (T_J = 85°C), Worst Case VCC = 1.425 V

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

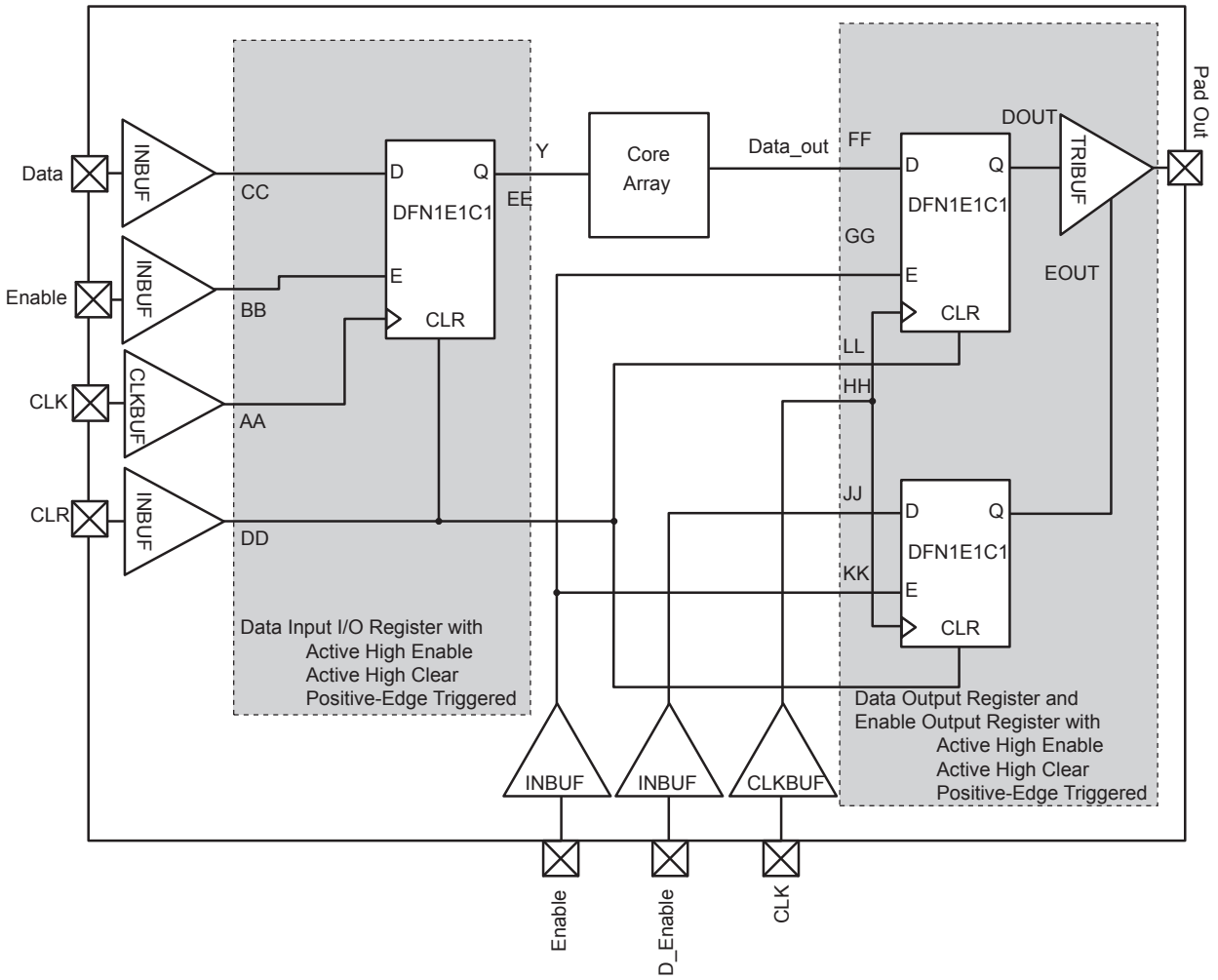


Figure 2-15 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Output DDR Module

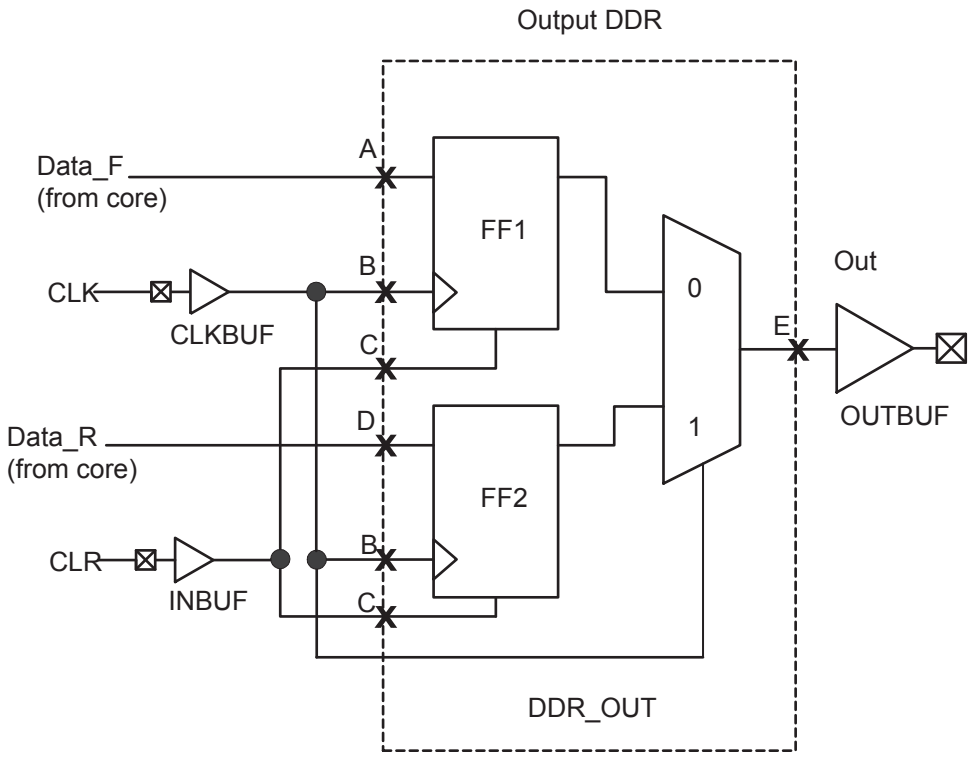


Figure 2-21 • **Output DDR Timing Model**

Table 2-76 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Timing Characteristics

Table 2-89 • **FIFO**
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.40	1.68	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.19	0.19	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.19	0.22	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.39	2.87	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.91	1.09	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.74	2.09	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.66	1.99	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	6.29	7.54	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.72	2.06	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.22	7.47	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to Data Out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET Recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.22	0.22	ns
t_{CYC}	Clock Cycle Time	3.28	3.28	ns
F_{MAX}	Maximum Frequency for FIFO	305	305	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Embedded Design

Microsemi offers FREE SoftConsole Eclipse based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microsemi also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.

Analog Design

The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, as well as DAC output.

The MSS configurator creates a bridge between the FPGA fabric and embedded designers so device configuration can be easily shared between multiple developers.

The MSS configurator includes the following:

- A simple configurator for the embedded designer to control the MSS peripherals and I/Os
- A method to import and view a hardware configuration from the FPGA flow into the embedded flow containing the memory map
- Automatic generation of drivers for any peripherals or soft IP used in the system configuration
- Comprehensive analog configuration for the programmable analog components
- Creation of a standard MSS block to be used in SmartDesign for connection of FPGA fabric designs and IP

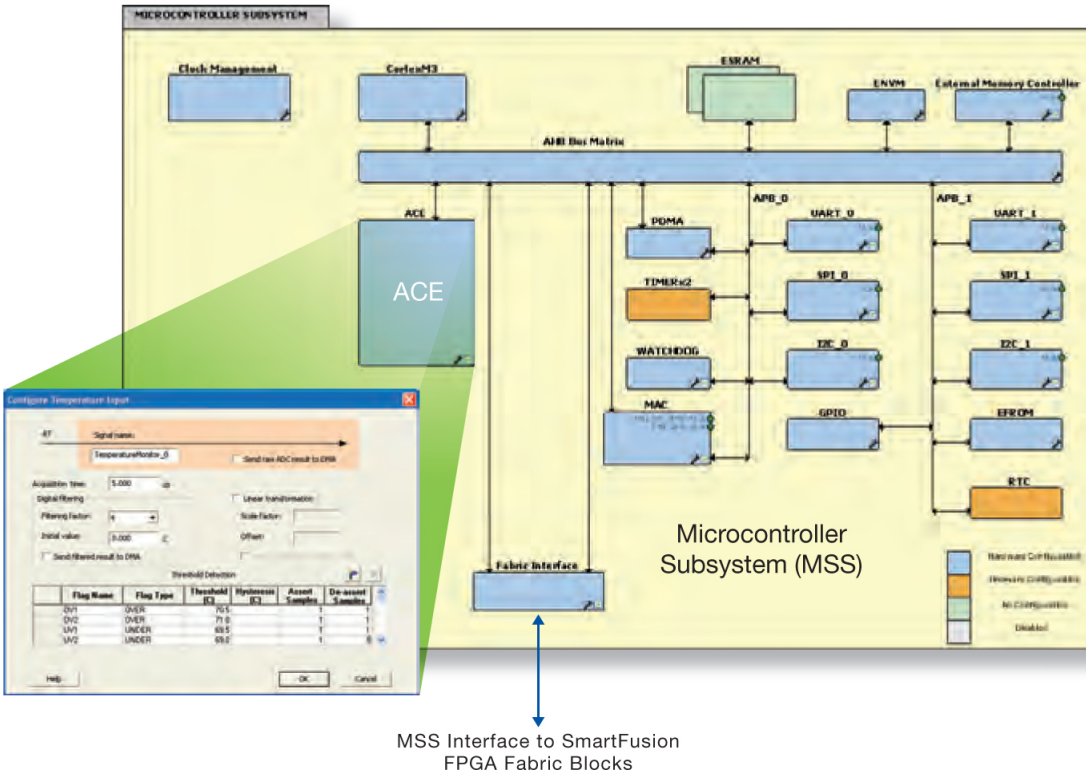


Figure 3-2 • **MSS Configurator**

Name	Type	Description
VCCFPGAIOB5	Supply	Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCLPXTAL	Supply	Analog supply to the low power 32 KHz crystal oscillator. Always power this pin.[1]
VCCMAINXTAL	Supply	Analog supply to the main crystal oscillator circuit. Always power this pin.[1]
VCCMSSIOB2	Supply	Supply voltage to the microcontroller subsystem I/O bank 2 (east MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCMSSIOB4	Supply	Supply voltage to the microcontroller subsystem I/O bank 4 (west MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCPLLx	Supply	Analog 1.5 V supply to the PLL. Always power this pin.
VCCRCOSC	Supply	Analog supply to the integrated RC oscillator circuit. Always power this pin.[1]
VCOMPLAx	Supply	Analog ground for the PLL
VDDBAT	Supply	External battery connection to the low power 32 KHz crystal oscillator (along with VCCLPXTAL), RTC, and battery switchover circuit. Can be pulled down if unused.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Name	Type	Polarity/Bus Size	Description
NCAP		1	Negative capacitor connection. This is the negative terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
PCAP		1	Positive Capacitor connection. This is the positive terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used.
PTBASE		1	Pass transistor base connection This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
PTEM		1	Pass transistor emitter connection. This is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
MSS_RESET_N		Low	Low Reset signal which can be used as an external reset and can also be used as a system level reset under control of the Cortex-M3 processor. MSS_RESET_N is an output asserted low after power-on reset. The direction of MSS_RESET_N changes during the execution of the Microsemi System Boot when chip-level reset is enabled. The Microsemi System Boot reconfigures MSS_RESET_N to become a reset input signal when chip-level reset is enabled. It has an internal pull-up so it can be left floating. In the current software, the MSS_RESET_N is modeled as an external input signal only.
PU_N	In	Low	Push-button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

JTAG Pins

SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the SmartFusion cSoC part must be supplied to allow JTAG signals to transition the SmartFusion cSoC. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRSTB pin could be tied to GND.

Name	Type	Polarity/ Bus Size	Description
JTAGSEL	In	1	JTAG controller selection Depending on the state of the JTAGSEL pin, an external JTAG controller will either see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low). The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP.
TCK	In	1	Test clock Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, it is recommended to tie off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state. Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 5-1 on page 5-11 for more information. Can be left floating when unused.
TDI	In	1	Test data Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
TDO	Out	1	Test data Serial output for JTAG boundary scan, ISP, and UJTAG usage.
TMS	In	HIGH	Test mode select The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin. Can be left floating when unused.
TRSTB	In	HIGH	Boundary scan reset pin The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 5-1 on page 5-11 and must satisfy the parallel resistance value requirement. The values in Table 5-1 on page 5-11 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected via a JTAG chain. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, it is recommended that you tie off TRST to GND through a resistor placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG – debug port (SWJ-DP) circuitry within the Cortex-M3. Can be left floating when unused.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
F12	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
F13	GND	GND	GND
F14	GCB1/IO19PPB0V0	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
F15	GNDQ	GNDQ	GNDQ
F16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
F17	GCB0/IO19NPB0V0	IO24NDB1V0	IO33NDB1V0
F19	IO23NDB1V0	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
F21	GCA2/IO21PDB1V0	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
G1	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G3	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	NC	GFB1/IO65PDB5V0	GFB1/IO82PDB5V0
G6	EMC_DB[10]/IO43NDB5V0	EMC_DB[10]/IO69NDB5V0	EMC_DB[10]/IO86NDB5V0
G9	NC	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
G13	GCA0/IO20NPB0V0	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
G16	NC	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
G17	IO22NPB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
G19	GCC2/IO23PDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
G21	GND	GND	GND
H1	EMC_DB[9]/IO40PPB5V0	EMC_DB[9]/GEC1/IO63PPB5V0	EMC_DB[9]/GEC1/IO80PPB5V0
H3	GND	GND	GND
H5	NC	GFB0/IO65NDB5V0	GFB0/IO82NDB5V0
H6	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H8	GND	GND	GND
H9	VCC	VCC	VCC
H10	GND	GND	GND
H11	VCC	VCC	VCC
H12	GND	GND	GND
H13	VCC	VCC	VCC
H14	GND	GND	GND
H16	NC	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
H17	NC	GDC2/IO32PPB1V0	GDC2/IO41PPB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
156	GNDQ	GNDQ
157	GNDQ	GNDQ
158	VCCFPGAIOB0	VCCFPGAIOB0
159	GBA1/IO19PDB0V0	GBA1/IO23PDB0V0
160	GBA0/IO19NDB0V0	GBA0/IO23NDB0V0
161	VCCFPGAIOB0	VCCFPGAIOB0
162	GND	GND
163	VCC	VCC
164	EMC_AB[25]/IO16PDB0V0	IO21PDB0V0
165	EMC_AB[24]/IO16NDB0V0	IO21NDB0V0
166	EMC_AB[23]/IO15PDB0V0	IO20PDB0V0
167	EMC_AB[22]/IO15NDB0V0	IO20NDB0V0
168	EMC_AB[21]/IO14PDB0V0	IO19PDB0V0
169	EMC_AB[20]/IO14NDB0V0	IO19NDB0V0
170	EMC_AB[19]/IO13PDB0V0	IO18PDB0V0
171	EMC_AB[18]/IO13NDB0V0	IO18NDB0V0
172	EMC_AB[17]/IO12PDB0V0	IO17PDB0V0
173	EMC_AB[16]/IO12NDB0V0	IO17NDB0V0
174	VCCFPGAIOB0	VCCFPGAIOB0
175	GND	GND
176	VCC	VCC
177	EMC_AB[15]/IO11PDB0V0	IO14PDB0V0
178	EMC_AB[14]/IO11NDB0V0	IO14NDB0V0
179	EMC_AB[13]/IO10PDB0V0	IO13PDB0V0
180	EMC_AB[12]/IO10NDB0V0	IO13NDB0V0
181	EMC_AB[11]/IO09PDB0V0	IO12PDB0V0
182	EMC_AB[10]/IO09NDB0V0	IO12NDB0V0
183	EMC_AB[9]/IO08PDB0V0	IO11PDB0V0
184	EMC_AB[8]/IO08NDB0V0	IO11NDB0V0
185	EMC_AB[7]/IO07PDB0V0	IO10PDB0V0
186	EMC_AB[6]/IO07NDB0V0	IO10NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
F14	IO21NDB1V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
F15	GND	GND	GND
F16	VCCENVM	VCCENVM	VCCENVM
G1	EMC_DB[8]/IO40NDB5V0	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
G2	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
G3	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
G4	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G6	GND	GND	GND
G7	VCC	VCC	VCC
G8	GND	GND	GND
G9	VCC	VCC	VCC
G10	GND	GND	GND
G11	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
G12	VPP	VPP	VPP
G13	TRSTB	TRSTB	TRSTB
G14	TMS	TMS	TMS
G15	TCK	TCK	TCK
G16	GNDENVM	GNDENVM	GNDENVM
H1	GND	GND	GND
H2	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
H3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H4	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
H5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
H6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H7	GND	GND	GND
H8	VCC	VCC	VCC
H9	GND	GND	GND
H10	VCC	VCC	VCC
H11	GND	GND	GND
H12	VJTAG	VJTAG	VJTAG

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
C15	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO19NPB0V0	GBA0/IO23NPB0V0
C20	NC	NC
C21	GBC2/IO21PDB1V0	GBC2/IO30PDB1V0
C22	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
D1	GND	GND
D2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC	NC
D5	NC	NC
D6	GND	GND
D7	NC	IO00NPB0V0
D8	NC	IO03NPB0V0
D9	GND	GND
D10	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
D14	GND	GND
D15	GBC1/IO17PPB0V0	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
D17	GND	GND
D18	GBA1/IO19PPB0V0	GBA1/IO23PPB0V0
D19	NC	NC
D20	NC	NC
D21	IO21NDB1V0	IO30NDB1V0
D22	GND	GND
E1	GFC2/IO67PPB5V0	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5	VCCFPGAIOB5
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
W3	GND	GND
W4	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
W5	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
W6	NC	SDD2
W7	GNDA	GNDA
W8	TM0	TM0
W9	ABPS2	ABPS2
W10	GND33ADC0	GND33ADC0
W11	VCC15ADC1	VCC15ADC1
W12	ABPS6	ABPS6
W13	NC	CM4
W14	NC	ABPS9
W15	NC	VCC33ADC2
W16	GNDA	GNDA
W17	PU_N	PU_N
W18	GNDSDD1	GNDSDD1
W19	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
W20	GND	GND
W21	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
W22	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
Y1	GPIO_3/IO44RSB4V0	GPIO_3/IO53RSB4V0
Y2	VCCMSSIOB4	VCCMSSIOB4
Y3	GPIO_15/IO34RSB4V0	GPIO_15/IO43RSB4V0
Y4	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
Y5	VCCMSSIOB4	VCCMSSIOB4
Y6	GNDSDD0	GNDSDD0
Y7	CM0	CM0
Y8	GNDTM0	GNDTM0
Y9	ADC0	ADC0
Y10	VCC15ADC0	VCC15ADC0
Y11	ABPS7	ABPS7
Y12	TM3	TM3
Y13	NC	ABPS8
Y14	NC	GND33ADC2

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (continued)	Corrected the Start-up time unit from "ms" to "µs" in Table 2-99 • Voltage Regulator (SAR 39395).	2-87
	Added the "References" section for "SmartFusion Development Tools" (SAR 43460).	3-1
	Updated the "References" section for Programming (SAR 43304). Added the "Application Notes on IAP Programming Technique" section (SAR 43458).	4-9
	A note was added to the "Supply Pins" table, referring to the *SmartFusion cSoC Board Design Guidelines* application note for details on VCCPLLx capacitor recommendations (SAR 42183).	5-1
	In the "Supply Pins" section, the VPP capacitor value section has been modified to: "For proper programming, 0.01µF, and 0.1µF to 1µF capacitors, (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible." (SAR 43569).	5-1
	In the "User-Defined Supply Pins" section, added description 'These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices.' for GPIO_x (SAR 28595).	5-5
	Updated the MAINXIN and MAINXOUT pin descriptions in the "Special Function Pins" section to read "If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating." (SAR 42807).	5-8
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 9 (September 2012)	The number of signal conditioning blocks (SCBs) for A2F500 in the "SmartFusion cSoC Family Product Table" was corrected to 4. Previously it had incorrectly been listed as 2 (SAR 39536).	II
	The "Product Ordering Codes" section was revised to clarify that only one eNVM size for each device is currently available (SAR 40333).	VI
	Information pertaining to analog I/Os was added to the "Specifying I/O States During Programming" section on page 1-3 (SAR 34836).	1-3
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34757).	2-27
	Maximum values for VIL and VIH were corrected in LVPECL Table 2-66 • Minimum and Maximum DC Input and Output Levels (SAR 37695).	2-43
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 29270).	2-59
	The temperature range for accuracy in Table 2-83 • Electrical Characteristics of the RC Oscillator was changed from "0°C to 85°C" to "–40°C to 100°C" (SAR 33670). The units for jitter were changed from ps to ps RMS (SAR 34270).	2-61
	In Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator, the output jitter for the 10 MHz crystal was corrected from 50 ps RMS to 1 ns RS (SAR 32939). Values for the startup time of VILXTAL were added (SAR 25248).	2-62
	In Table 2-85 • Electrical Characteristics of the Low Power Oscillator, output jitter was changed from 50 ps RMS to 30 ps RMS (SAR 32939). A value for ISTBXTAL standby current was added (SAR 25249). Startup time for a test load of 30 pF was added (SAR 27436).	2-62

Revision	Changes	Page
Revision 9 (continued)	The following note was added to Table 2-86 • SmartFusion CCC/PLL Specification in regard to delay increments in programmable delay blocks (SAR 34816): "When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information."	2-63
	Figure 2-36 • FIFO Read and Figure 2-37 • FIFO Write have been added (SAR 34851).	2-72
	Information regarding the MSS resetting itself after IAP of the FPGA fabric was added to the "Reprogramming the FPGA Fabric Using the Cortex-M3" section (SAR 37970).	4-8
	Instructions for unused VCC33ADCx pins were revised in "Supply Pins" (SAR 41137).	5-1
	Libero IDE was changed to Libero SoC throughout the document (SAR 40264).	N/A
Revision 8 (March 2012)	In the "Analog Front-End (AFE)" section, the resolution for the first-order sigma delta DAC was corrected from 12-bit to "8-bit, 16-bit, or 24-bit." The same correction was made in the "SmartFusion cSoC Family Product Table" (SAR 36541).	I, II
	The "SmartFusion cSoC Family Product Table" was revised to break out the features by package as well as device. The table now indicates that only one SPI is available for the PQ208 package in A2F200 and A2F500, and in the TQ144 package for A2F060 (SAR 33477). The EMC address bus size has been corrected to 26 bits (SAR 35664).	II
	The "SmartFusion cSoC Device Status" table was revised to change the CS288 package for A2F200 and A2F500 from preliminary to production status (SAR 37811).	III
	TQ144 package information for A2F060 was added to the "Package I/Os: MSS + FPGA I/Os" table, "SmartFusion cSoC Device Status" table, "Product Ordering Codes", and "Temperature Grade Offerings" table (SAR 36246).	III, VI
	Table 1 • SmartFusion cSoC Package Sizes Dimensions is new (SAR 31178).	III
	The Halogen-Free Packaging code (H) was removed from the "Product Ordering Codes" table (SAR 34017).	VI
	The "Specifying I/O States During Programming" section is new (SAR 34836).	1-3
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—P_{CLOCK}" section, was corrected to the "Device Architecture" chapter in the *SmartFusion FPGA Fabric User's Guide* (SAR 34742).	2-15
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34891).	2-30, 2-24
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34799): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-32
	In the SRAM "Timing Characteristics" tables, reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34874).	2-69
	The note for Table 2-93 • Current Monitor Performance Specification was modified to include the statement that the restriction on the TM pad being no greater than 10 mV above the CM pad.is applicable only if current monitor is used (SAR 26373).	2-78
	The unit "FR" in Table 2-96 • ABPS Performance Specifications and Table 2-98 • Analog Sigma-Delta DAC, used to designate full-scale error, was changed to "FS" and clarified with a table note (SAR 35342).	2-82, 2-85

Revision	Changes	Page
Revision 7 (continued)	The following sentence was removed from the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section because it is incorrect (SAR 31047): "The many different supplies can power up in any sequence with minimized current spikes or surges."	2-4
	Table 2-8 • Quiescent Supply Current Characteristics was divided into two tables: one for power supplies configurations and one for quiescent supply current. SoC mode was added to both tables (SAR 26378) and VCOMPLAx was removed from Table 2-8 • Power Supplies Configuration (SAR 29591). Quiescent supply current values were updated in Table 2-9 • Quiescent Supply Current Characteristics (SAR 33067).	2-10
	The "Total Static Power Consumption—P_{STAT}" section was revised: "$N_{eNVM\text{-}BLOCKS}$ * P_{DC4}" was removed from the equation for P_{STAT} (SAR 33067).	2-14
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs were revised to reflect updates in the SmartFusion power calculator (SARs 26405, 33067).	2-12, 2-13
	Table 2-82 • A2F060 Global Resource is new (SAR 33132).	2-61
	Output duty cycle was corrected to 50% in Table 2-83 • Electrical Characteristics of the RC Oscillator. It was incorrectly noted as 1% previously. Operating current for 3.3 domain was added (SAR 32940).	2-61
	Table 2-86 • SmartFusion CCC/PLL Specification was revised to add information and measurements regarding CCC output peak-to-peak period jitter (SAR 32996).	2-63
	The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-38 • FIFO Reset, and the FIFO "Timing Waveforms" tables were revised to ensure consistency with the software names (SAR 29991).	2-66 to 2-75
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised to correct the maximum frequencies (SAR 32410).	2-76
	Table 2-97 • Comparator Performance Specifications was moved to the "SmartFusion DC and Switching Characteristics" section from the SmartFusion Programmable Analog User's Guide because the information is extracted from characterization (SAR 24298).	2-84
	The hysteresis section in Table 2-97 • Comparator Performance Specifications was revised (SAR 33158).	2-84
	The "SmartFusion Development Tools" was extensively updated (SAR 33216).	3-1
	The text following Table 4-2 • JTAG Pin Descriptions was updated to add information on control of the JTAGSEL pin. Manual jumpers on the evaluation and development kits allow manual selection of this function for J-Link and ULINK debuggers (SAR 25592).	4-7