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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-csg288

Specify I/O States During Programming

Load from file... Save to file... ☐ Show BSR Details

Port Name	Macro Cell	Pin Number	I/O State (Output Only)
BIST	ADLIB:INBUF	T2	1
BYPASS_IO	ADLIB:INBUF	K1	1
CLK	ADLIB:INBUF	B1	1
ENOUT	ADLIB:INBUF	J16	1
LED	ADLIB:OUTBUF	M3	0
MONITOR[0]	ADLIB:OUTBUF	B5	0
MONITOR[1]	ADLIB:OUTBUF	C7	Z
MONITOR[2]	ADLIB:OUTBUF	D9	Z
MONITOR[3]	ADLIB:OUTBUF	D7	Z
MONITOR[4]	ADLIB:OUTBUF	A11	Z
OEa	ADLIB:INBUF	E4	Z
OEb	ADLIB:INBUF	F1	Z
OSC_EN	ADLIB:INBUF	K3	Z
PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

Help OK Cancel

Figure 1-1 • I/O States During Programming Window

- Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Table 2-2 • Analog Maximum Ratings

Parameter	Conditions	Min.	Max.	Units
ABPS[n] pad voltage (relative to ground)	GDEC[1:0] = 00 (± 15.36 V range)			
	Absolute maximum	–11.5	14.4	V
	Recommended	–11	14	V
	GDEC[1:0] = 01 (± 10.24 V range)	–11.5	12	V
	GDEC[1:0] = 10 (± 5.12 V range)	–6	6	V
	GDEC[1:0] = 11 (± 2.56 V range)	–3	3	V
CM[n] pad voltage relative to ground)	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 0 (comparator off, for the associated even-numbered comparator)			
	Absolute maximum	–0.3	14.4	V
	Recommended	–0.3	14	V
	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
TM[n] pad voltage (relative to ground)	TMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
ADC[n] pad voltage (relative to ground)		–0.3	3.6	V

Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. $T_J = 0^{\circ}\text{C}$ Max. $T_J = 85^{\circ}\text{C}$	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years
Industrial	Min. $T_J = -40^{\circ}\text{C}$ Max. $T_J = 100^{\circ}\text{C}$	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

Table 2-5 • Overshoot and Undershoot Limits ¹

VCCxxxxIOBx	Average VCCxxxxIOBx–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C .
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

Power Supply Sequencing Requirement

SmartFusion cSoCs have an on-chip 1.5 V regulator, but usage of an external 1.5 V supply is also allowed while the on-chip regulator is disabled. In that case, the 3.3 V supplies (VCC33A, etc.) should be powered before 1.5 V (VCC, etc.) supplies. The 1.5 V supplies should be enabled only after 3.3 V supplies reach a value higher than 2.7 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every SmartFusion cSoC. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-6](#).

There are five regions to consider during power-up.

SmartFusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCxxxxIOBx are above the minimum specified trip points ([Figure 2-1 on page 2-6](#)).
2. $VCC_{xxxxIOBx} > VCC - 0.75\text{ V}$ (typical)
3. Chip is in the SoC Mode.

VCCxxxxIOBx Trip Point:Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$ Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$ **VCC Trip Point:**Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$ Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1\text{ V}$

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to ["Specifying I/O States During Programming" on page 1-3](#).
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see [Figure 2-1 on page 2-6](#) for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the [ProASIC3 FPGA Fabric User's Guide](#) for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 2-6 • Package Thermal Resistance

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
A2F200M3F-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
A2F200M3F-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
A2F200M3F-CS288	26.6	20.2	18.1	7.3	9.4	°C/W
A2F200M3F-PQG208I	38.5	34.6	33.1	0.7	31.6	°C/W

DDR Module Specifications

Input DDR Module

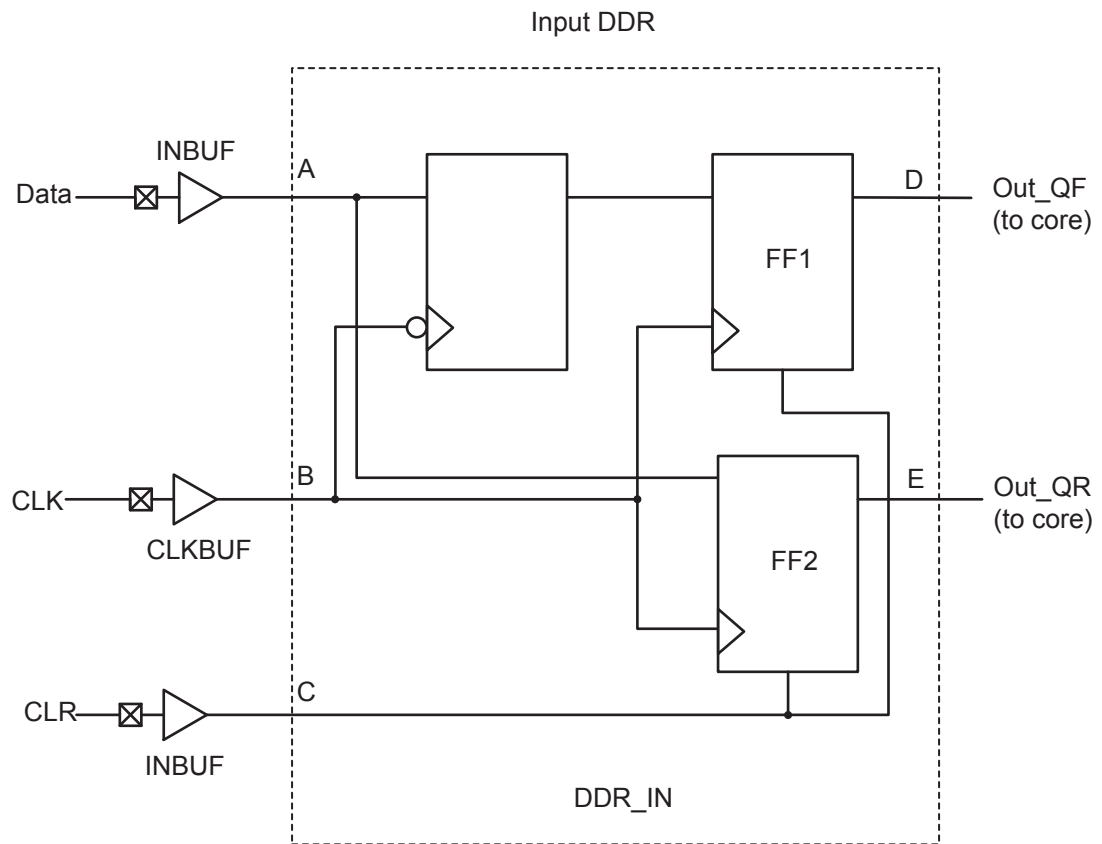


Figure 2-19 • Input DDR Timing Model

Table 2-74 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Output DDR Module

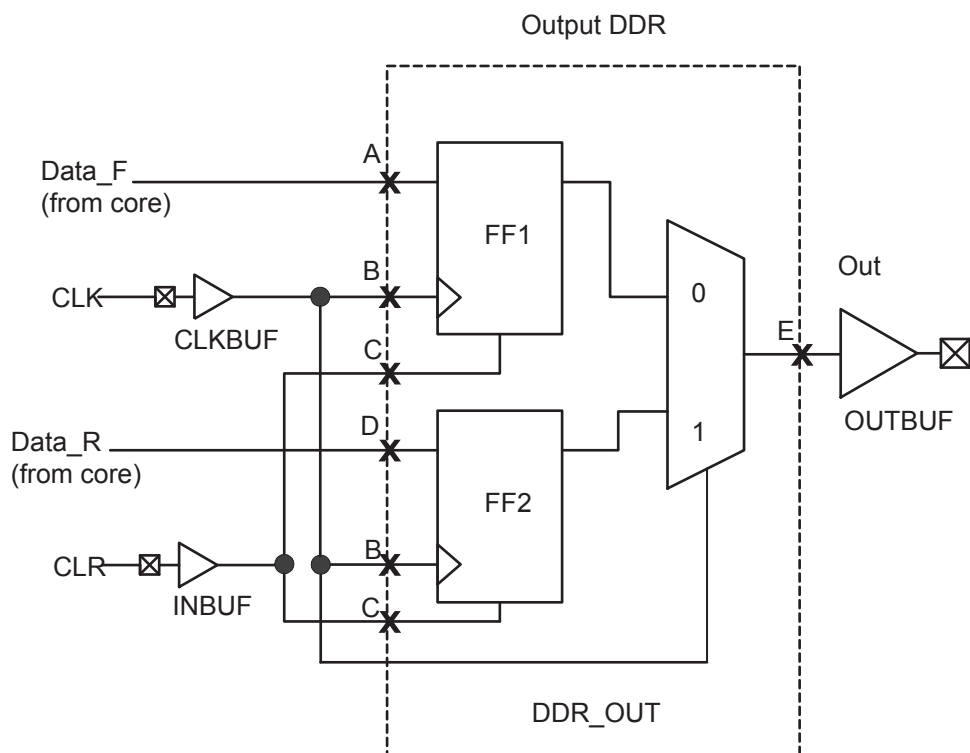


Figure 2-21 • Output DDR Timing Model

Table 2-76 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Name	Type	Polarity/Bus Size	Description
NCAP		1	Negative capacitor connection. This is the negative terminal of the charge pump. A capacitor, with a 2.2 μ F recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
PCAP		1	Positive Capacitor connection. This is the positive terminal of the charge pump. A capacitor, with a 2.2 μ F recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used.
PTBASE		1	Pass transistor base connection This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
PTEM		1	Pass transistor emitter connection. This is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
MSS_RESET_N		Low	Low Reset signal which can be used as an external reset and can also be used as a system level reset under control of the Cortex-M3 processor. MSS_RESET_N is an output asserted low after power-on reset. The direction of MSS_RESET_N changes during the execution of the Microsemi System Boot when chip-level reset is enabled. The Microsemi System Boot reconfigures MSS_RESET_N to become a reset input signal when chip-level reset is enabled. It has an internal pull-up so it can be left floating. In the current software, the MSS_RESET_N is modeled as an external input signal only.
PU_N	In	Low	Push-button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

Table 5-1 • Recommended Tie-Off Values for the TCK and TRST Pins

VJTAG	Tie-Off Resistance^{1, 2}
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Notes:

1. The TCK pin can be pulled up/down.
2. The TRST pin can only be pulled down.
1. Equivalent parallel resistance if more than one device is on JTAG chain.

TQ144	
Pin Number	A2F060 Function
109	VPP
110	GNDQ
111	GCA1/IO20PDB0V0
112	GCA0/IO20NDB0V0
113	GCB1/IO19PDB0V0
114	GCB0/IO19NDB0V0
115	GCC1/IO18PDB0V0
116	GCC0/IO18NDB0V0
117	VCCFPGAIOB0
118	GND
119	VCC
120	IO14PDB0V0
121	IO14NDB0V0
122	IO13NSB0V0
123	IO11PDB0V0
124	IO11NDB0V0
125	IO09PDB0V0
126	IO09NDB0V0
127	VCCFPGAIOB0
128	GND
129	IO07PDB0V0
130	IO07NDB0V0
131	IO06PDB0V0
132	IO06NDB0V0
133	IO05PDB0V0
134	IO05NDB0V0
135	IO03PDB0V0
136	IO03NDB0V0
137	VCCFPGAIOB0
138	GND
139	VCC
140	IO01PDB0V0
141	IO01NDB0V0
142	IO00PDB0V0
143	IO00NDB0V0
144	GNDQ

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
C21	IO17NDB0V0	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
D1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
D3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D19	GND	GND	GND
D21	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E3	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E5	GNDQ	GNDQ	GNDQ
E6	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
E7	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
E8	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
E9	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
E10	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
E11	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
E12	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
E13	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
E14	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
E15	GCC0/IO18NPB0V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
E16	GCA1/IO20PPB0V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E17	GCC1/IO18PPB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
E19	GCB2/IO22PPB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
E21	IO21NDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
F1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F5	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
F6	EMC_DB[11]/IO43PDB5V0	EMC_DB[11]/IO69PDB5V0	EMC_DB[11]/IO86PDB5V0
F7	GND	GND	GND
F8	NC	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
F9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
F10	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
F11	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin Number	PQ208	
	A2F200	A2F500
1	VCCPLL	VCCPLL0
2	VCOMPLA	VCOMPLA0
3	GNDQ	GNDQ
4	EMC_DB[15]/GAA2/IO71PDB5V0	GAA2/IO88PDB5V0
5	EMC_DB[14]/GAB2/IO71NDB5V0	GAB2/IO88NDB5V0
6	EMC_DB[13]/GAC2/IO70PDB5V0	GAC2/IO87PDB5V0
7	EMC_DB[12]/IO70NDB5V0	IO87NDB5V0
8	VCC	VCC
9	GND	GND
10	VCCFPGAIOB5	VCCFPGAIOB5
11	EMC_DB[11]/IO69PDB5V0	IO86PDB5V0
12	EMC_DB[10]/IO69NDB5V0	IO86NDB5V0
13	GFA2/IO68PSB5V0	GFA2/IO85PSB5V0
14	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0
15	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
16	EMC_DB[9]/GEC1/IO63PDB5V0	GEC1/IO80PDB5V0
17	EMC_DB[8]/GEC0/IO63NDB5V0	GEC0/IO80NDB5V0
18	EMC_DB[7]/GEB1/IO62PDB5V0	GEB1/IO79PDB5V0
19	EMC_DB[6]/GEB0/IO62NDB5V0	GEB0/IO79NDB5V0
20	EMC_DB[5]/GEA1/IO61PDB5V0	GEA1/IO78PDB5V0
21	EMC_DB[4]/GEA0/IO61NDB5V0	GEA0/IO78NDB5V0
22	VCC	VCC
23	GND	GND
24	VCCFPGAIOB5	VCCFPGAIOB5
25	EMC_DB[3]/GEC2/IO60PDB5V0	GEC2/IO77PDB5V0
26	EMC_DB[2]/IO60NDB5V0	IO77NDB5V0
27	EMC_DB[1]/GEB2/IO59PDB5V0	GEB2/IO76PDB5V0
28	EMC_DB[0]/GEA2/IO59NDB5V0	GEA2/IO76NDB5V0
29	VCC	VCC
30	GND	GND
31	GNDRCOSC	GNDRCOSC

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin Number	PQ208	
	A2F200	A2F500
187	VCCFPGAIOB0	VCCFPGAIOB0
188	GND	GND
189	VCC	VCC
190	EMC_AB[5]/IO06PDB0V0	IO08PDB0V0
191	EMC_AB[4]/IO06NDB0V0	IO08NDB0V0
192	EMC_AB[3]/IO05PDB0V0	GAC1/IO07PDB0V0
193	EMC_AB[2]/IO05NDB0V0	GAC0/IO07NDB0V0
194	EMC_AB[1]/IO04PDB0V0	IO04PDB0V0
195	EMC_AB[0]/IO04NDB0V0	IO04NDB0V0
196	EMC_OEN1_N/IO03PDB0V0	IO03PDB0V0
197	EMC_OEN0_N/IO03NDB0V0	IO03NDB0V0
198	EMC_BYTEN[1]/GAC1/IO02PDB0V0	GAA1/IO02PDB0V0
199	EMC_BYTEN[0]/GAC0/IO02NDB0V0	GAA0/IO02NDB0V0
200	VCCFPGAIOB0	VCCFPGAIOB0
201	GND	GND
202	VCC	VCC
203	EMC_CS1_N/GAB1/IO01PDB0V0	IO01PDB0V0
204	EMC_CS0_N/GAB0/IO01NDB0V0	IO01NDB0V0
205	EMC_RW_N/GAA1/IO00PDB0V0	IO00PDB0V0
206	EMC_CLK/GAA0/IO00NDB0V0	IO00NDB0V0
207	VCCFPGAIOB0	VCCFPGAIOB0
208	GNDQ	GNDQ

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
D15	GCA1/IO20PDB0V0	IO24NDB1V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E3	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ	GNDQ
E6	GND	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
E13	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND	GND
F8	VCC	VCC	VCC
F9	GND	GND	GND
F10	VCC	VCC	VCC
F11	GND	GND	GND
F12	IO22NDB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
F13	NC	GNDQ	GNDQ

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
T9	VAREF0	VAREF1	VAREF1
T10	ABPS0	ABPS6	ABPS6
T11	NC	ABPS5	ABPS5
T12	NC	SDD1	SDD1
T13	GNDVAREF	GNDVAREF	GNDVAREF
T14	GNDMAINXTAL	GNDMAINXTAL	GNDMAINXTAL
T15	VCCLPXTAL	VCCLPXTAL	VCCLPXTAL
T16	PU_N	PU_N	PU_N

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

6 – Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 13 (March 2015)	Updated Unused MSS I/O Configuration information in "User I/O Naming Conventions" (SAR 62994).	5-7
	Updated Table 2-90: "eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V" . Changed the maximum clock frequency for the control logic – 5 cycles to 50 MHz for A2F060 and A2F200 devices (SAR 63920). Added the following Note: "Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%" (SAR 63920).	2-76
Revision 12 (November 2013)	CS288 package dimensions added to "SmartFusion cSoC Package Sizes Dimensions" table (SAR 43730).	1-III
	Added "Typical Programming and Erase Times" table (SAR 43732).	4-9
	Definition of Ethernet MAC clarified in the "General Description" section (SAR 50083).	1-1
	Clarified GC and GF global inputs in "Global I/O Naming Conventions" section and link to SF Fabric UG added (SAR 42802).	5-6
Revision 11 (September 2013)	Modified the description for VAREF0 in the "User-Defined Supply Pins" (SAR 30204).	5-5
	Updated the "Pin Assignment Tables" section with a note for A2F500, all packages with GCAx saying: "Signal assigned to those pins as a CLKBUF or CLKBUF_LVPECL or CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal (SAR 45985).	5-18

Revision	Changes	Page
Revision 9 (continued)	The following note was added to Table 2-86 • SmartFusion CCC/PLL Specification in regard to delay increments in programmable delay blocks (SAR 34816): "When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information."	2-63
	Figure 2-36 • FIFO Read and Figure 2-37 • FIFO Write have been added (SAR 34851).	2-72
	Information regarding the MSS resetting itself after IAP of the FPGA fabric was added to the "Reprogramming the FPGA Fabric Using the Cortex-M3" section (SAR 37970).	4-8
	Instructions for unused VCC33ADCx pins were revised in "Supply Pins" (SAR 41137).	5-1
	Libero IDE was changed to Libero SoC throughout the document (SAR 40264).	N/A
Revision 8 (March 2012)	In the "Analog Front-End (AFE)" section , the resolution for the first-order sigma delta DAC was corrected from 12-bit to "8-bit, 16-bit, or 24-bit." The same correction was made in the "SmartFusion cSoC Family Product Table" (SAR 36541).	I, II
	The "SmartFusion cSoC Family Product Table" was revised to break out the features by package as well as device. The table now indicates that only one SPI is available for the PQ208 package in A2F200 and A2F500, and in the TQ144 package for A2F060 (SAR 33477). The EMC address bus size has been corrected to 26 bits (SAR 35664).	II
	The "SmartFusion cSoC Device Status" table was revised to change the CS288 package for A2F200 and A2F500 from preliminary to production status (SAR 37811).	III
	TQ144 package information for A2F060 was added to the "Package I/Os: MSS + FPGA I/Os" table, "SmartFusion cSoC Device Status" table, "Product Ordering Codes" , and "Temperature Grade Offerings" table (SAR 36246).	III, VI
	Table 1 • SmartFusion cSoC Package Sizes Dimensions is new (SAR 31178).	III
	The Halogen-Free Packaging code (H) was removed from the "Product Ordering Codes" table (SAR 34017).	VI
	The "Specifying I/O States During Programming" section is new (SAR 34836).	1-3
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—P_{CLOCK}" section , was corrected to the "Device Architecture" chapter in the SmartFusion FPGA Fabric User's Guide (SAR 34742).	2-15
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34891).	2-30, 2-24
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34799): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-32
	In the SRAM "Timing Characteristics" tables, reference was made to a new application note, Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs , which covers these cases in detail (SAR 34874).	2-69
	The note for Table 2-93 • Current Monitor Performance Specification was modified to include the statement that the restriction on the TM pad being no greater than 10 mV above the CM pad is applicable only if current monitor is used (SAR 26373).	2-78
	The unit "FR" in Table 2-96 • ABPS Performance Specifications and Table 2-98 • Analog Sigma-Delta DAC , used to designate full-scale error, was changed to "FS" and clarified with a table note (SAR 35342).	2-82, 2-85

Revision	Changes	Page
Revision 3 (continued)	Two notes were added to the "Supply Pins" table (SAR 27109): 1. The following supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL. 2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.	5-1
	The descriptions for the "VCC33N", "NCAP", and "PCAP" pins were revised to include information on what to do if analog SCB features and SDDs are not used (SAR 26744).	5-2, 5-9, 5-9
	Information was added to the "User Pins" table regarding tristating of used and unused GPIO pins. The IO portion of the table was revised to state that unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor (SAR 26890). Information was added regarding behavior of used I/O pins during power-up.	5-6
	The type for "EMC_RW_N" was changed from In/out to Out (SAR 25113).	5-12
	A note was added to the "Analog Front-End (AFE)" table stating that unused analog inputs should be grounded (SAR 26744).	5-14
	The "TQ144" section is new, with pin tables for A2F200 and A2F500 (SAR 27044).	5-18
	The "FG256" pin table was replaced and now includes "Handling When Unused" information (SAR 27709).	5-42
Revision 2 (May 2010)	Embedded nonvolatile flash memory (eNVM) was changed from "64 to 512 Kbytes" to "128 to 512 Kbytes" in the "Microcontroller Subsystem (MSS)" section and "SmartFusion cSoC Family Product Table" (SAR 26005).	I, II
	The main oscillator range of values was changed to "32 KHz to 20 MHz" in the "Microcontroller Subsystem (MSS)" section and the "SmartFusion cSoC Family Product Table" (SAR 24906).	I, II
	The value for t_{PD} was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the "Analog Front-End (AFE)" section (SAR 26005).	I
	The number of PLLs for A2F200 was changed from 2 to 1 in the "SmartFusion cSoC Family Product Table" (SAR 25093).	II
	Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the "Package I/Os: MSS + FPGA I/Os" table. The Max. column was removed from the table (SAR 26005).	III
	The Speed Grade section of the "Product Ordering Codes" table was revised (SAR 25257).	VI
Revision 1 (March 2010)	The "Product Ordering Codes" table was revised to add "blank" as an option for lead-free packaging and application (junction temperature range).	VI
	Table 2-3 • Recommended Operating Conditions ^{5,6} was revised. T_a (ambient temperature) was replaced with T_J (junction temperature).	2-3
	PDC5 was deleted from Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs.	2-13
	The formulas in the footnotes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised.	2-27
	The values for input biased current were revised in Table 2-93 • Current Monitor Performance Specification.	2-78
Revision 0 (March 2010)	The "Analog Front-End (AFE)" section was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps.	I