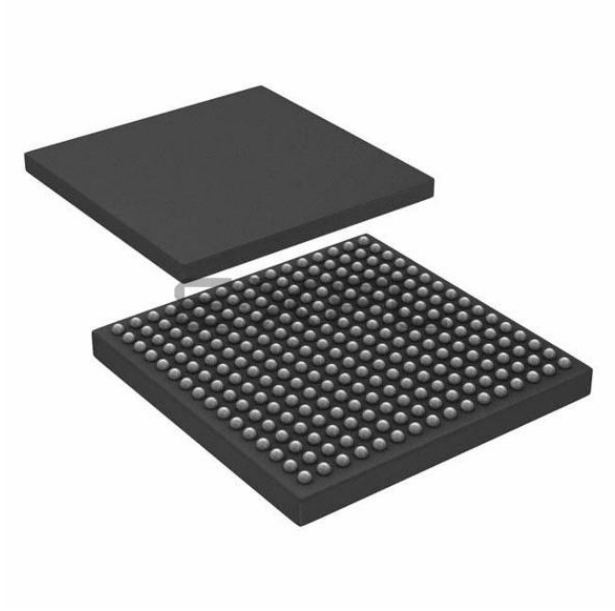

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-fg256

VCCxxxxIOBx Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to "Specifying I/O States During Programming" on page 1-3.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

Calculating Power Dissipation

Quiescent Supply Current

Table 2-8 • **Power Supplies Configuration**

Modes and Power Supplies	VCCxxxxIOBx VCCFPGAIOBx VCCMSSIOBx	VCC33A / VCC33ADCx VCC33AP / VCC33SDDx VCCMAINXTAL / VCCLPXTAL	VCC / VCC15A / VCC15ADCx VCCPLLx, VCCENVM, VCCESRAM	VDDBAT	VCCRCOSC	VJTAG	VPP	eNVM (reset/off)	LPXTAL (enable/disable)	MAINXTAL (enable/disable)
Time Keeping mode	0 V	0 V	0 V	3.3 V	0 V	0 V	0 V	Off	Enable	Disable
Standby mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	Reset	Enable	Disable
SoC mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	On	Enable	Enable

*Note: *On means proper voltage is applied. Refer to Table 2-3 on page 2-3 for recommended operating conditions.*

Table 2-9 • **Quiescent Supply Current Characteristics**

Parameter	Modes	A2F060		A2F200		A2F500	
		1.5 V Domain	3.3 V Domain	1.5 V Domain	3.3 V Domain	1.5 V Domain	3.3 V Domain
IDC1	SoC mode	3 mA	2 mA	7 mA	4 mA	16.5 mA	4 mA
IDC2	Standby mode	3 mA	2 mA	7 mA	4 mA	16.5 mA	4 mA
IDC3	Time Keeping mode	N/A	10 µA	N/A	10 µA	N/A	10 µA

Power per I/O Pin

Table 2-10 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins**

	VCCFPGAIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.55
2.5 V LVCMOS	2.5	–	5.97
1.8 V LVCMOS	1.8	–	2.88
1.5 V LVCMOS (JESD8-11)	1.5	–	2.33
3.3 V PCI	3.3	–	19.21
3.3 V PCI-X	3.3	–	19.21
Differential			
LVDS	2.5	2.26	0.82
LVPECL	3.3	5.72	1.16

Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings* Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.74	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	155.65
2.5 V LVCMOS	10	2.5	–	88.23
1.8 V LVCMOS	10	1.8	–	45.03
1.5 V LVCMOS (JESD8-11)	10	1.5	–	31.01

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
2.5 V LVCMOS	12 mA	High	35	–	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
1.8 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
1.5 V LVCMOS	12 mA	High	35	–	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
3.3 V PCI	Per PCI spec	High	10	25[1]	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25[1]	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
LVDS	24 mA	High	–	–	0.50	1.53	0.03	1.55	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.50	1.46	0.03	1.46	–	–	–	–	–	–	–	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns
2.5 V LVCMOS	8 mA	High	10	–	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns
1.8 V LVCMOS	4 mA	High	10	–	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns
1.5 V LVCMOS	2 mA	High	10	–	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-28 • I/O Output Buffer Maximum Resistances[1]
Applicable to MSS I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	8mA	50	150
2.5 V LVCMOS	8 mA	50	100
1.8 V LVCMOS	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCxxxxIOBx	$R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

Table 2-52 • 1.8 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	Std.	0.22	2.77	0.09	1.09	1.64	0.22	2.82	2.72	2.21	2.25	ns
	–1	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Output Enable Register

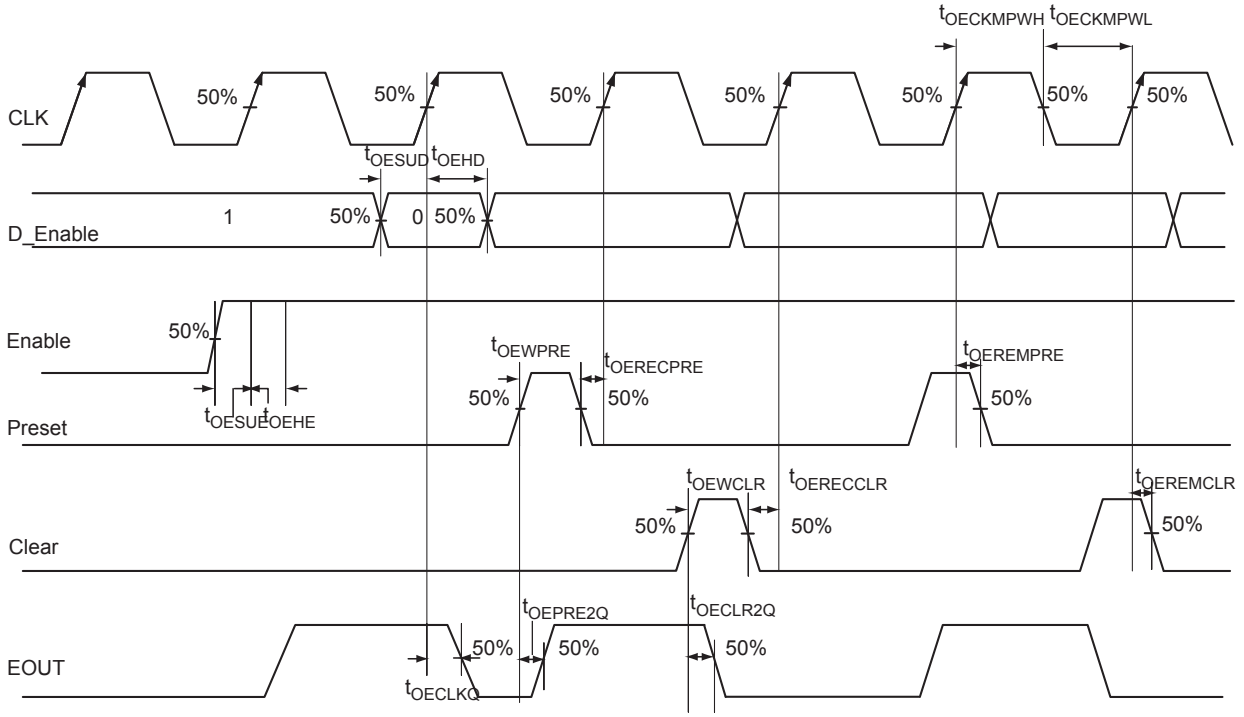


Figure 2-18 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-73 • **Output Enable Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.54	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.38	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.53	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

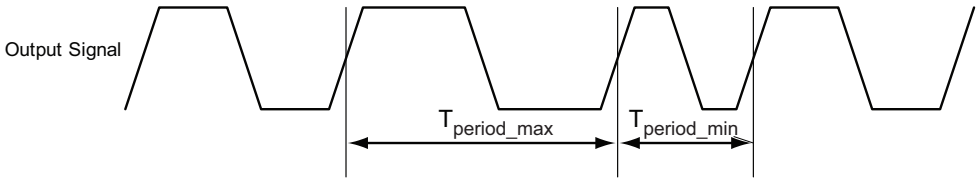
***Table 2-86* • SmartFusion CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350[1]	MHz
Delay Increments in Programmable Delay Blocks[2,3,4]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		5.15	%
Delay Range in Block: Programmable Delay 1[2,3]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[2,3]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[2,3]		2.2		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6,7]	Maximum Peak-to-Peak Period Jitter			

	SSO ≤ 2		SSO ≤ 4		SSO ≤ 8		SSO ≤ 16	
	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-28 • **Peak-to-Peak Jitter Definition**

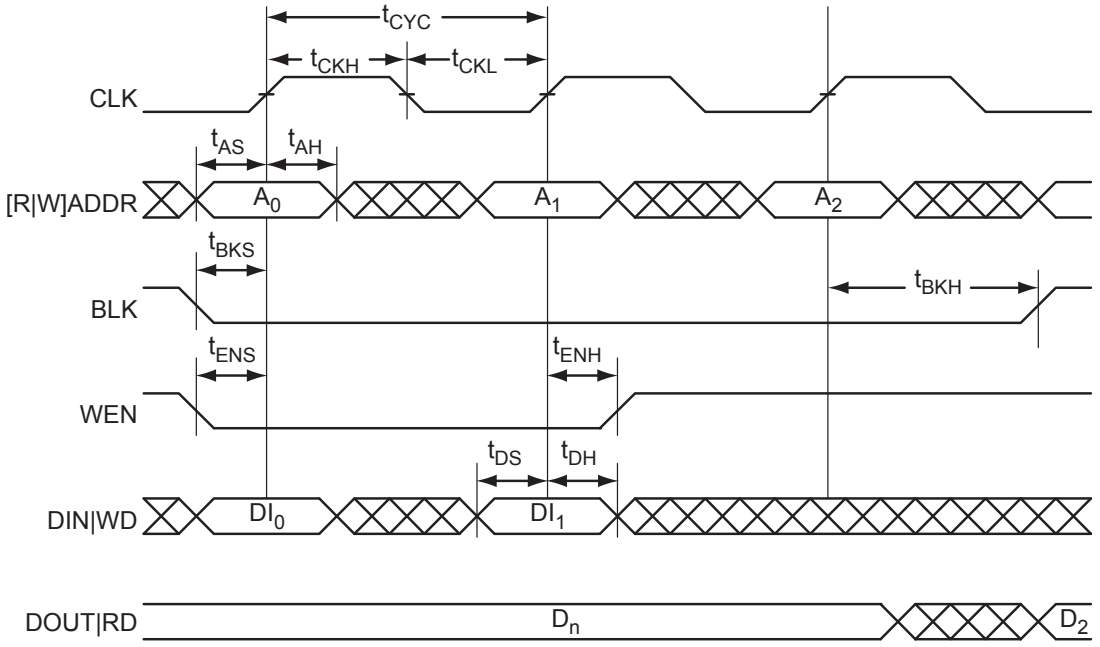


Figure 2-32 • **RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.**

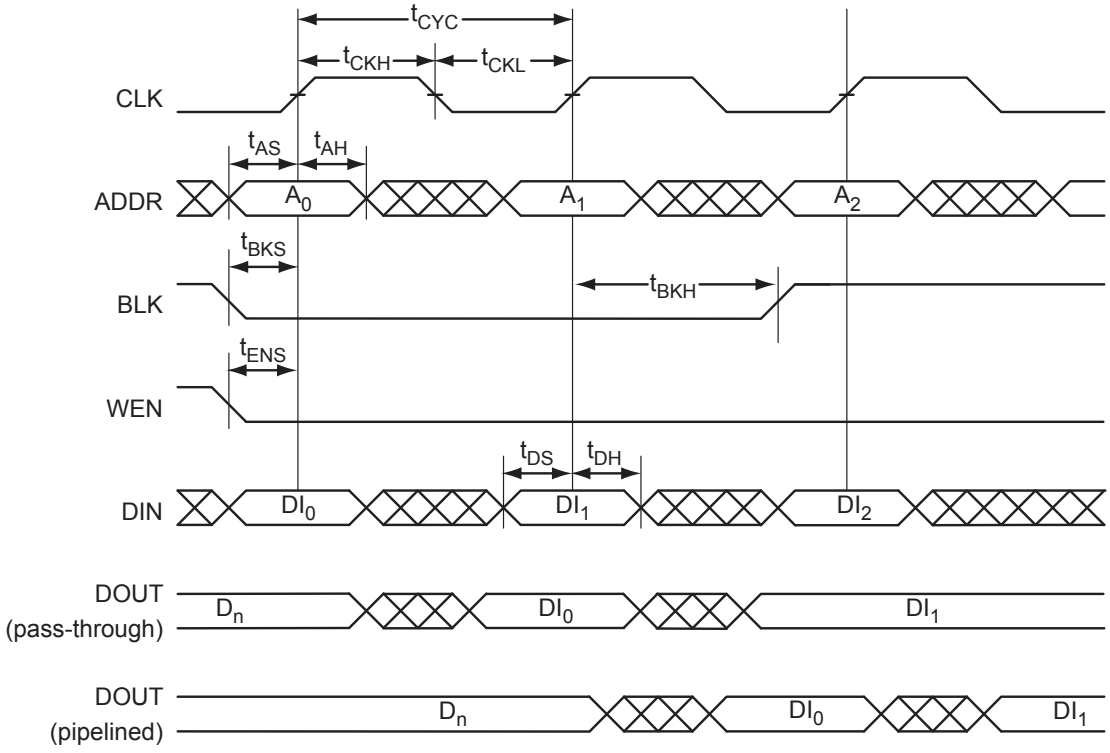


Figure 2-33 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

Timing Characteristics

Table 2-87 • RAM4K9
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.15	0.17	ns
t_{ENH}	REN, WEN hold time	0.10	0.12	ns
t_{BKS}	BLK setup time	0.24	0.28	ns
t_{BKH}	BLK hold time	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.19	0.22	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.81	2.18	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.39	2.87	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.91	1.09	ns
t_{C2CWWH}[1]	Address collision clk-to-clk delay for reliable write after write on same address—applicable to rising edge	0.23	0.26	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.34	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address— applicable to opening edge	0.37	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	0.94	1.12	ns
	RESET Low to Data Out Low on DOUT (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.22	ns
t_{CYC}	Clock cycle time	3.28	3.28	ns
F_{MAX}	Maximum clock frequency	305	305	MHz

Notes:

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Name	Type	Description
VCCFPGAIOB5	Supply	Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCLPXTAL	Supply	Analog supply to the low power 32 KHz crystal oscillator. Always power this pin.[1]
VCCMAINXTAL	Supply	Analog supply to the main crystal oscillator circuit. Always power this pin.[1]
VCCMSSIOB2	Supply	Supply voltage to the microcontroller subsystem I/O bank 2 (east MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCMSSIOB4	Supply	Supply voltage to the microcontroller subsystem I/O bank 4 (west MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCPLLx	Supply	Analog 1.5 V supply to the PLL. Always power this pin.
VCCRCOSC	Supply	Analog supply to the integrated RC oscillator circuit. Always power this pin.[1]
VCOMPLAx	Supply	Analog ground for the PLL
VDDBAT	Supply	External battery connection to the low power 32 KHz crystal oscillator (along with VCCLPXTAL), RTC, and battery switchover circuit. Can be pulled down if unused.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Pin Number	PQ208	
	A2F200	A2F500
1	VCCPLL	VCCPLL0
2	VCOMPLA	VCOMPLA0
3	GNDQ	GNDQ
4	EMC_DB[15]/GAA2/IO71PDB5V0	GAA2/IO88PDB5V0
5	EMC_DB[14]/GAB2/IO71NDB5V0	GAB2/IO88NDB5V0
6	EMC_DB[13]/GAC2/IO70PDB5V0	GAC2/IO87PDB5V0
7	EMC_DB[12]/IO70NDB5V0	IO87NDB5V0
8	VCC	VCC
9	GND	GND
10	VCCFPGAIOB5	VCCFPGAIOB5
11	EMC_DB[11]/IO69PDB5V0	IO86PDB5V0
12	EMC_DB[10]/IO69NDB5V0	IO86NDB5V0
13	GFA2/IO68PSB5V0	GFA2/IO85PSB5V0
14	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0
15	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
16	EMC_DB[9]/GEC1/IO63PDB5V0	GEC1/IO80PDB5V0
17	EMC_DB[8]/GEC0/IO63NDB5V0	GEC0/IO80NDB5V0
18	EMC_DB[7]/GEB1/IO62PDB5V0	GEB1/IO79PDB5V0
19	EMC_DB[6]/GEB0/IO62NDB5V0	GEB0/IO79NDB5V0
20	EMC_DB[5]/GEA1/IO61PDB5V0	GEA1/IO78PDB5V0
21	EMC_DB[4]/GEA0/IO61NDB5V0	GEA0/IO78NDB5V0
22	VCC	VCC
23	GND	GND
24	VCCFPGAIOB5	VCCFPGAIOB5
25	EMC_DB[3]/GEC2/IO60PDB5V0	GEC2/IO77PDB5V0
26	EMC_DB[2]/IO60NDB5V0	IO77NDB5V0
27	EMC_DB[1]/GEB2/IO59PDB5V0	GEB2/IO76PDB5V0
28	EMC_DB[0]/GEA2/IO59NDB5V0	GEA2/IO76NDB5V0
29	VCC	VCC
30	GND	GND
31	GNDRCOSC	GNDRCOSC

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
B16	GNDQ	GNDQ	GNDQ
C1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	VCCPLL0	VCCPLL	VCCPLL0
C3	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
C4	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C5	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
C6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
C7	GND	GND	GND
C8	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C9	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
C10	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C11	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C12	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C13	GND	GND	GND
C14	GCC0/IO18NPB0V0	GBA2/IO20PPB1V0	GBA2/IO27PPB1V0
C15	GCB0/IO19NDB0V0	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
C16	GCB1/IO19PDB0V0	IO23NDB1V0	IO28NDB1V0
D1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D2	VCOMPLA0	VCOMPLA	VCOMPLA0
D3	GND	GND	GND
D4	GNDQ	GNDQ	GNDQ
D5	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
D6	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
D7	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
D8	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
D9	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D10	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
D11	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
D12	GNDQ	GNDQ	GNDQ
D13	GCC1/IO18PPB0V0	GBB2/IO20NPB1V0	GBB2/IO27NPB1V0
D14	GCA0/IO20NDB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
F14	IO21NDB1V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
F15	GND	GND	GND
F16	VCCENVM	VCCENVM	VCCENVM
G1	EMC_DB[8]/IO40NDB5V0	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
G2	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
G3	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
G4	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G6	GND	GND	GND
G7	VCC	VCC	VCC
G8	GND	GND	GND
G9	VCC	VCC	VCC
G10	GND	GND	GND
G11	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
G12	VPP	VPP	VPP
G13	TRSTB	TRSTB	TRSTB
G14	TMS	TMS	TMS
G15	TCK	TCK	TCK
G16	GNDENVM	GNDENVM	GNDENVM
H1	GND	GND	GND
H2	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
H3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H4	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
H5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
H6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H7	GND	GND	GND
H8	VCC	VCC	VCC
H9	GND	GND	GND
H10	VCC	VCC	VCC
H11	GND	GND	GND
H12	VJTAG	VJTAG	VJTAG

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
C15	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO19NPB0V0	GBA0/IO23NPB0V0
C20	NC	NC
C21	GBC2/IO21PDB1V0	GBC2/IO30PDB1V0
C22	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
D1	GND	GND
D2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC	NC
D5	NC	NC
D6	GND	GND
D7	NC	IO00NPB0V0
D8	NC	IO03NPB0V0
D9	GND	GND
D10	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
D14	GND	GND
D15	GBC1/IO17PPB0V0	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
D17	GND	GND
D18	GBA1/IO19PPB0V0	GBA1/IO23PPB0V0
D19	NC	NC
D20	NC	NC
D21	IO21NDB1V0	IO30NDB1V0
D22	GND	GND
E1	GFC2/IO67PPB5V0	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5	VCCFPGAIOB5
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
H7	GND	GND
H8	VCC	VCC
H9	GND	GND
H10	VCC	VCC
H11	GND	GND
H12	VCC	VCC
H13	GND	GND
H14	VCC	VCC
H15	GND	GND
H16	VCCFPGAIOB1	VCCFPGAIOB1
H17	IO25NDB1V0	IO29NDB1V0
H18	GCC2/IO25PDB1V0	GCC2/IO29PDB1V0
H19	GND	GND
H20	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
H21	VCCFPGAIOB1	VCCFPGAIOB1
H22	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
J1	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J2	EMC_DB[5]/GEA1/IO61PDB5V0	EMC_DB[5]/GEA1/IO78PDB5V0
J3	EMC_DB[4]/GEA0/IO61NDB5V0	EMC_DB[4]/GEA0/IO78NDB5V0
J4	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
J5	VCCFPGAIOB5	VCCFPGAIOB5
J6	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5
J8	GND	GND
J9	VCC	VCC
J10	GND	GND
J11	VCC	VCC
J12	GND	GND
J13	VCC	VCC
J14	GND	GND
J15	VCC	VCC
J16	GND	GND
J17	NC	IO37PDB1V0
J18	VCCFPGAIOB1	VCCFPGAIOB1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
J19	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
J20	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
J21	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
J22	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
K1	GND	GND
K2	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
K4	NC	IO74PPB5V0
K5	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
K6	NC	IO75PDB5V0
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC
K11	GND	GND
K12	VCC	VCC
K13	GND	GND
K14	VCC	VCC
K15	GND	GND
K16	VCCFPGAIOB1	VCCFPGAIOB1
K17	NC	IO37NDB1V0
K18	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
K19	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
K20	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
K21	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
K22	GND	GND
L1	NC	IO73PDB5V0
L2	NC	IO73NDB5V0
L3	NC	IO72PPB5V0
L4	GND	GND
L5	NC	IO74NPB5V0
L6	NC	IO75NDB5V0
L7	VCCFPGAIOB5	VCCFPGAIOB5
L8	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (continued)	Corrected the Start-up time unit from "ms" to "µs" in Table 2-99 • Voltage Regulator (SAR 39395).	2-87
	Added the "References" section for "SmartFusion Development Tools" (SAR 43460).	3-1
	Updated the "References" section for Programming (SAR 43304). Added the "Application Notes on IAP Programming Technique" section (SAR 43458).	4-9
	A note was added to the "Supply Pins" table, referring to the *SmartFusion cSoC Board Design Guidelines* application note for details on VCCPLLx capacitor recommendations (SAR 42183).	5-1
	In the "Supply Pins" section, the VPP capacitor value section has been modified to: "For proper programming, 0.01µF, and 0.1µF to 1µF capacitors, (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible." (SAR 43569).	5-1
	In the "User-Defined Supply Pins" section, added description 'These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices.' for GPIO_x (SAR 28595).	5-5
	Updated the MAINXIN and MAINXOUT pin descriptions in the "Special Function Pins" section to read "If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating." (SAR 42807).	5-8
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 9 (September 2012)	The number of signal conditioning blocks (SCBs) for A2F500 in the "SmartFusion cSoC Family Product Table" was corrected to 4. Previously it had incorrectly been listed as 2 (SAR 39536).	II
	The "Product Ordering Codes" section was revised to clarify that only one eNVM size for each device is currently available (SAR 40333).	VI
	Information pertaining to analog I/Os was added to the "Specifying I/O States During Programming" section on page 1-3 (SAR 34836).	1-3
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34757).	2-27
	Maximum values for VIL and VIH were corrected in LVPECL Table 2-66 • Minimum and Maximum DC Input and Output Levels (SAR 37695).	2-43
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 29270).	2-59
	The temperature range for accuracy in Table 2-83 • Electrical Characteristics of the RC Oscillator was changed from "0°C to 85°C" to "–40°C to 100°C" (SAR 33670). The units for jitter were changed from ps to ps RMS (SAR 34270).	2-61
	In Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator, the output jitter for the 10 MHz crystal was corrected from 50 ps RMS to 1 ns RS (SAR 32939). Values for the startup time of VILXTAL were added (SAR 25248).	2-62
	In Table 2-85 • Electrical Characteristics of the Low Power Oscillator, output jitter was changed from 50 ps RMS to 30 ps RMS (SAR 32939). A value for ISTBXTAL standby current was added (SAR 25249). Startup time for a test load of 30 pF was added (SAR 27436).	2-62

Revision	Changes	Page
Revision 7 (continued)	The following sentence was removed from the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section because it is incorrect (SAR 31047): "The many different supplies can power up in any sequence with minimized current spikes or surges."	2-4
	Table 2-8 • Quiescent Supply Current Characteristics was divided into two tables: one for power supplies configurations and one for quiescent supply current. SoC mode was added to both tables (SAR 26378) and VCOMPLAx was removed from Table 2-8 • Power Supplies Configuration (SAR 29591). Quiescent supply current values were updated in Table 2-9 • Quiescent Supply Current Characteristics (SAR 33067).	2-10
	The "Total Static Power Consumption—P_{STAT}" section was revised: "$N_{eNVM\text{-}BLOCKS}$ * P_{DC4}" was removed from the equation for P_{STAT} (SAR 33067).	2-14
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs were revised to reflect updates in the SmartFusion power calculator (SARs 26405, 33067).	2-12, 2-13
	Table 2-82 • A2F060 Global Resource is new (SAR 33132).	2-61
	Output duty cycle was corrected to 50% in Table 2-83 • Electrical Characteristics of the RC Oscillator. It was incorrectly noted as 1% previously. Operating current for 3.3 domain was added (SAR 32940).	2-61
	Table 2-86 • SmartFusion CCC/PLL Specification was revised to add information and measurements regarding CCC output peak-to-peak period jitter (SAR 32996).	2-63
	The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-38 • FIFO Reset, and the FIFO "Timing Waveforms" tables were revised to ensure consistency with the software names (SAR 29991).	2-66 to 2-75
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised to correct the maximum frequencies (SAR 32410).	2-76
	Table 2-97 • Comparator Performance Specifications was moved to the "SmartFusion DC and Switching Characteristics" section from the SmartFusion Programmable Analog User's Guide because the information is extracted from characterization (SAR 24298).	2-84
	The hysteresis section in Table 2-97 • Comparator Performance Specifications was revised (SAR 33158).	2-84
	The "SmartFusion Development Tools" was extensively updated (SAR 33216).	3-1
	The text following Table 4-2 • JTAG Pin Descriptions was updated to add information on control of the JTAGSEL pin. Manual jumpers on the evaluation and development kits allow manual selection of this function for J-Link and ULINK debuggers (SAR 25592).	4-7