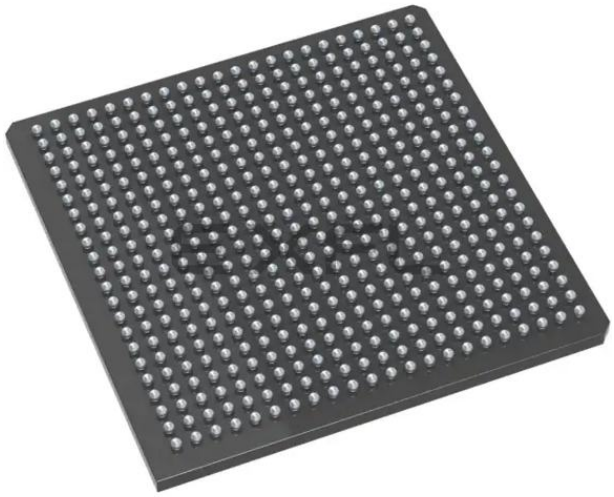

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-fg484

SmartFusion cSoC Family Product Table

FPGA Fabric	A2F060			A2F200				A2F500			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
System Gates	60,000			200,000				500,000			
Tiles (D-flip-flops)	1,536			4,608				11,520			
RAM Blocks (4,608 bits)	8			8				24			
Microcontroller Subsystem (MSS)	**A2F060**			**A2F200**				**A2F500**			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Flash (Kbytes)	128			256				512			
SRAM (Kbytes)	16			64				64			
Cortex-M3 processor with MPU	Yes			Yes				Yes			
10/100 Ethernet MAC	No			Yes				Yes			
External Memory Controller (EMC)	–	26-/16-bit address/data		26-bit address,16-bit data				–	26-/16-bit address/data		
DMA	8 Ch			8 Ch				8 Ch			
I^2C	2			2				2			
SPI	1	2		1	2			1	2		
16550 UART	2			2				2			
32-Bit Timer	2			2				2			
PLL	1			1				1	2	1	2
32 KHz Low Power Oscillator	1			1				1			
100 MHz On-Chip RC Oscillator	1			1				1			
Main Oscillator (32 KHz to 20 MHz)	1			1				1			
Programmable Analog	**A2F060**			**A2F200**				**A2F500**			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
ADCs (8-/10-/12-bit SAR)	1			2				2			3
DACs (8-/16-/24-bit sigma-delta)	1			2				2			3
Signal Conditioning Blocks (SCBs)	1			4				4			5
Comparator*	2			8				8			10
Current Monitors*	1			4				4			5
Temperature Monitors*	1			4				4			5
Bipolar High Voltage Monitors*	2			8				8			10

*Note: *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130925 for details.*

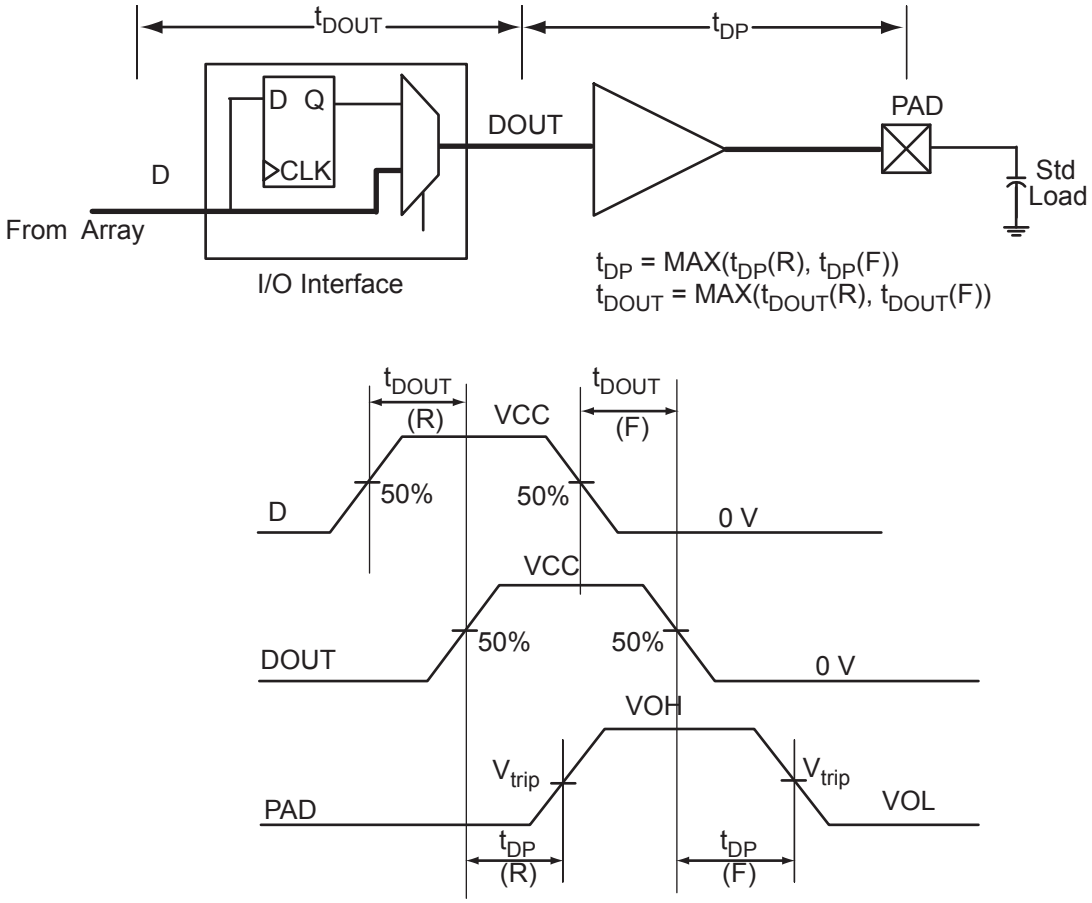

Figure 2-4 • **Output Buffer Model and Delays (example)**

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than 2200 operation hours to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-32* • Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

***Table 2-33* • Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical)
3.3 V LVTTL / LVCMOS / PCI / PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

***Table 2-34* • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (100°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi SoC Products Group recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Timing Characteristics

Table 2-50 • 1.8 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.06	0.04	1.14	0.39	8.61	11.06	2.61	1.59	10.67	13.12	ns
	–1	0.50	9.22	0.03	0.95	0.32	7.17	9.22	2.18	1.33	8.89	10.93	ns
4 mA	Std.	0.60	6.46	0.04	1.14	0.39	5.53	6.46	3.04	2.66	7.59	8.51	ns
	–1	0.50	5.38	0.03	0.95	0.32	4.61	5.38	2.54	2.22	6.33	7.10	ns
6 mA	Std.	0.60	4.16	0.04	1.14	0.39	3.99	4.16	3.34	3.18	6.05	6.22	ns
	–1	0.50	3.47	0.03	0.95	0.32	3.32	3.47	2.78	2.65	5.04	5.18	ns
8 mA	Std.	0.60	3.69	0.04	1.14	0.39	3.76	3.67	3.40	3.31	5.81	5.73	ns
	–1	0.50	3.07	0.03	0.95	0.32	3.13	3.06	2.84	2.76	4.85	4.78	ns
12 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
16 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-51 • 1.8 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	14.24	0.04	1.14	0.39	13.47	14.24	2.62	1.54	15.53	16.30	ns
	–1	0.50	11.87	0.03	0.95	0.32	11.23	11.87	2.18	1.28	12.94	13.59	ns
4 mA	Std.	0.60	9.74	0.04	1.14	0.39	9.92	9.62	3.05	2.57	11.98	11.68	ns
	–1	0.50	8.11	0.03	0.95	0.32	8.26	8.02	2.54	2.14	9.98	9.74	ns
6 mA	Std.	0.60	7.67	0.04	1.14	0.39	7.81	7.24	3.34	3.08	9.87	9.30	ns
	–1	0.50	6.39	0.03	0.95	0.32	6.51	6.03	2.79	2.56	8.23	7.75	ns
8 mA	Std.	0.60	7.15	0.04	1.14	0.39	7.29	6.75	3.41	3.21	9.34	8.80	ns
	–1	0.50	5.96	0.03	0.95	0.32	6.07	5.62	2.84	2.68	7.79	7.34	ns
12 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns
16 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

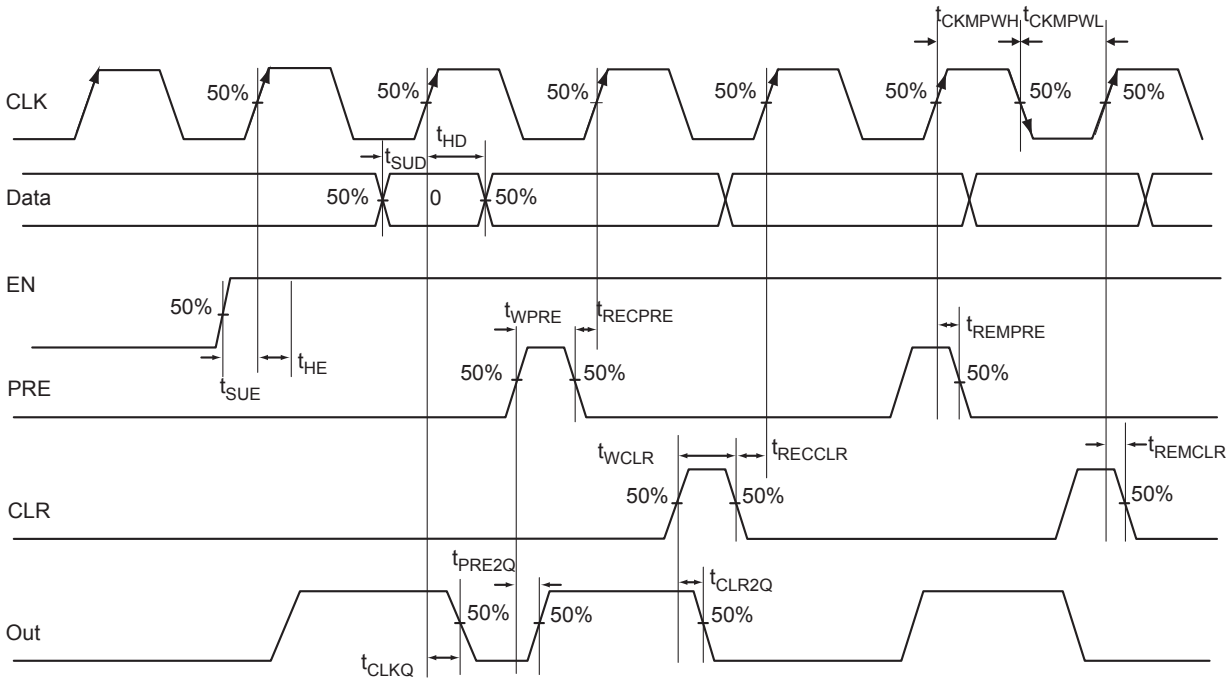

Figure 2-26 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-79 • **Register Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.56	0.67	ns
t_{SUD}	Data Setup Time for the Core Register	0.44	0.52	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.46	0.55	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.41	0.49	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.41	0.49	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.23	0.27	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	0.27	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.22	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.22	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.32	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-80 • A2F500 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.54	1.73	1.84	2.08	ns
t_{RCKH}	Input High Delay for Global Clock	1.53	1.76	1.84	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.23		0.28	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-81 • A2F200 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.74	0.99	0.88	1.19	ns
t_{RCKH}	Input High Delay for Global Clock	0.76	1.05	0.91	1.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.29		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

FPGA Fabric SRAM and FIFO Characteristics

FPGA Fabric SRAM

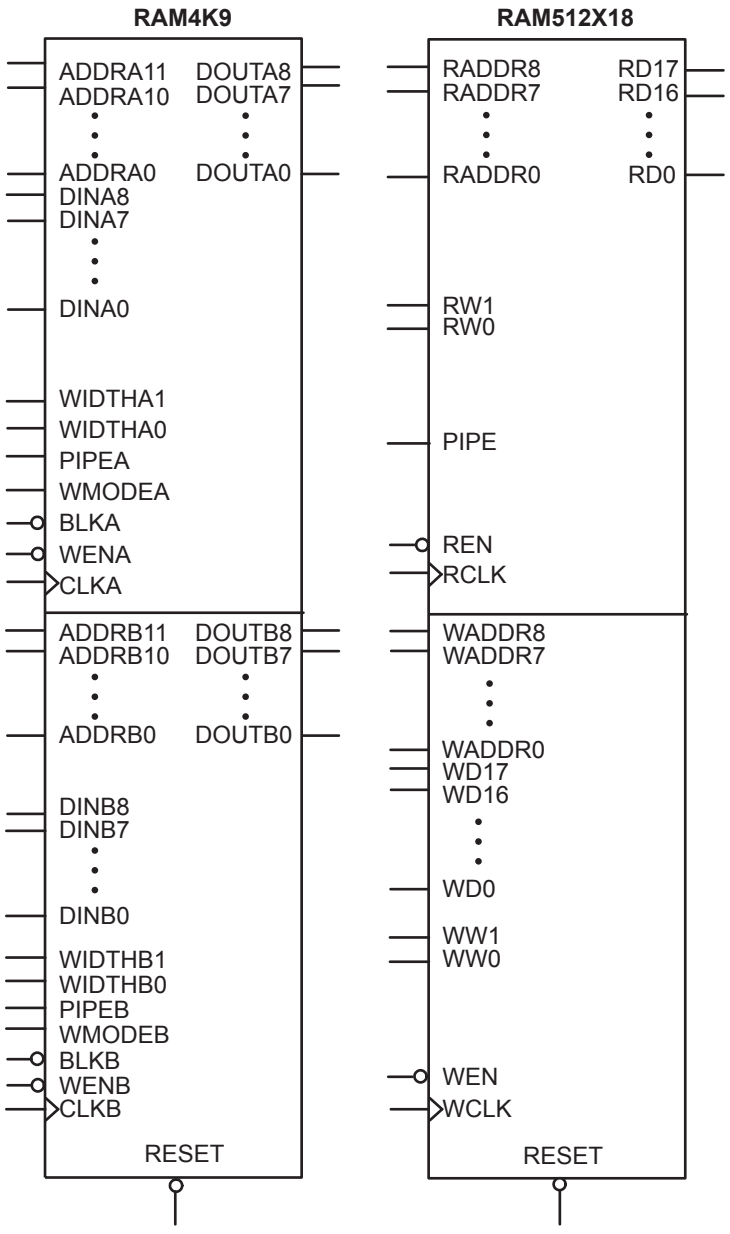

Figure 2-29 • **RAM Models**

***Table 2-96* • ABPS Performance Specifications (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input referred offset voltage					
	GDEC[1:0] = 11	–0.31	–0.07	0.31	% FS*
	–40ºC to +100ºC	–1.00		1.47	% FS*
	GDEC[1:0] = 10	–0.34	–0.07	0.34	% FS*
	–40ºC to +100ºC	–0.90		1.37	% FS*
	GDEC[1:0] = 01	–0.61	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.05		1.35	% FS*
	GDEC[1:0] = 00	–0.39	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.06		1.38	% FS*
SINAD		53	56		dB
Non-linearity	RMS deviation from BFSL			0.5	% FS*
Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 11*	GDEC[1:0] = 11 (±2.56 range), –1 dBFS input				
	12-bit mode 10 KHz	8.6	9.1		Bits
	12-bit mode 100 KHz	8.6	9.1		Bits
	10-bit mode 10 KHz	8.5	8.9		Bits
	10-bit mode 100 KHz	8.5	8.9		Bits
	8-bit mode 10 KHz	7.7	7.8		Bits
	8-bit mode 100 KHz	7.7	7.8		Bits
Large-signal bandwidth	–1 dBFS input		1		MHz
Analog settling time	To 0.1% of final value (with ADC load)			10	µs
Input resistance			1		MΩ
Power supply rejection ratio	DC (0–1 KHz)	38	40		dB
ABPS power supply current requirements (not including ADC or VAREFx)	ABPS_EN = 1 (operational mode)				
	VCC33A		123	134	µA
	VCC33AP		89	94	µA
	VCC15A		1		µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quite analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GNDA	Ground	Quiet analog ground to the analog front-end
GNDAQ	Ground	Quiet analog ground to the analog I/O of SmartFusion cSoCs
GNDENVM	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GNDLPXTAL	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GNDMAINXTAL	Ground	Analog ground to the main crystal oscillator circuitry
GNDQ	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND.
GNDRCOSC	Ground	Analog ground to the integrated RC oscillator circuit
GNDSDD0	Ground	Analog ground to the first sigma-delta DAC
GNDSDD1	Ground	Common analog ground to the second and third sigma-delta DACs
GNDTM0	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM1	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM2	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GNDVAREF	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the *SmartFusion Programmable Analog User's Guide*.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

PQ208

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
B3	NC	NC
B4	NC	NC
B5	VCCFPGAIOB0	VCCFPGAIOB0
B6	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
B7	NC	IO04PPB0V0
B8	VCCFPGAIOB0	VCCFPGAIOB0
B9	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
B10	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B11	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
B12	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
B13	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
B14	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
B15	VCCFPGAIOB0	VCCFPGAIOB0
B16	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B17	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
B18	VCCFPGAIOB0	VCCFPGAIOB0
B19	GBB0/IO18NDB0V0	GBB0/IO24NDB0V0
B20	GBB1/IO18PDB0V0	GBB1/IO24PDB0V0
B21	GND	GND
B22	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
C1	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	NC	NC
C3	NC	NC
C4	NC	IO01NDB0V0
C5	NC	IO01PDB0V0
C6	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
C7	NC	IO03PPB0V0
C8	NC	IO04NPB0V0
C9	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
C10	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
C11	GND	GND
C12	VCCFPGAIOB0	VCCFPGAIOB0
C13	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C14	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
H7	GND	GND
H8	VCC	VCC
H9	GND	GND
H10	VCC	VCC
H11	GND	GND
H12	VCC	VCC
H13	GND	GND
H14	VCC	VCC
H15	GND	GND
H16	VCCFPGAIOB1	VCCFPGAIOB1
H17	IO25NDB1V0	IO29NDB1V0
H18	GCC2/IO25PDB1V0	GCC2/IO29PDB1V0
H19	GND	GND
H20	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
H21	VCCFPGAIOB1	VCCFPGAIOB1
H22	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
J1	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J2	EMC_DB[5]/GEA1/IO61PDB5V0	EMC_DB[5]/GEA1/IO78PDB5V0
J3	EMC_DB[4]/GEA0/IO61NDB5V0	EMC_DB[4]/GEA0/IO78NDB5V0
J4	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
J5	VCCFPGAIOB5	VCCFPGAIOB5
J6	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5
J8	GND	GND
J9	VCC	VCC
J10	GND	GND
J11	VCC	VCC
J12	GND	GND
J13	VCC	VCC
J14	GND	GND
J15	VCC	VCC
J16	GND	GND
J17	NC	IO37PDB1V0
J18	VCCFPGAIOB1	VCCFPGAIOB1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
J19	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
J20	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
J21	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
J22	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
K1	GND	GND
K2	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
K4	NC	IO74PPB5V0
K5	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
K6	NC	IO75PDB5V0
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC
K11	GND	GND
K12	VCC	VCC
K13	GND	GND
K14	VCC	VCC
K15	GND	GND
K16	VCCFPGAIOB1	VCCFPGAIOB1
K17	NC	IO37NDB1V0
K18	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
K19	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
K20	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
K21	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
K22	GND	GND
L1	NC	IO73PDB5V0
L2	NC	IO73NDB5V0
L3	NC	IO72PPB5V0
L4	GND	GND
L5	NC	IO74NPB5V0
L6	NC	IO75NDB5V0
L7	VCCFPGAIOB5	VCCFPGAIOB5
L8	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
T1	GND	GND
T2	VCCMSSIOB4	VCCMSSIOB4
T3	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO57RSB4V0	GPIO_11/IO66RSB4V0
T5	GND	GND
T6	MAC_CLK	MAC_CLK
T7	VCCMSSIOB4	VCCMSSIOB4
T8	VCC33SDD0	VCC33SDD0
T9	VCC15A	VCC15A
T10	GNDAQ	GNDAQ
T11	GND33ADC0	GND33ADC0
T12	ADC7	ADC7
T13	NC	TM4
T14	NC	VAREF2
T15	VAREFOUT	VAREFOUT
T16	VCCMSSIOB2	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
T18	GND	GND
T19	NC	NC
T20	NC	NC
T21	VCCMSSIOB2	VCCMSSIOB2
T22	GND	GND
U1	GND	GND
U2	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO58RSB4V0	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4	VCCMSSIOB4
U5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
U6	NC	NC
U7	VCC33AP	VCC33AP
U8	VCC33N	VCC33N
U9	CM1	CM1
U10	VAREF0	VAREF0
U11	GND33ADC1	GND33ADC1
U12	ADC4	ADC4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 8 (continued)	The description of "In-application programming (IAP)" methodology was changed to state the difference for A2F060 and A2F500 compared to A2F200 (SAR 37808).	4-7
	The "Global I/O Naming Conventions" section is new (SARs 28996, 31147). The description for IO "User Pins" was revised accordingly and moved out of the table and into a new section: "User I/O Naming Conventions".	5-6, 5-6
	The descriptions for "MAINXIN" and "MAINXOUT" were revised to state how they should be handled if using an external RC network or clock input (SAR 32594).	5-8
	The description and type was revised for the "MSS_RESET_N" pin (SAR 34133).	5-9
	The "TQ144" section and pin table for A2F060 are new (SAR 36246).	5-18
Revision 7 (August 2011)	The title of the datasheet was changed from SmartFusion Intelligent Mixed Signal FPGAs to SmartFusion Customizable System-on-Chip (cSoC). Terminology throughout was changed accordingly. The term cSoC defines a category of devices that include at least FPGA fabric and a processor subsystem of some sort. It can also include any of the following: analog, SerDes, ASIC blocks, customer specific IP, or application-specific IP. SmartFusion is Microsemi's first cSoC (SAR 33071).	N/A
	The "SmartFusion cSoC Family Product Table" was revised to remove the note stating that the A2F060 device is under definition and subject to change (SAR 33070). A note was added for EMC, stating that it is not available on A2F500 for the PQ208 package (SAR 33041).	II
	The "SmartFusion cSoC Device Status" table was revised. The status for A2F060 CS288 and FG256 moved from Advance to Preliminary. A2F200 PQ208 and A2F500 PQ208 moved from Advance to Production (SAR 33069).	III
	The "Package I/Os: MSS + FPGA I/Os" table was revised. The number of direct analog inputs for A2F060 packages increased from 6 to 11. The number of MSS I/Os for the A2F060 FG256 package increased from 25 to 26 (SAR 33070). A note was added stating that EMC is not available for the A2F500 PQ208 package (SAR 33041).	III
	The note associated with the "SmartFusion cSoC System Architecture" diagram was corrected from "Architecture for A2F500" to "Architecture for A2F200" (SAR 32578).	V
	The Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 32151).	VI
	The "Security" section and "Secure Programming" section were updated to clarify that although no existing security measures can give an absolute guarantee, SmartFusion cSoCs implement the best security available in the industry (SAR 32865).	1-2, 4-9
	Storage temperature, T_{STG}, and junction temperature, T_J, were added to Table 2-1 • Absolute Maximum Ratings (SAR 30863).	2-1
	AC/DC characteristics for A2F060 were added to the "SmartFusion DC and Switching Characteristics" chapter (SAR 33132). The following tables were updated: Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V Table 2-98 • Analog Sigma-Delta DAC Table 2-100 • SPI Characteristics	 2-12 2-13 2-76 2-85 2-89

Revision	Changes	Page
Revision 3 (continued)	Two notes were added to the "Supply Pins" table (SAR 27109): 1. *The following supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* 2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	5-1
	The descriptions for the "VCC33N", "NCAP", and "PCAP" pins were revised to include information on what to do if analog SCB features and SDDs are not used (SAR 26744).	5-2, 5-9, 5-9
	Information was added to the "User Pins" table regarding tristating of used and unused GPIO pins. The IO portion of the table was revised to state that unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor (SAR 26890). Information was added regarding behavior of used I/O pins during power-up.	5-6
	The type for "EMC_RW_N" was changed from In/out to Out (SAR 25113).	5-12
	A note was added to the "Analog Front-End (AFE)" table stating that unused analog inputs should be grounded (SAR 26744).	5-14
	The "TQ144" section is new, with pin tables for A2F200 and A2F500 (SAR 27044).	5-18
	The "FG256" pin table was replaced and now includes "Handling When Unused" information (SAR 27709).	5-42
Revision 2 (May 2010)	Embedded nonvolatile flash memory (eNVM) was changed from "64 to 512 Kbytes" to "128 to 512 Kbytes" in the "Microcontroller Subsystem (MSS)" section and "SmartFusion cSoC Family Product Table" (SAR 26005).	I, II
	The main oscillator range of values was changed to "32 KHz to 20 MHz" in the "Microcontroller Subsystem (MSS)" section and the "SmartFusion cSoC Family Product Table" (SAR 24906).	I, II
	The value for t_{PD} was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the "Analog Front-End (AFE)" section (SAR 26005).	I
	The number of PLLs for A2F200 was changed from 2 to 1 in the "SmartFusion cSoC Family Product Table" (SAR 25093).	II
	Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the "Package I/Os: MSS + FPGA I/Os" table. The Max. column was removed from the table (SAR 26005).	III
	The Speed Grade section of the "Product Ordering Codes" table was revised (SAR 25257).	VI
Revision 1 (March 2010)	The "Product Ordering Codes" table was revised to add "blank" as an option for lead-free packaging and application (junction temperature range).	VI
	Table 2-3 • Recommended Operating Conditions[5,6] was revised. Ta (ambient temperature) was replaced with T_J (junction temperature).	2-3
	PDC5 was deleted from Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs.	2-13
	The formulas in the footnotes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised.	2-27
	The values for input biased current were revised in Table 2-93 • Current Monitor Performance Specification.	2-78
Revision 0 (March 2010)	The "Analog Front-End (AFE)" section was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps.	I

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