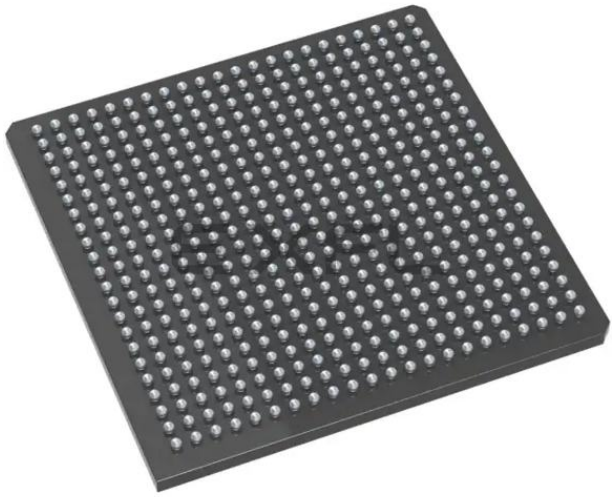

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-fgg484

Package I/Os: MSS + FPGA I/Os

Device	A2F060[1]			A2F200[2]				A2F500[2]			
Package	**TQ144**	**CS288**	**FG256**	**PQ208**	**CS288**	**FG256**	**FG484**	**PQ208**	**CS288**	**FG256**	**FG484**
Direct Analog Inputs	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Inputs	4	4	4	16	16	16	16	16	16	16	20
Total Analog Inputs	15	15	15	24	24	24	24	24	24	24	32
Analog Outputs	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[3,4]	21[5]	28[5]	26[5]	22	31	25	41	22	31	25	41
FPGA I/Os	33[6]	68	66	66	78	66	94	66[6]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:

1. *There are no LVTTL capable direct inputs available on A2F060 devices.*
2. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
3. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
4. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
5. *10/100 Ethernet MAC is not available on A2F060.*
6. *EMC is not available on the A2F500 PQ208 and A2F060 TQ144 package.*

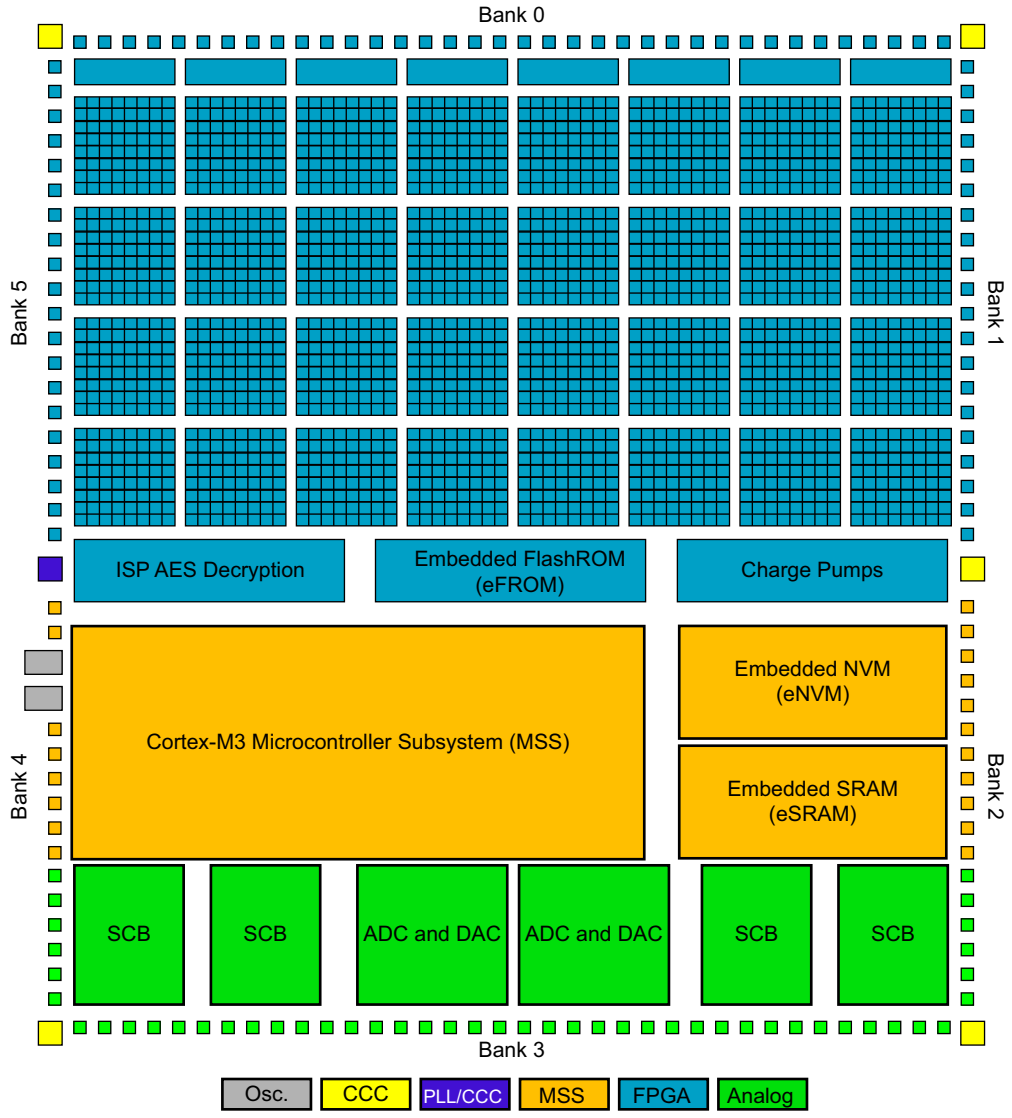
Table 1 • SmartFusion cSoC Package Sizes Dimensions

Package	TQ144	PQ208	CS288	FG256	FG484
Length × Width (mm\mm)	20 × 20	28 × 28	11 × 11	17 × 17	23 × 23
Nominal Area (mm^2)	400	784	121	289	529
Pitch (mm)	0.5	0.5	0.5	1.0	1.0
Height (mm)	1.40	3.40	1.05	1.60	2.23

SmartFusion cSoC Device Status

Device	Status
A2F060	Preliminary: CS288, FG256, TQ144
A2F200	Production: CS288, FG256, FG484, PQ208
A2F500	Production: CS288, FG256, FG484, PQ208

SmartFusion cSoC System Architecture



Note: Architecture for A2F200

This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

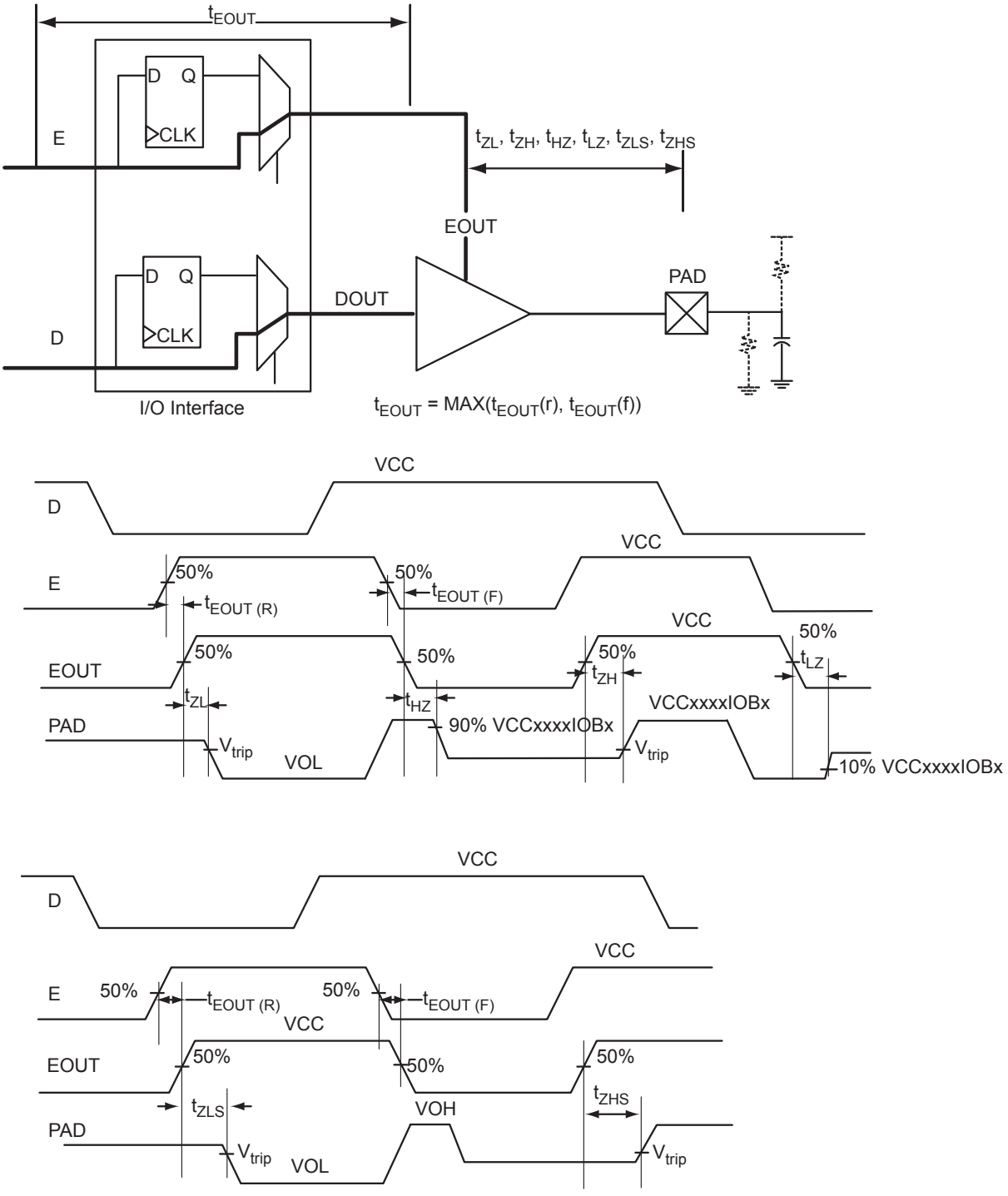


Figure 2-5 • **Tristate Output Buffer Timing Model and Delays (example)**

DDR Module Specifications

Input DDR Module

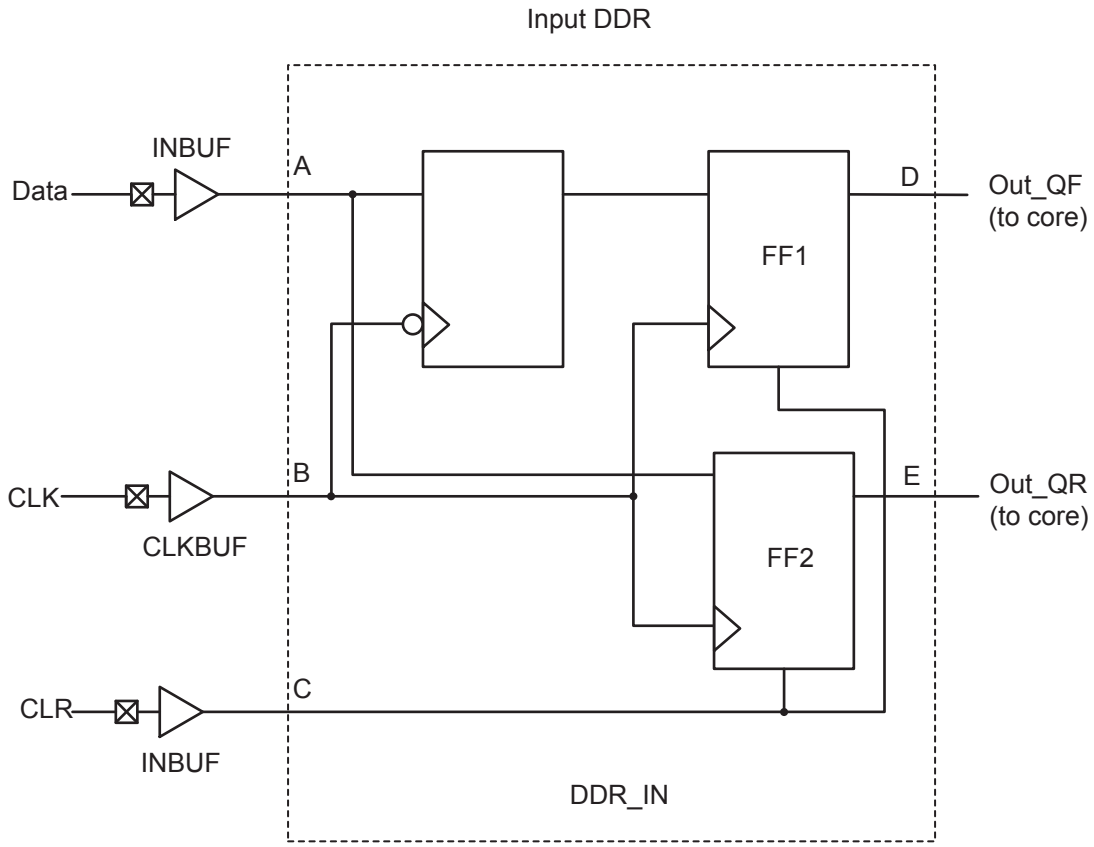


Figure 2-19 • **Input DDR Timing Model**

Table 2-74 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-86* • SmartFusion CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350[1]	MHz
Delay Increments in Programmable Delay Blocks[2,3,4]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		5.15	%
Delay Range in Block: Programmable Delay 1[2,3]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[2,3]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[2,3]		2.2		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6,7]	Maximum Peak-to-Peak Period Jitter			

	SSO ≤ 2		SSO ≤ 4		SSO ≤ 8		SSO ≤ 16	
	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*

FIFO

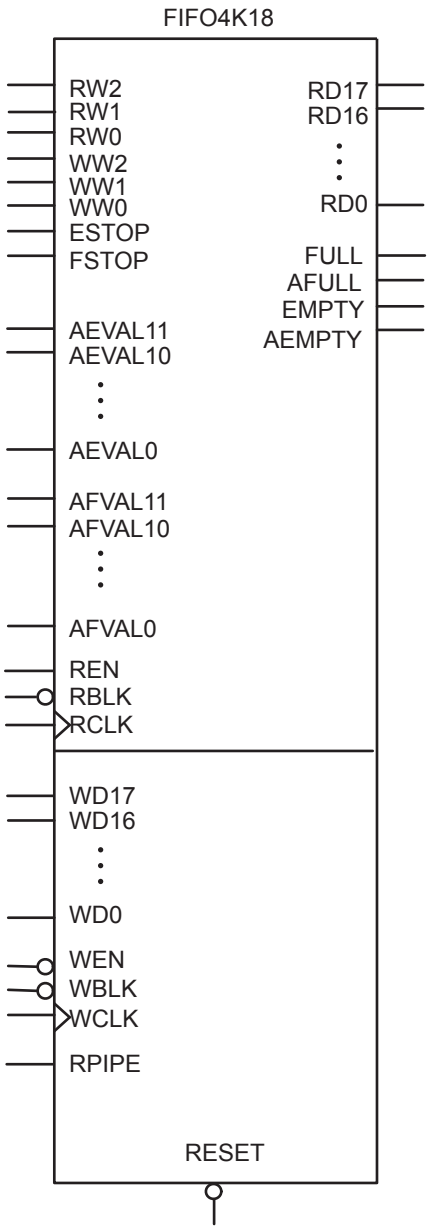


Figure 2-35 • **FIFO Model**

***Table 2-96* • ABPS Performance Specifications (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input referred offset voltage					
	GDEC[1:0] = 11	–0.31	–0.07	0.31	% FS*
	–40ºC to +100ºC	–1.00		1.47	% FS*
	GDEC[1:0] = 10	–0.34	–0.07	0.34	% FS*
	–40ºC to +100ºC	–0.90		1.37	% FS*
	GDEC[1:0] = 01	–0.61	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.05		1.35	% FS*
	GDEC[1:0] = 00	–0.39	–0.07	0.35	% FS*
	–40ºC to +100ºC	–1.06		1.38	% FS*
SINAD		53	56		dB
Non-linearity	RMS deviation from BFSL			0.5	% FS*
Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 11*	GDEC[1:0] = 11 (±2.56 range), –1 dBFS input				
	12-bit mode 10 KHz	8.6	9.1		Bits
	12-bit mode 100 KHz	8.6	9.1		Bits
	10-bit mode 10 KHz	8.5	8.9		Bits
	10-bit mode 100 KHz	8.5	8.9		Bits
	8-bit mode 10 KHz	7.7	7.8		Bits
	8-bit mode 100 KHz	7.7	7.8		Bits
Large-signal bandwidth	–1 dBFS input		1		MHz
Analog settling time	To 0.1% of final value (with ADC load)			10	µs
Input resistance			1		MΩ
Power supply rejection ratio	DC (0–1 KHz)	38	40		dB
ABPS power supply current requirements (not including ADC or VAREFx)	ABPS_EN = 1 (operational mode)				
	VCC33A		123	134	µA
	VCC33AP		89	94	µA
	VCC15A		1		µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Compile and Debug

Microsemi's SoftConsole is a free Eclipse-based IDE that enables the rapid production of C and C++ executables for Microsemi FPGA and cSoCs using Cortex-M3, Cortex-M1 and Core8051s. For SmartFusion support, SoftConsole includes the GNU C/C++ compiler and GDB debugger. Additional examples can be found on the SoftConsole page:

- Using UART with SmartFusion: SoftConsole Standalone Flow Tutorial
  - Design Files
- Displaying POT Level with LEDs: Libero SoC and SoftConsole Flow Tutorial for SmartFusion
  - Design Files

IAR Embedded Workbench® for ARM/Cortex is an integrated development environment for building and debugging embedded ARM applications using assembler, C and C++. It includes a project manager, editor, build and debugger tools with support for RTOS-aware debugging on hardware or in a simulator.

- Designing SmartFusion cSoC with IAR Systems
- IAR Embedded Workbench IDE User Guide for ARM
- Download Evaluation or Kickstart version of IAR Embedded Workbench for ARM

Keil's Microcontroller Development Kit comes in two editions: MDK-ARM and MDK Basic. Both editions feature µVision®, the ARM Compiler, MicroLib, and RTX, but the MDK Basic edition is limited to 256K so that small applications are more affordable.

- Designing SmartFusion cSoC with Keil
- Using Keil µVision and Microsemi SmartFusion cSoC
  - Programming file for use with this tutorial
- Keil Microcontroller Development Kit for ARM Product Manuals
- Download Evaluation version of Keil MDK-ARM

CMSIS COMPLIANT ARM® Cortex™ Microcontroller Software Interface Standard	Microsemi	KEIL™ An ARM® Company	IAR SYSTEMS
Software IDE	**SoftConsole**	**Vision IDE**	**Embedded Workbench**
Website	www.microsemi.com/soc	www.keil.com	www.iar.com
Free versions from SoC Products Group	Free with Libero SoC	32 K code limited	32 K code limited
Available from Vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView C/C++	IAR ARM Compiler
Debugger	GDB debug	Vision Debugger	C-SPY Debugger
Instruction Set Simulator	No	Vision Simulator	Yes
Debug Hardware	FlashPro4	ULINK2 or ULINK-ME	J-LINK or J-LINK Lite

Operating Systems

FreeRTOS™ is a portable, open source, royalty free, mini real-time kernel (a free-to-download and free-to-deploy RTOS that can be used in commercial applications without any requirement to expose your proprietary source code). FreeRTOS is scalable and designed specifically for small embedded systems. This FreeRTOS version ported by Microsemi is 6.0.1. For more information, visit the FreeRTOS website: www.freertos.org

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion cSoC: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

- Flash File System (RL-Flash) allows your embedded applications to create, save, read, and modify files in standard storage devices such as ROM, RAM, or FlashROM, using a standard serial peripheral interface (SPI). Many ARM-based microcontrollers have a practical requirement for a standard file system. With RL-FlashFS you can implement new features in embedded applications such as data logging, storing program state during standby modes, or storing firmware upgrades.

Micrium, in addition to µC/OS-III®, offers the following support for SmartFusion cSoC:

- µC/TCP-IP™ is a compact, reliable, and high-performance stack built from the ground up by Micrium and has the quality, scalability, and reliability that translates into a rapid configuration of network options, remarkable ease-of-use, and rapid time-to-market.
- µC/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running.

References

PCB Files

A2F500 SmartFusion Development Kit PCB Files

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130770

A2F200 SmartFusion Development Kit PCB Files

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130773

Application Notes

SmartFusion cSoC Board Design Guidelines

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129815

Name	Type	Polarity/Bus Size	Description
NCAP		1	Negative capacitor connection. This is the negative terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
PCAP		1	Positive Capacitor connection. This is the positive terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used.
PTBASE		1	Pass transistor base connection This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
PTEM		1	Pass transistor emitter connection. This is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
MSS_RESET_N		Low	Low Reset signal which can be used as an external reset and can also be used as a system level reset under control of the Cortex-M3 processor. MSS_RESET_N is an output asserted low after power-on reset. The direction of MSS_RESET_N changes during the execution of the Microsemi System Boot when chip-level reset is enabled. The Microsemi System Boot reconfigures MSS_RESET_N to become a reset input signal when chip-level reset is enabled. It has an internal pull-up so it can be left floating. In the current software, the MSS_RESET_N is modeled as an external input signal only.
PU_N	In	Low	Push-button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
M21	TRSTB	TRSTB	TRSTB
N1	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
N3	GND	GND	GND
N5	GPIO_4/IO29RSB4V0	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
N6	GPIO_8/IO25RSB4V0	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
N7	GPIO_9/IO24RSB4V0	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
N8	VCC	VCC	VCC
N9	GND	GND	GND
N10	VCC	VCC	VCC
N11	GND	GND	GND
N12	VCC	VCC	VCC
N13	GND	GND	GND
N14	VCC	VCC	VCC
N15	GND	GND	GND
N16	TCK	TCK	TCK
N17	TDI	TDI	TDI
N19	GNDENVM	GNDENVM	GNDENVM
N21	VCCENVM	VCCENVM	VCCENVM
P1	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
P3	GPIO_7/IO26RSB4V0	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0
P5	GPIO_6/IO27RSB4V0	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
P6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
P8	GND	GND	GND
P9	VCC	VCC	VCC
P10	GND	GND	GND
P11	VCC	VCC	VCC
P12	GND	GND	GND
P13	VCC	VCC	VCC
P14	GND	GND	GND
P16	JTAGSEL	JTAGSEL	JTAGSEL
P17	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23

Notes:

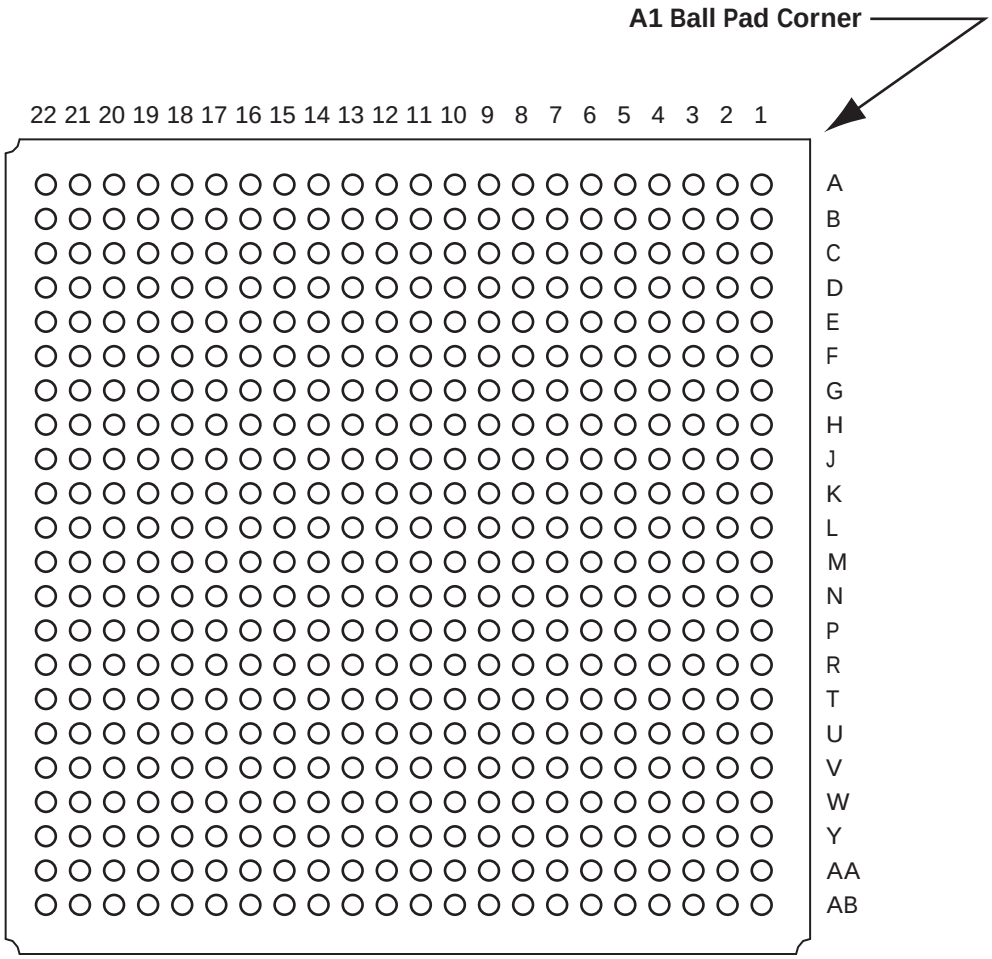
1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
M11	ADC6	TM2	TM2
M12	ADC5	CM2	CM2
M13	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
M14	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
M15	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
M16	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
N1	GPIO_8/IO25RSB4V0	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
N2	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
N3	VCC15A	VCC15A	VCC15A
N4	VCC33AP	VCC33AP	VCC33AP
N5	NC	ABPS3	ABPS3
N6	ADC4	TM1	TM1
N7	NC	GND33ADC0	GND33ADC0
N8	VCC33ADC0	VCC33ADC1	VCC33ADC1
N9	ADC8	ADC5	ADC5
N10	CM0	CM3	CM3
N11	GNDAQ	GNDAQ	GNDAQ
N12	VAREFOUT	VAREFOUT	VAREFOUT
N13	NC	GNDSDD1	GNDSDD1
N14	NC	VCC33SDD1	VCC33SDD1
N15	GND	GND	GND
N16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
P1	GNDSDD0	GNDSDD0	GNDSDD0
P2	VCC33SDD0	VCC33SDD0	VCC33SDD0
P3	VCC33N	VCC33N	VCC33N
P4	GNDA	GNDA	GNDA
P5	GNDAQ	GNDAQ	GNDAQ
P6	NC	CM1	CM1
P7	NC	ADC2	ADC2
P8	NC	VCC15ADC0	VCC15ADC0
P9	ADC9	ADC6	ADC6

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
W3	GND	GND
W4	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
W5	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
W6	NC	SDD2
W7	GNDA	GNDA
W8	TM0	TM0
W9	ABPS2	ABPS2
W10	GND33ADC0	GND33ADC0
W11	VCC15ADC1	VCC15ADC1
W12	ABPS6	ABPS6
W13	NC	CM4
W14	NC	ABPS9
W15	NC	VCC33ADC2
W16	GNDA	GNDA
W17	PU_N	PU_N
W18	GNDSDD1	GNDSDD1
W19	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
W20	GND	GND
W21	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
W22	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
Y1	GPIO_3/IO44RSB4V0	GPIO_3/IO53RSB4V0
Y2	VCCMSSIOB4	VCCMSSIOB4
Y3	GPIO_15/IO34RSB4V0	GPIO_15/IO43RSB4V0
Y4	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
Y5	VCCMSSIOB4	VCCMSSIOB4
Y6	GNDSDD0	GNDSDD0
Y7	CM0	CM0
Y8	GNDTM0	GNDTM0
Y9	ADC0	ADC0
Y10	VCC15ADC0	VCC15ADC0
Y11	ABPS7	ABPS7
Y12	TM3	TM3
Y13	NC	ABPS8
Y14	NC	GND33ADC2

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

6 – Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 13 (March 2015)	Updated Unused MSS I/O Configuration information in "User I/O Naming Conventions" (SAR 62994).	5-7
	Updated Table 2-90: "eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V". Changed the maximum clock frequency for the control logic – 5 cycles to 50 MHz for A2F060 and A2F200 devices (SAR 63920). Added the following Note: "Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%" (SAR 63920).	2-76
Revision 12 (November 2013)	CS288 package dimensions added to "SmartFusion cSoC Package Sizes Dimensions" table (SAR 43730).	1-III
	Added "Typical Programming and Erase Times" table (SAR 43732).	4-9
	Definition of Ethernet MAC clarified in the "General Description" section (SAR 50083).	1-1
	Clarified GC and GF global inputs in "Global I/O Naming Conventions" section and link to SF Fabric UG added (SAR 42802).	5-6
Revision 11 (September 2013)	Modified the description for VAREF0 in the "User-Defined Supply Pins"(SAR 30204).	5-5
	Updated the "Pin Assignment Tables" section with a note for A2F500, all packages with GCAx saying: "Signal assigned to those pins as a CLKBUF or CLKBUF_LVPECL or CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal (SAR 45985).	5-18

Revision	Changes	Page
Revision 6 (continued)	Dynamic power values were updated in the following tables. The table subtitles changed where FPGA I/O banks were involved to note "I/O assigned to EMC I/O pins" (SAR 30987). Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings.	2-10 2-11
	The "Timing Model" was updated (SAR 30986).	2-19
	Values in the timing tables for the following sections were updated. Table subtitles were updated for FPGA I/O banks to note "I/O assigned to EMC I/O pins" (SAR 30986). "Overview of I/O Performance" section: Table 2-24, Table 2-25 "Detailed I/O DC Characteristics" section: Table 2-38, Table 2-39, Table 2-40, Table 2-44, Table 2-45, Table 2-46, Table 2-50, Table 2-51, Table 2-52, Table 2-56, Table 2-57, Table 2-58, Table 2-61, Table 2-62 "LVDS" section: Table 2-65 "LVPECL" section: Table 2-68 "Global Tree Timing Characteristics" section: Table 2-80, Table 2-81	2-23 2-26 2-40 2-42 2-59
	The "PQ208" section and pin tables are new (SAR 31005).	5-34
	Global clocks were removed from the A2F060 pin table for the "CS288" and "FG256" packages, resulting in changed function names for affected pins (SAR 31033).	5-43
Revision 5 (December 2010)	Table 2-2 • Analog Maximum Ratings was revised. The recommended CM[n] pad voltage (relative to ground) was changed from –11 to –0.3 (SAR 28219).	2-2
	Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays was revised to change the values for 100ºC.	2-9
	Power-down and Sleep modes, and all associated notes, were removed from Table 2-8 • Power Supplies Configuration (SAR 29479). IDC3 and IDC4 were renamed to IDC1 and IDC2 (SAR 29478). These modes are no longer supported. A note was added to the table stating that current monitors and temperature monitors should not be used when Power-down and/or Sleep mode are required by the application.	2-10
	The "Power-Down and Sleep Mode Implementation" section was deleted (SAR 29479).	N/A
	Values for PAC9 and PAC10 for LVDS and LVPECL were revised in Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings*.	2-10, 2-11
	Values for PAC1 through PAC4, PDC1, and PDC2 were added for A2F500 in Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs	2-12, 2-13
	The equation for "Total Dynamic Power Consumption—P_{DYN}" in "SoC Mode" was revised to add P_{MSS}. The "Microcontroller Subsystem Dynamic Contribution—P_{MSS}" section is new (SAR 29462).	2-14, 2-18
	Information in Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to FPGA I/O banks) and Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to MSS I/O banks) was updated.	2-25

Revision	Changes	Page
Revision 3 (continued)	In Table 2-3 • Recommended Operating Conditions[5,6], the VDDBAT recommended operating range was changed from "2.97 to 3.63" to "2.7 to 3.63" (SAR 25246). Recommended operating range was changed to "3.15 to 3.45" for the following voltages: VCC33A VCC33ADCx VCC33AP VCC33SDDx VCCMAINXTAL VCCLPXTAL Two notes were added to the table (SAR 27109): 1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* 2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	2-3
	In Table 2-3 • Recommended Operating Conditions[5,6], the description for VCCLPXTAL was corrected to change "32 Hz" to "32 KHz" (SAR 27110).	2-3
	The "Power Supply Sequencing Requirement" section is new (SAR 27178).	2-4
	Table 2-8 • Power Supplies Configuration was revised to change most on/off entries to voltages. Note 5 was added, stating that "on" means proper voltage is applied. The values of 6 µA and 16 µA were removed for IDC1 and IDC2 for 3.3 V. A note was added for IDC1 and IDC2: "Power mode and Sleep mode are consuming higher current than expected in the current version of silicon. These specifications will be updated when new version of the silicon is available" (SAR 27926).	2-10
	The "Power-Down and Sleep Mode Implementation" section is new (SAR 27178).	2-11
	A note was added to Table 2-86 • SmartFusion CCC/PLL Specification, pertaining to f_{out_CCC}, stating that "one of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software" (SAR 26388).	2-63
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised. Values were included for A2F200 and A2F500, for –1 and Std. speed grades. A note was added to define 6:1:1:1 and 5:1:1:1 (SAR 26166).	2-76
	The units were corrected (mV instead of V) for input referred offset voltage, GDEC[1:0] = 00 in Table 2-96 • ABPS Performance Specifications (SAR 25381).	2-82
	The test condition values for operating current (ICC33A, typical) were changed in Table 2-99 • Voltage Regulator (SAR 26465).	2-87
	Figure 2-45 • Typical Output Voltage was revised to add legends for the three curves, stating the load represented by each (SAR 25247).	2-88
	The "SmartFusion Programming" chapter was moved to this document from the SmartFusion Subsystem Microcontroller User's Guide (SAR 26542). The "Typical Programming and Erase Times" section was added to this chapter.	4-7
	Figure 4-1 • TRSTB Logic was revised to change 1.5 V to "VJTAG (1.5 V to 3.3 V nominal)" (SAR 24694).	4-8