Microchip Technology - A2F200M3F-PQG208 Datasheet

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-pqg208

Datasheet Categories 6-14
Microsemi SoC Products Group Safety Critical, Life Support, and High-Reliability Applications Policy 6-14

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 85°C, worst-case VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.425	0.86	0.91	0.93	0.98	1.00	1.02
1.500	0.81	0.86	0.88	0.93	0.95	0.96
1.575	0.78	0.83	0.85	0.90	0.91	0.93

Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03			mW
PAC25	ABPS Power Contribution	See Table 2-96 on page 2-82	–	0.70			mW
PAC26	Sigma-Delta DAC Power Contribution[2]	See Table 2-98 on page 2-85	–	0.58			mW
PAC27	Comparator Power Contribution	See Table 2-97 on page 2-84	–	1.02			mW
PAC28	Voltage Regulator Power Contribution[3]	See Table 2-99 on page 2-87	–	36.30			mW

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Assumes Input = Half Scale Operation mode.*
3. *Assumes 100 mA load on 1.5 V domain.*

Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F200	
PDC1	Core static power contribution in SoC mode	VCC	1.5 V	11.10	23.70	37.95	mW
PDC2	Device static power contribution in Standby Mode	See Table 2-8 on page 2-10	–	11.10	23.70	37.95	mW
PDC3	Device static power contribution in Time Keeping mode	See Table 2-8 on page 2-10	3.3 V	33.00	33.00	33.00	µW
PDC7	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11.				
PDC8	Static contribution per output pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11.				
PDC9	Static contribution per PLL	VCC	1.5 V	2.55	2.55	2.55	mW

Table 2-16 • eNVM Dynamic Power Consumption

Parameter	Description	Condition	Min.	Typ.	Max.	Units
eNVM System	eNVM array operating power	Idle		795		µA
		Read operation	See Table 2-14 on page 2-12.			
		Erase		900		µA
		Write		900		µA
PNVMCTRL	eNVM controller operating power			20		µW/MHz

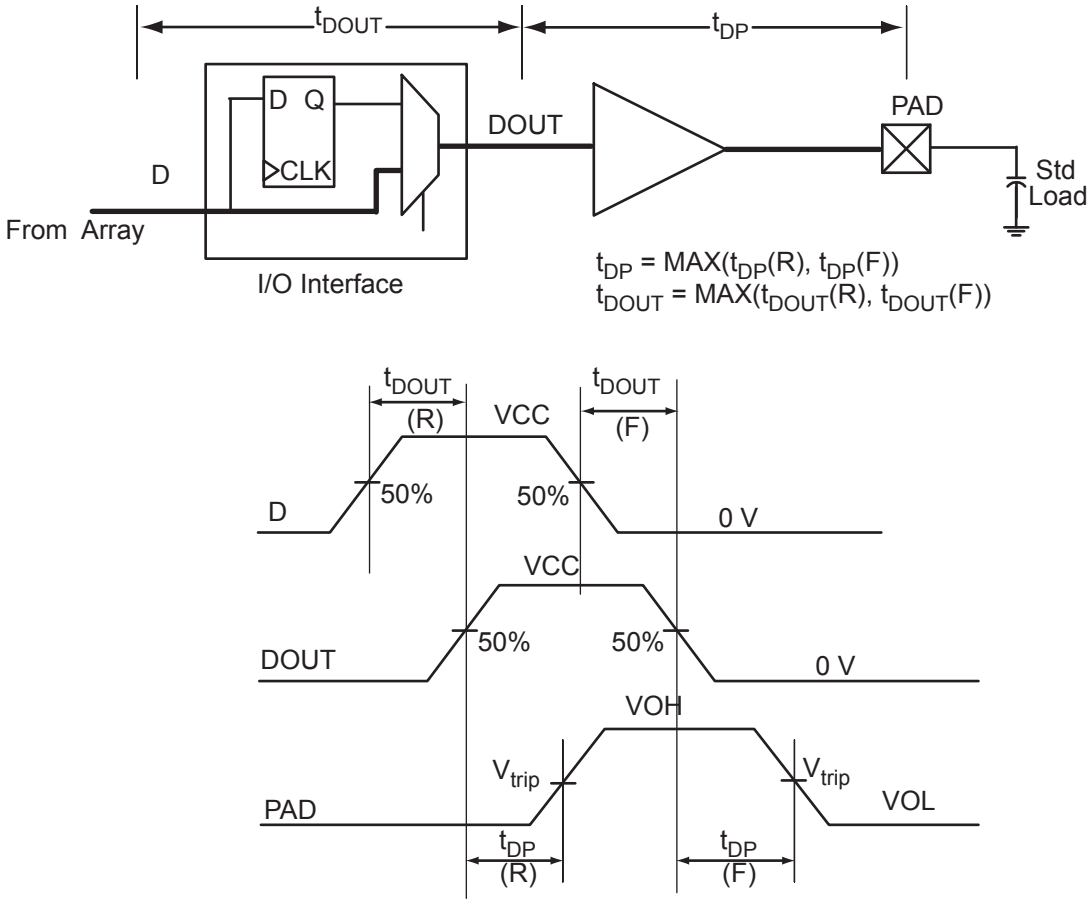

Figure 2-4 • **Output Buffer Model and Delays (example)**

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-59 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in Figure 2-10.

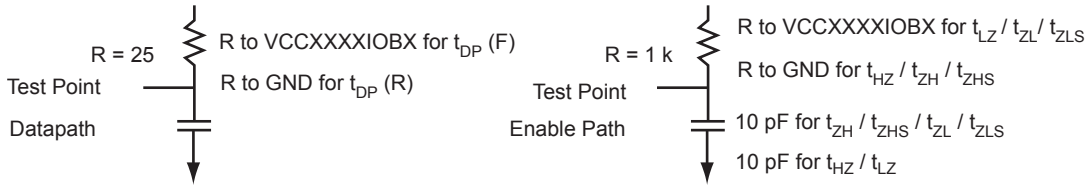

Figure 2-10 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in Table 2-60.

Table 2-60 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCxxxxIOBx for $t_{DP(R)}$ 0.615 * VCCxxxxIOBx for $t_{DP(F)}$	–	10

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-61 • 3.3 V PCI
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.54	0.04	0.82	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-62 • 3.3 V PCI-X
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.54	0.04	0.77	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

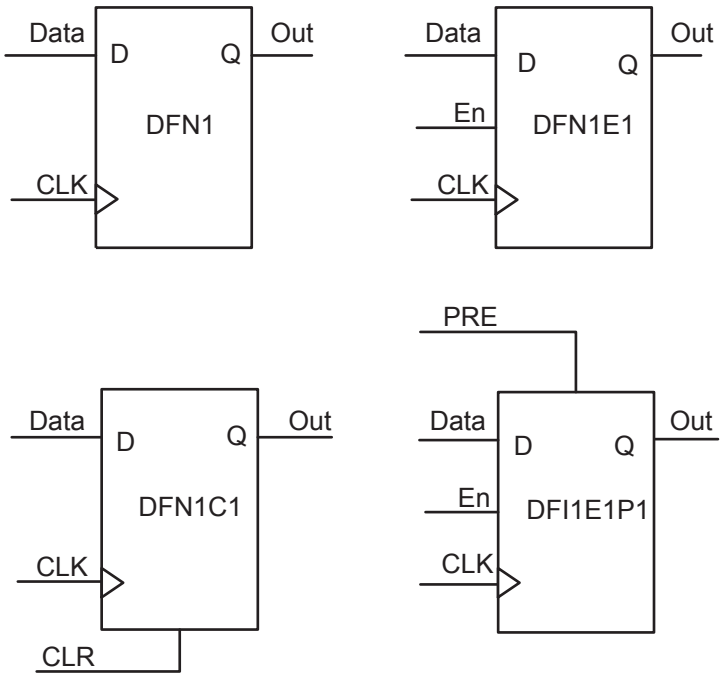

Figure 2-25 • Sample of Sequential Cells

Global Resource Characteristics

A2F200 Clock Tree Topology

Clock delays are device-specific. Figure 2-27 is an example of a global tree used for clock routing. The global tree presented in Figure 2-27 is driven by a CCC located on the west side of the A2F200 device. It is used to drive all D-flip-flops in the device.

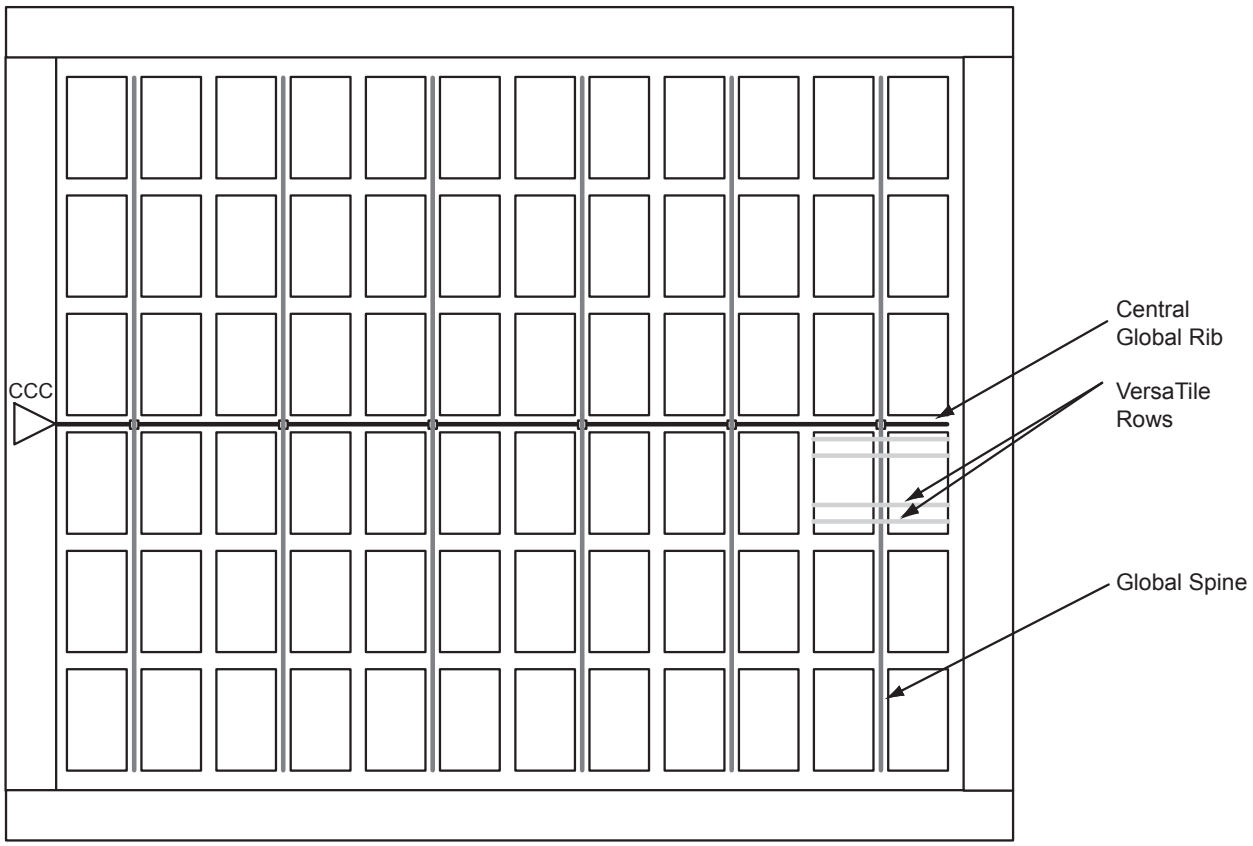

Figure 2-27 • **Example of Global Tree Use in an A2F200 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-63. Table 2-80 through Table 2-82 on page 2-61 present minimum and maximum global clock delays for the SmartFusion cSoCs. Minimum and maximum delays are measured with minimum and maximum loading.

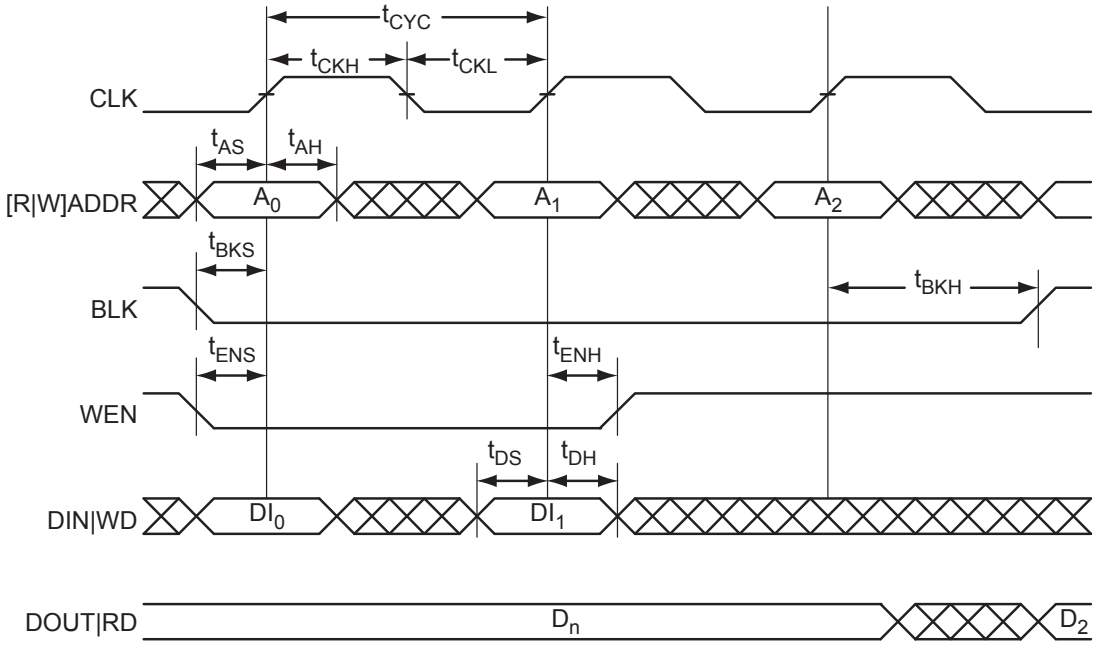

Figure 2-32 • **RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.**

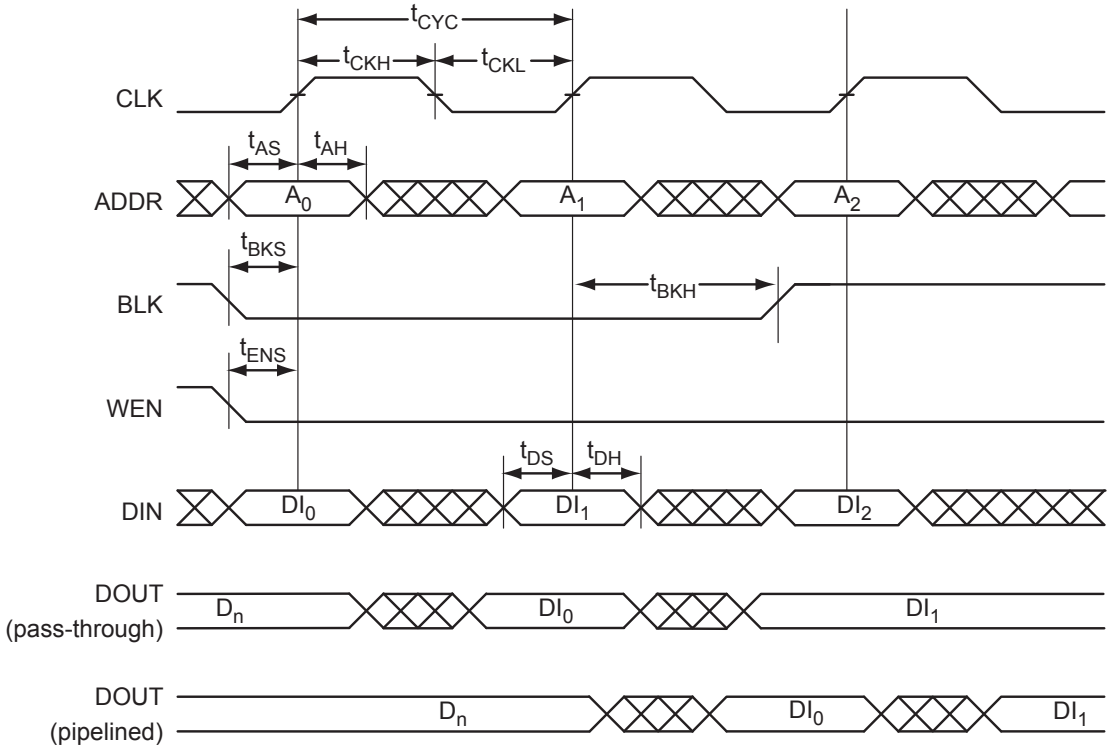

Figure 2-33 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

***Table 2-98* • Analog Sigma-Delta DAC (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Sigma-delta DAC power supply current requirements (not including VAREFx)	Input = 0, EN = 1 (operational mode)				
	VCC33SDDx		30	35	µA
	VCC15A		3	5	µA
	Input = Half scale, EN = 1 (operational mode)				
	VCC33SDDx		160	165	µA
	VCC15A		33	35	µA
	Input = Full scale, EN = 1 (operational mode)				
	VCC33SDDx		280	285	µA
	VCC15A		70	75	µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

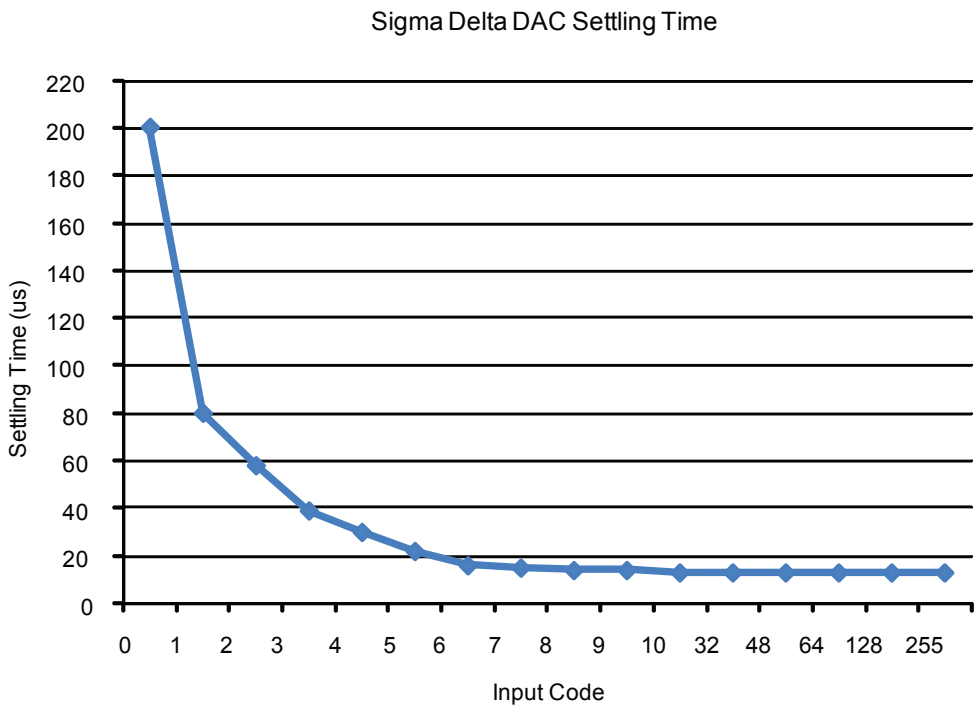

***Figure 2-44* • Sigma-Delta DAC Setting Time**

SmartFusion Ecosystem

The Microsemi SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in Figure 3-3.

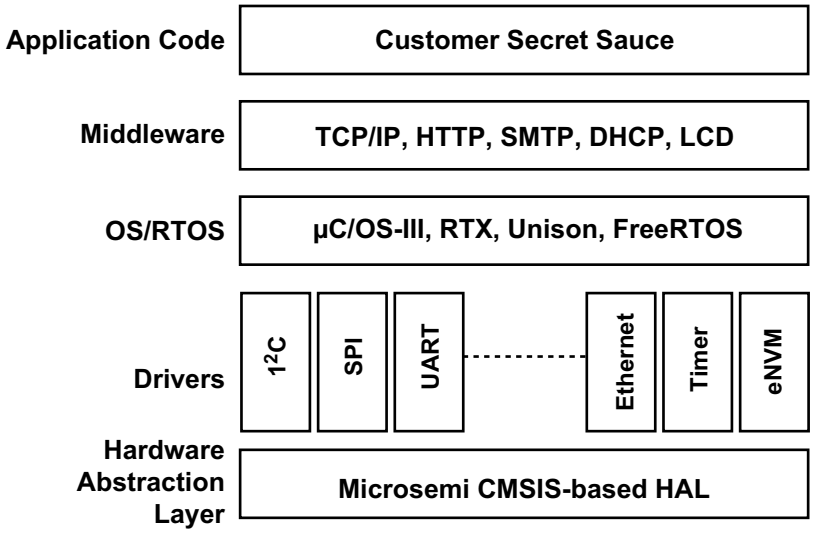

Figure 3-3 • **SmartFusion Ecosystem**

Figure 3-3 shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

ARM

Because an ARM processor was chosen for SmartFusion cSoCs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers* White Paper

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

4 – SmartFusion Programming

SmartFusion cSoCs have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
   a. A2F060 and A2F500: The FPGA fabric, eNVM, and eFROM
   b. A2F200: Only the FPGA fabric and the eNVM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. Table 4-1 describes the JTAG programming hardware that will program a SmartFusion cSoC and Table 4-2 defines the JTAG pins that provide the interface for the programming hardware.

***Table 4-1* • Supported JTAG Programming Hardware**

Dongle	Source	JTAG	SWD[1]	SWV[2]	Program FPGA	Program eFROM	Program eNVM
FlashPro3/4	SoC Products Group	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes

Notes:

1. *SWD = ARM Serial Wire Debug*
2. *SWV = ARM Serial Wire Viewer*
3. *Planned support*

***Table 4-2* • JTAG Pin Descriptions**

Pin Name	Description
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

Name	Type	Description
VCC15A	Supply	Clean analog 1.5 V supply to the analog circuitry. Always power this pin.
VCC15ADC0	Supply	Analog 1.5 V supply to the first ADC. Always power this pin.
VCC15ADC1	Supply	Analog 1.5 V supply to the second ADC. Always power this pin.
VCC15ADC2	Supply	Analog 1.5 V supply to the third ADC. Always power this pin.
VCC33A	Supply	Clean 3.3 V analog supply to the analog circuitry. VCC33A is also used to feed the 1.5 V voltage regulator for designs that do not provide an external supply to VCC. Refer to the Voltage Regulator (VR), Power Supply Monitor (PSM), and Power Modes section in the *SmartFusion Microcontroller Subsystem User's Guide* for more information.
VCC33ADC0	Supply	Analog 3.3 V supply to the first ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33ADC1	Supply	Analog 3.3 V supply to the second ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33ADC2	Supply	Analog 3.3 V supply to the third ADC. If unused, Microsemi recommends connecting this pin to a 3.3 V supply.[1]
VCC33AP	Supply	Analog clean 3.3 V supply to the charge pump. To avoid high current draw, VCC33AP should be powered up simultaneously with or after VCC33A. Can be pulled down if unused.[1]
VCC33N	Supply	–3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to GND. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
VCC33SDD0	Supply	Analog 3.3 V supply to the first sigma-delta DAC
VCC33SDD1	Supply	Common analog 3.3 V supply to the second and third sigma-delta DACs
VCCENVM	Supply	Digital 1.5 V power supply to the embedded nonvolatile memory blocks. To avoid high current draw, VCC should be powered up before or simultaneously with VCCENVM.
VCCESRAM	Supply	Digital 1.5 V power supply to the embedded SRAM blocks. Available only on the 208PQFP package. It should be connected to VCC (in other packages, it is internally connected to VCC).
VCCFPGAIOB0	Supply	Digital supply to the FPGA fabric I/O bank 0 (north FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB1	Supply	Digital supply to the FPGA fabric I/O bank 1 (east FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Name	Type	Description
VJTAG	Supply	Digital supply to the JTAG controller SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the V_{JTAG} pin together with the TRSTB pin could be tied to GND. Note that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a SmartFusion cSoC is in a JTAG chain of interconnected boards and it is desired to power down the board containing the device, this can be done provided both VJTAG and VCC to the device remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode. See "JTAG Pins" section on page 5-10.
VPP	Supply	Digital programming circuitry supply SmartFusion cSoCs support single-voltage in-system programming (ISP) of the configuration flash, embedded FlashROM (eFROM), and embedded nonvolatile memory (eNVM). For programming, VPP should be in the 3.3 V ± 5% range. During normal device operation, VPP can be left floating or can be tied to any voltage between 0 V and 3.6 V. When the VPP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry. For proper programming, 0.01µF, and 0.1µF to 1µF capacitors, (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
A1	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A2	GNDQ	GNDQ	GNDQ
A3	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
A4	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
A5	GND	GND	GND
A6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
A7	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
A8	EMC_AB[0]/IO04NPB0V0	EMC_AB[0]/IO04NPB0V0	EMC_AB[0]/IO06NPB0V0
A9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A10	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
A11	EMC_AB[8]/IO08NPB0V0	EMC_AB[8]/IO08NPB0V0	EMC_AB[8]/IO13NPB0V0
A12	EMC_AB[14]/IO11NPB0V0	EMC_AB[14]/IO11NPB0V0	EMC_AB[14]/IO15NPB0V0
A13	GND	GND	GND
A14	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
A15	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
A17	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A18	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A19	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
A20	GNDQ	GNDQ	GNDQ
A21	GND	GND	GND
AA1	ADC1	ABPS1	ABPS1
AA2	GNDAQ	GNDAQ	GNDAQ
AA3	GNDA	GNDA	GNDA
AA4	VCC33N	VCC33N	VCC33N
AA5	SDD0	SDD0	SDD0
AA6	ADC0	ABPS0	ABPS0
AA7	NC	GNDTM0	GNDTM0
AA8	NC	ABPS2	ABPS2
AA9	NC	VAREF0	VAREF0
AA10	NC	GND15ADC0	GND15ADC0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
C21	IO17NDB0V0	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
D1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
D3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D19	GND	GND	GND
D21	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E3	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E5	GNDQ	GNDQ	GNDQ
E6	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
E7	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
E8	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
E9	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
E10	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
E11	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
E12	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
E13	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
E14	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
E15	GCC0/IO18NPB0V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
E16	GCA1/IO20PPB0V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E17	GCC1/IO18PPB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
E19	GCB2/IO22PPB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
E21	IO21NDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
F1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F5	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
F6	EMC_DB[11]/IO43PDB5V0	EMC_DB[11]/IO69PDB5V0	EMC_DB[11]/IO86PDB5V0
F7	GND	GND	GND
F8	NC	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
F9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
F10	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
F11	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

PQ208

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Revision	Changes	Page
Revision 7 (continued)	Usage instructions, such as how to handle the pin when unused, were added for the following supply pins (SAR 29769): "VCC15A" "VCC15ADC0" through "VCC15ADC2" "VCC33ADC0" through "VCC33ADC2" "VCC33AP" "VCC33ADC2" "VCCLPXTAL" "VCCMAINXTAL" "VCCMSSIOB2" "VCCPLLx" "VCCRCOSC" "VDDBAT"	5-2 through 5-3
	The "IO" description was revised to clarify the definitions of u, I/O pair, and w, differential pair (SAR 31147). Information on configuration of unused I/Os (including unused MSS I/Os, SAR 26891) was added (SAR 32643).	5-6
	Usage instructions were added for the following pins (SAR 29769): "MSS_RESET_N" "TCK" "TMS" "TRSTB" "MAC_CLK"	5-9 through 5-13
	Package names used in the "Pin Assignment Tables" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	5-18
	The pin assignments for A2F060 for "TQ144" and "FG256" have been revised due to the device status change from advance to preliminary (SAR 33068). The "TQ144" and "FG256" pin assignment sections previously compared functions between A2F060/A2F200 devices in one table and A2F200/A2F500 in a separate table. Functions for all three devices have now been combined into one table for each package (SAR 33072).	5-18, 5-42
	The "PQ208" pin table was revised for A2F500 to remove EMC functions, which are not available for this device/package combination (SAR 33041).	5-34
Revision 6 (March 2011)	The "PQ208" package was added to product tables and "Product Ordering Codes" for A2F200 and A2F500 (SAR 31005).	III
	The "Package I/Os: MSS + FPGA I/Os" table was revised to add the CS288 package for A2F060 and the PQ208 package for A2F200 and A2F500. A row was added for shared analog inputs (SAR 31034).	III
	The "SmartFusion cSoC Device Status" table was updated (SAR 31084).	III
	VCCESRAM was added to Table 2-1 • Absolute Maximum Ratings, Table 2-3 • Recommended Operating Conditions[5,6], Table 2-8 • Power Supplies Configuration, and the "Supply Pins" table (SAR 31035).	2-1, 2-3, 2-10, 5-1
	The following note was removed from Table 2-8 • Power Supplies Configuration (SAR 30984): "Current monitors and temperature monitors should not be used when Power-Down and/or Sleep mode are required by the application."	2-10

Revision	Changes	Page
Revision 5 (continued)	Available values for the Std. speed were added to the timing tables from Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew to Table 2-92 • JTAG 1532 (SAR 29331). One or more values changed for the –1 speed in tables covering 3.3 V LVCMOS, 2.5 V LVCMOS, 1.8 V LVCMOS, 1.5 V LVCMOS, Combinatorial Cell Propagation Delays, and A2F200 Global Resources.	2-31 to 2-76
	Table 2-80 • A2F500 Global Resource is new.	2-60
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised (SAR 27585).	2-76
	The programmable analog specifications tables were revised with updated information.	2-78 to 2-87
	Table 4-1 • Supported JTAG Programming Hardware was revised by adding a note to indicate "planned support" for several of the items in the table.	4-7
	The note on JTAGSEL in the "In-System Programming" section was revised to state that SoftConsole selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care" (SAR 29261).	4-7
	The "CS288" and "FG256" pin tables for A2F060 are new, comparing the A2F060 function with the A2F200 function (SAR 29353).	5-24
	The "Handling When Unused" column was removed from the "FG256" pin table for A2F200 and A2F500 (SAR 29691).	5-42
Revision 4 (September 2010)	Table 2-8 • Power Supplies Configuration was revised. VCCRCOSC was moved to a column of its own with new values. VCCENVM was added to the table. Standby mode for VJTAG and VPP was changed from 0 V to N/A. "Disable" was changed to "Off" in the eNVM column. The column for RCOSC was deleted.	2-10
	The "Power-Down and Sleep Mode Implementation" section was revised to include VCCROSC.	2-11
Revision 3 (September 2010)	The "I/Os and Operating Voltage" section was revised to list "single 3.3 V power supply with on-chip 1.5 V regulator" and "external 1.5 V is allowed" (SAR 27663).	I
	The CS288 package was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 27101), "Product Ordering Codes" table, and "Temperature Grade Offerings" table (SAR 27044). The number of direct analog inputs for the FG256 package in A2F060 was changed from 8 to 6.	III, VI, VI
	Two notes were added to the "SmartFusion cSoC Family Product Table" indicating limitations for features of the A2F500 device: *Two PLLs are available in CS288 and FG484 (one PLL in FG256).* *[ADCs, DACs, SCBs, comparators, current monitors, and bipolar high voltage monitors are] Available on FG484 only. FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.* Table cells were merged in rows containing the same values for easier reading (SAR 24748).	II
	The security feature option was added to the "Product Ordering Codes" table.	VI