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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 200K Gates, 4608 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f200m3f-pqg208i

SmartFusion Family Overview

SmartFusion DC and Switching Characteristics

SmartFusion Development Tools

SmartFusion Programming

Pin Descriptions

Datasheet Information

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 2-6 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
A2F200M3F-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
A2F200M3F-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
A2F200M3F-CS288	26.6	20.2	18.1	7.3	9.4	°C/W
A2F200M3F-PQG208I	38.5	34.6	33.1	0.7	31.6	°C/W

Table 2-14 • **Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03			mW
PAC25	ABPS Power Contribution	See Table 2-96 on page 2-82	–	0.70			mW
PAC26	Sigma-Delta DAC Power Contribution[2]	See Table 2-98 on page 2-85	–	0.58			mW
PAC27	Comparator Power Contribution	See Table 2-97 on page 2-84	–	1.02			mW
PAC28	Voltage Regulator Power Contribution[3]	See Table 2-99 on page 2-87	–	36.30			mW

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Assumes Input = Half Scale Operation mode.*
3. *Assumes 100 mA load on 1.5 V domain.*

Table 2-15 • **Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F200	
PDC1	Core static power contribution in SoC mode	VCC	1.5 V	11.10	23.70	37.95	mW
PDC2	Device static power contribution in Standby Mode	See Table 2-8 on page 2-10	–	11.10	23.70	37.95	mW
PDC3	Device static power contribution in Time Keeping mode	See Table 2-8 on page 2-10	3.3 V	33.00	33.00	33.00	µW
PDC7	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11.				
PDC8	Static contribution per output pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11.				
PDC9	Static contribution per PLL	VCC	1.5 V	2.55	2.55	2.55	mW

Table 2-16 • **eNVM Dynamic Power Consumption**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
eNVM System	eNVM array operating power	Idle		795		µA
		Read operation	See Table 2-14 on page 2-12.			
		Erase		900		µA
		Write		900		µA
PNVMCTRL	eNVM controller operating power			20		µW/MHz

Microcontroller Subsystem Dynamic Contribution—P_{MSS}

SoC Mode

$P_{MSS} = P_{AC22}$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 2-17 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-18 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	Toggle rate of the logic driving the output buffer
β_2	FPGA fabric SRAM enable rate for read operations	12.5%
β_3	FPGA fabric SRAM enable rate for write operations	12.5%
β_4	eNVM enable rate for read operations	< 5%

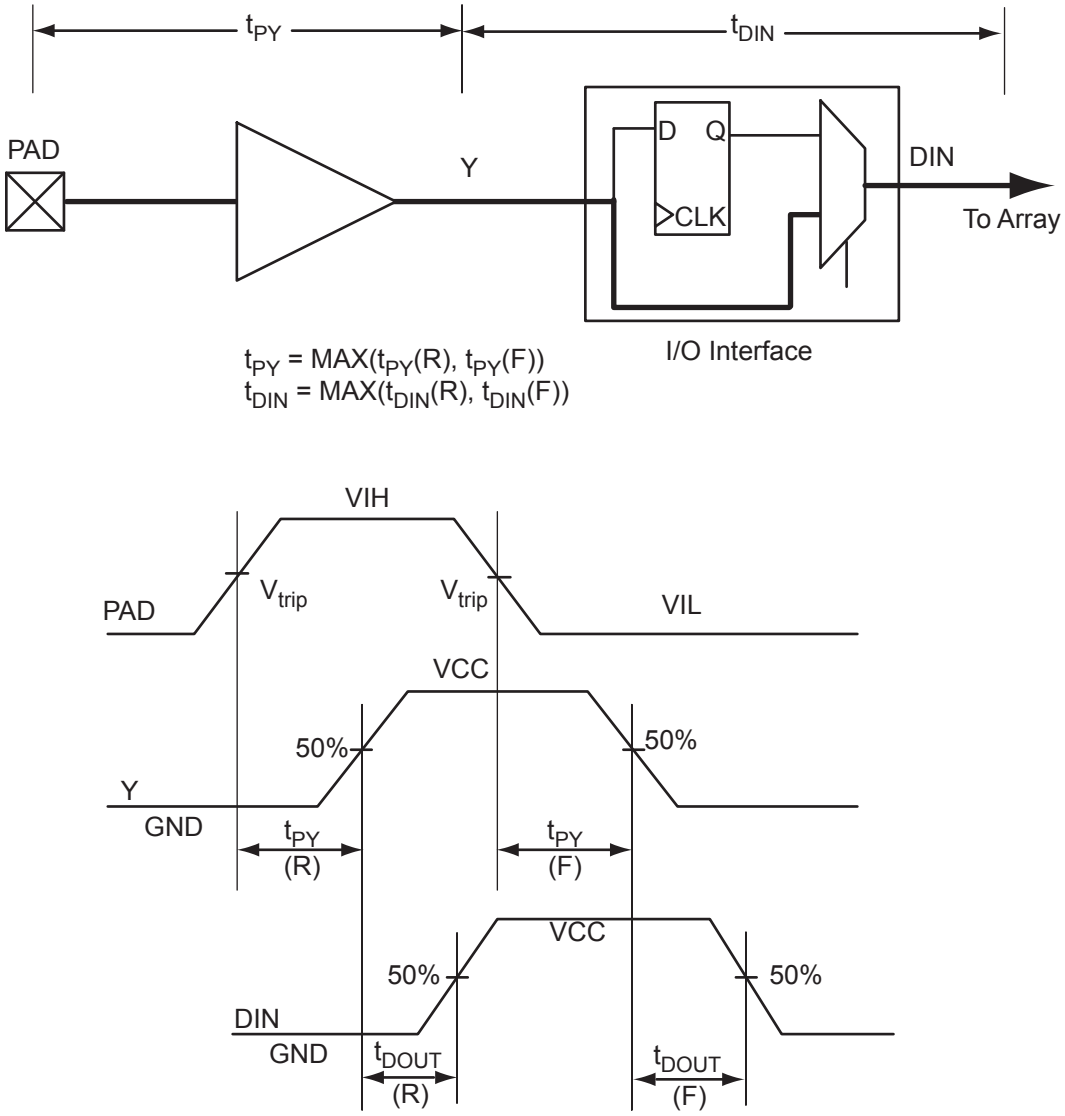


Figure 2-3 • **Input Buffer Timing Model and Delays (example)**

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-41 • **Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-42 • **Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

2.5 V LVCMOS	VIL		V_{IH}		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max., mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

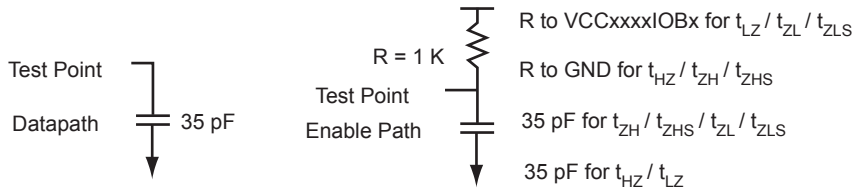


Figure 2-7 • **AC Loading**

Table 2-43 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-47 • **Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	16	16	74	91	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-48 • **Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

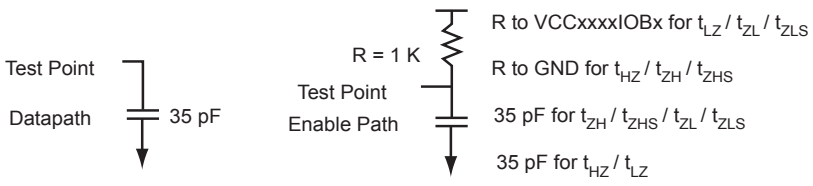


Figure 2-8 • **AC Loading**

Table 2-49 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-50 • **1.8 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.06	0.04	1.14	0.39	8.61	11.06	2.61	1.59	10.67	13.12	ns
	–1	0.50	9.22	0.03	0.95	0.32	7.17	9.22	2.18	1.33	8.89	10.93	ns
4 mA	Std.	0.60	6.46	0.04	1.14	0.39	5.53	6.46	3.04	2.66	7.59	8.51	ns
	–1	0.50	5.38	0.03	0.95	0.32	4.61	5.38	2.54	2.22	6.33	7.10	ns
6 mA	Std.	0.60	4.16	0.04	1.14	0.39	3.99	4.16	3.34	3.18	6.05	6.22	ns
	–1	0.50	3.47	0.03	0.95	0.32	3.32	3.47	2.78	2.65	5.04	5.18	ns
8 mA	Std.	0.60	3.69	0.04	1.14	0.39	3.76	3.67	3.40	3.31	5.81	5.73	ns
	–1	0.50	3.07	0.03	0.95	0.32	3.13	3.06	2.84	2.76	4.85	4.78	ns
12 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
16 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-51 • **1.8 V LVCMOS Low Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	14.24	0.04	1.14	0.39	13.47	14.24	2.62	1.54	15.53	16.30	ns
	–1	0.50	11.87	0.03	0.95	0.32	11.23	11.87	2.18	1.28	12.94	13.59	ns
4 mA	Std.	0.60	9.74	0.04	1.14	0.39	9.92	9.62	3.05	2.57	11.98	11.68	ns
	–1	0.50	8.11	0.03	0.95	0.32	8.26	8.02	2.54	2.14	9.98	9.74	ns
6 mA	Std.	0.60	7.67	0.04	1.14	0.39	7.81	7.24	3.34	3.08	9.87	9.30	ns
	–1	0.50	6.39	0.03	0.95	0.32	6.51	6.03	2.79	2.56	8.23	7.75	ns
8 mA	Std.	0.60	7.15	0.04	1.14	0.39	7.29	6.75	3.41	3.21	9.34	8.80	ns
	–1	0.50	5.96	0.03	0.95	0.32	6.07	5.62	2.84	2.68	7.79	7.34	ns
12 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns
16 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-11. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

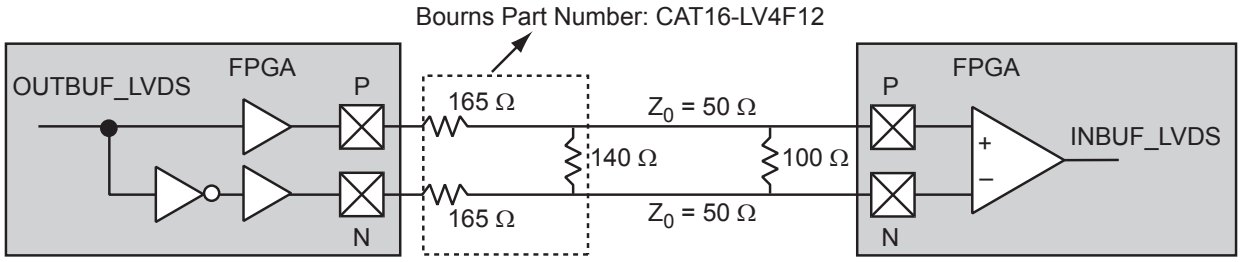


Figure 2-11 • **LVDS Circuit Diagram and Board-Level Implementation**

Output Enable Register

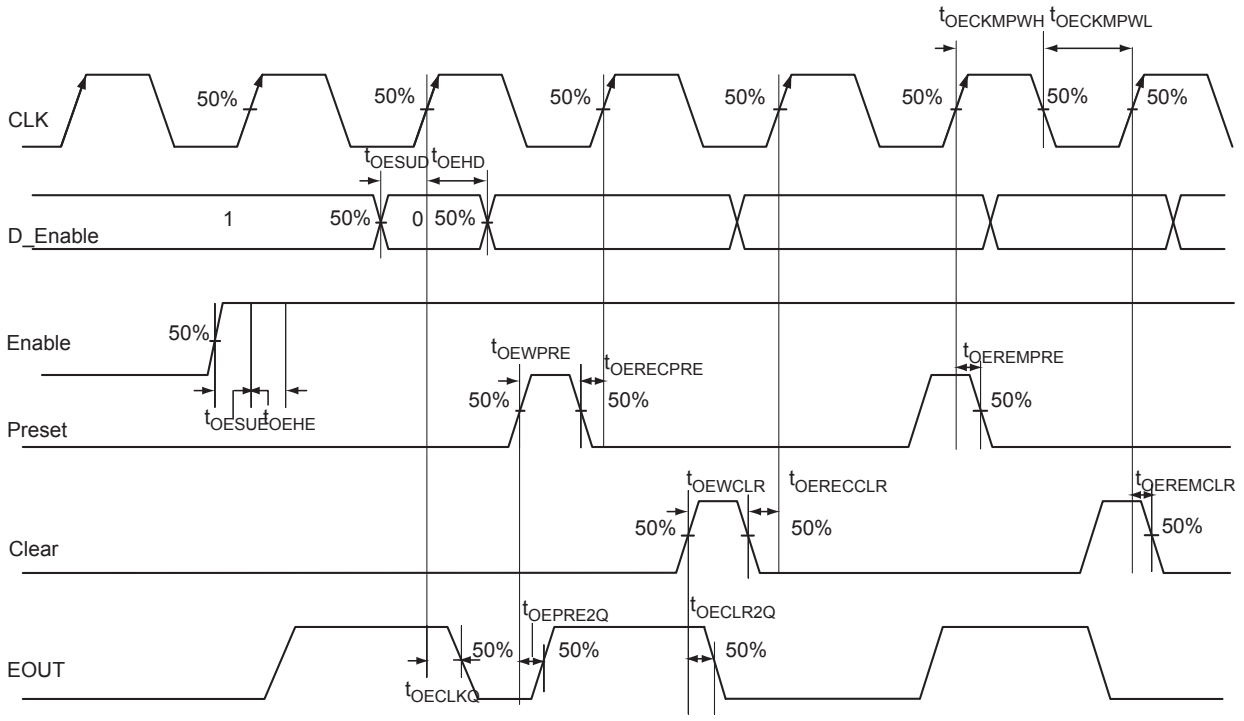


Figure 2-18 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-73 • **Output Enable Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.54	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.38	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.53	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Temperature Monitor

Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion cSoC and the sensing diode are at the same temperature.

Table 2-94 • **Temperature Monitor Performance Specifications**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input diode temperature range		–55		150	°C
		233.2		378.15	K
Temperature sensitivity			2.5		mV/K
Intercept	Extrapolated to 0K		0		V
Input referred temperature offset error	At 25°C (298.15K)		±1	1.5	°C
Gain error	Slope of BFSL vs. 2.5 mV/K		±1	2.5	% nom.
Overall accuracy	Peak error from ideal transfer function		±2	±3	°C
Input referred noise	At 25°C (298.15K) – no output averaging		4		°C rms
Output current	Idle mode		100		µA
	Final measurement phases		10		µA
Analog settling time	Measured to 0.1% of final value, (with ADC load)				
	From TM_STB (High)	5			µs
	From ADC_START (High)	5		105	µs
AT parasitic capacitance				500	pF
Power supply rejection ratio	DC (0–10 KHz)	1.2	0.7		°C/V
Input referred temperature sensitivity error	Variation due to device temperature (–40°C to +100°C). External temperature sensor held constant.		0.005	0.008	°C/°C
Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREFx)	VCC33A		200		µA
	VCC33AP		150		µA
	VCC15A		50		µA

Note: All results are based on averaging over 64 samples.

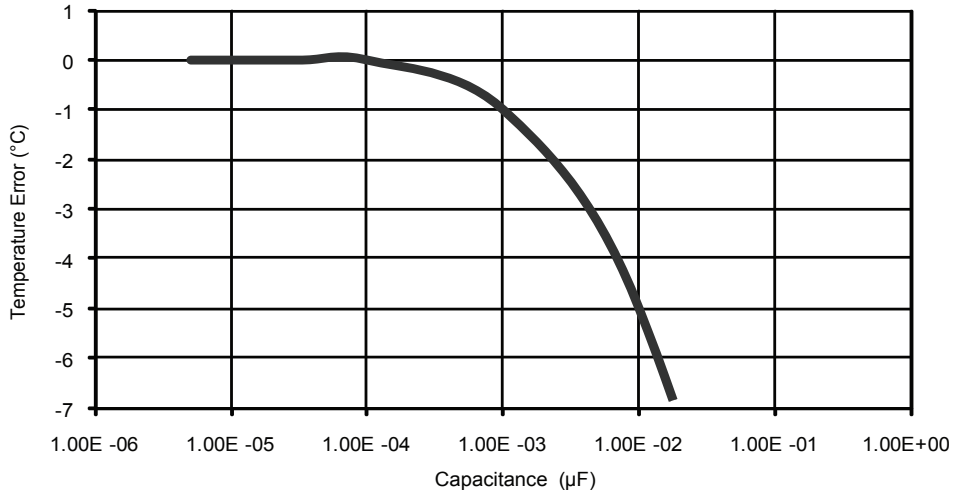


Figure 2-43 • **Temperature Error Versus External Capacitance**

Table 2-95 • **ADC Specifications (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-96 • **ABPS Performance Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

SmartFusion Ecosystem

The Microsemi SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in Figure 3-3.

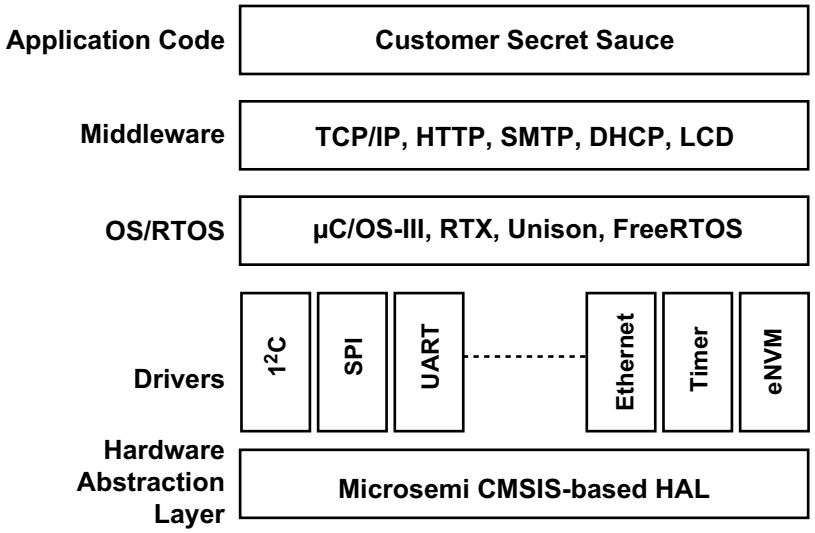


Figure 3-3 • **SmartFusion Ecosystem**

Figure 3-3 shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

ARM

Because an ARM processor was chosen for SmartFusion cSoCs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers* White Paper

Name	Type	Description
VCCFPGAIOB5	Supply	Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCLPXTAL	Supply	Analog supply to the low power 32 KHz crystal oscillator. Always power this pin.[1]
VCCMAINXTAL	Supply	Analog supply to the main crystal oscillator circuit. Always power this pin.[1]
VCCMSSIOB2	Supply	Supply voltage to the microcontroller subsystem I/O bank 2 (east MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCMSSIOB4	Supply	Supply voltage to the microcontroller subsystem I/O bank 4 (west MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCPLLx	Supply	Analog 1.5 V supply to the PLL. Always power this pin.
VCCRCOSC	Supply	Analog supply to the integrated RC oscillator circuit. Always power this pin.[1]
VCOMPLAx	Supply	Analog ground for the PLL
VDDBAT	Supply	External battery connection to the low power 32 KHz crystal oscillator (along with VCCLPXTAL), RTC, and battery switchover circuit. Can be pulled down if unused.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

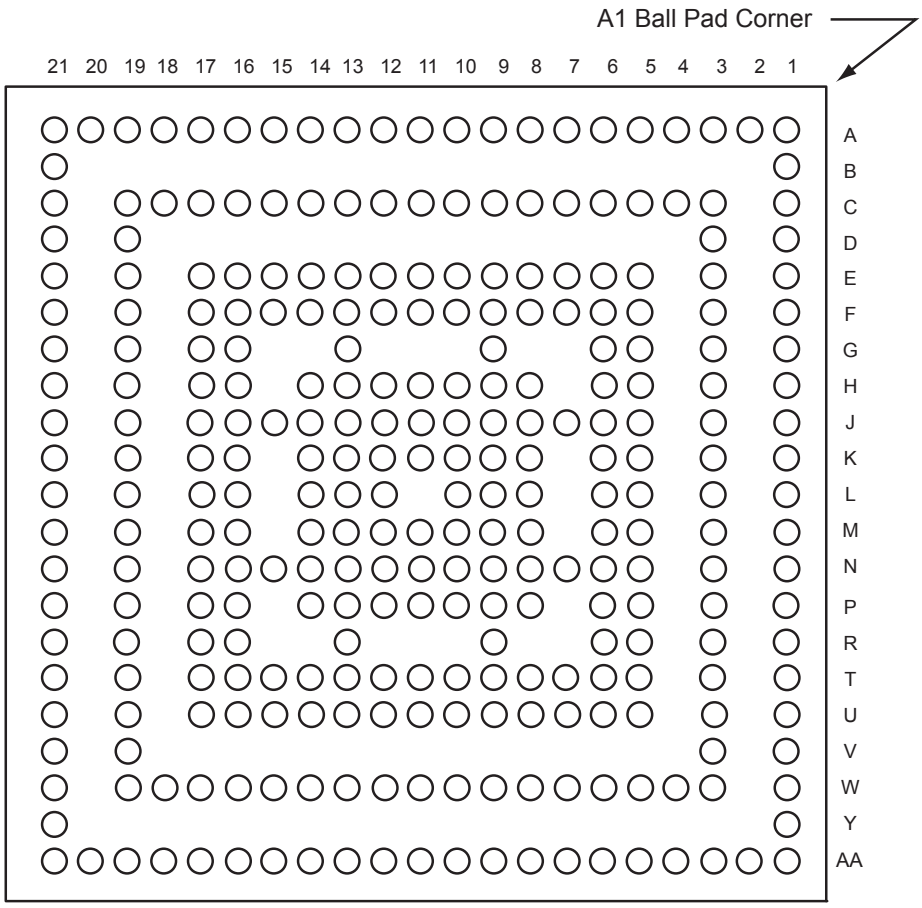
Table 5-2 • **Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

CS288



Note: Bottom view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
AA13	NC	ADC10
AA14	NC	ADC9
AA15	NC	GND15ADC2
AA16	MAINXIN	MAINXIN
AA17	MAINXOUT	MAINXOUT
AA18	LPXIN	LPXIN
AA19	LPXOUT	LPXOUT
AA20	NC	NC
AA21	NC	NC
AA22	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
AB1	GND	GND
AB2	GPIO_13/IO36RSB4V0	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO35RSB4V0	GPIO_14/IO44RSB4V0
AB4	GND	GND
AB5	PCAP	PCAP
AB6	NCAP	NCAP
AB7	ABPS3	ABPS3
AB8	ADC3	ADC3
AB9	GND15ADC0	GND15ADC0
AB10	VCC33ADC1	VCC33ADC1
AB11	VAREF1	VAREF1
AB12	TM2	TM2
AB13	CM2	CM2
AB14	ABPS4	ABPS4
AB15	GNDAQ	GNDAQ
AB16	GNDMAINXTAL	GNDMAINXTAL
AB17	GNDLPXTAL	GNDLPXTAL
AB18	VCCLPXTAL	VCCLPXTAL
AB19	VDDBAT	VDDBAT
AB20	PTBASE	PTBASE
AB21	NC	NC
AB22	GND	GND
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
U13	NC	GNDTM2
U14	NC	ADC11
U15	GNDVAREF	GNDVAREF
U16	VCC33SDD1	VCC33SDD1
U17	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
U18	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
U19	VCCMSSIOB2	VCCMSSIOB2
U20	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U21	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
U22	GND	GND
V1	GPIO_0/IO47RSB4V0	GPIO_0/IO56RSB4V0
V2	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
V3	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
V4	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
V5	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
V6	GND	GND
V7	SDD0	SDD0
V8	ABPS1	ABPS1
V9	ADC2	ADC2
V10	VCC33ADC0	VCC33ADC0
V11	ADC6	ADC6
V12	ADC5	ADC5
V13	ABPS5	ABPS5
V14	NC	ADC8
V15	NC	GND33ADC2
V16	NC	NC
V17	GND	GND
V18	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
V19	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
V20	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
V21	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
V22	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
W1	GPIO_2/IO45RSB4V0	GPIO_2/IO54RSB4V0
W2	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
	The A2F060 device was added to product information tables.	N/A
	The "Product Ordering Codes" table was updated to removed Std. speed and add speed grade 1. Pre-production was removed from the application ordering code category.	VI
	The "SmartFusion cSoC Block Diagram" was revised.	IV
	The "Datasheet Categories" section was updated, referencing the "SmartFusion cSoC Block Diagram" table, which is new.	1-4, IV
	The "VCCI" parameter was renamed to "VCCxxxxIOBx." "Advanced I/Os" were renamed to "FPGA I/Os." Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREFx designates VAREF0, VAREF1, and VAREF2. Modes were renamed as follows: Operating mode was renamed to SoC mode. 32KHz Active mode was renamed to Standby mode. Battery mode was renamed to Time Keeping mode. Table entries have been filled with values as data has become available.	N/A
	Table 2-1 • Absolute Maximum Ratings, Table 2-2 • Analog Maximum Ratings, and Table 2-3 • Recommended Operating Conditions[5,6] were revised extensively.	2-1 through 2-3
	Device names were updated in Table 2-6 • Package Thermal Resistance.	2-7
	Table 2-8 • Power Supplies Configuration was revised extensively.	2-10
	Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings was revised extensively.	2-11
	Removed "Example of Power Calculation."	N/A
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs was revised extensively.	2-12
	Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs was revised extensively.	2-13
	The "Power Calculation Methodology" section was revised.	2-14
	Table 2-83 • Electrical Characteristics of the RC Oscillator was revised extensively.	2-61
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator was revised extensively.	2-62
	The parameter t_{RSTBQ} was changed to T_{C2CWRH} in Table 2-87 • RAM4K9.	2-69
	The 12-bit mode row for integral non-linearity was removed from Table 2-95 • ADC Specifications. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear.	2-81
	Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted.	N/A
	Table 2-99 • Voltage Regulator was revised extensively.	2-87
	The "Serial Peripheral Interface (SPI) Characteristics" section and "Inter-Integrated Circuit (I^2C) Characteristics" section are new.	2-89, 2-91