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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1cs288i

Standby Mode

$P_{DYN} = P_{RC\text{-}OSC} + P_{LPXTAL\text{-}OSC}$

Time Keeping Mode

$P_{DYN} = P_{LPXTAL\text{-}OSC}$

Global Clock Dynamic Contribution—P_{CLOCK}

SoC Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Time Keeping Mode

$P_{CLOCK} = 0$ W

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

SoC Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{S\text{-}CELL} = 0$ W

Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

SoC Mode

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{C\text{-}CELL} = 0$ W

Routing Net Dynamic Contribution—P_{NET}

SoC Mode

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the frequency of the clock driving the logic including these nets.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

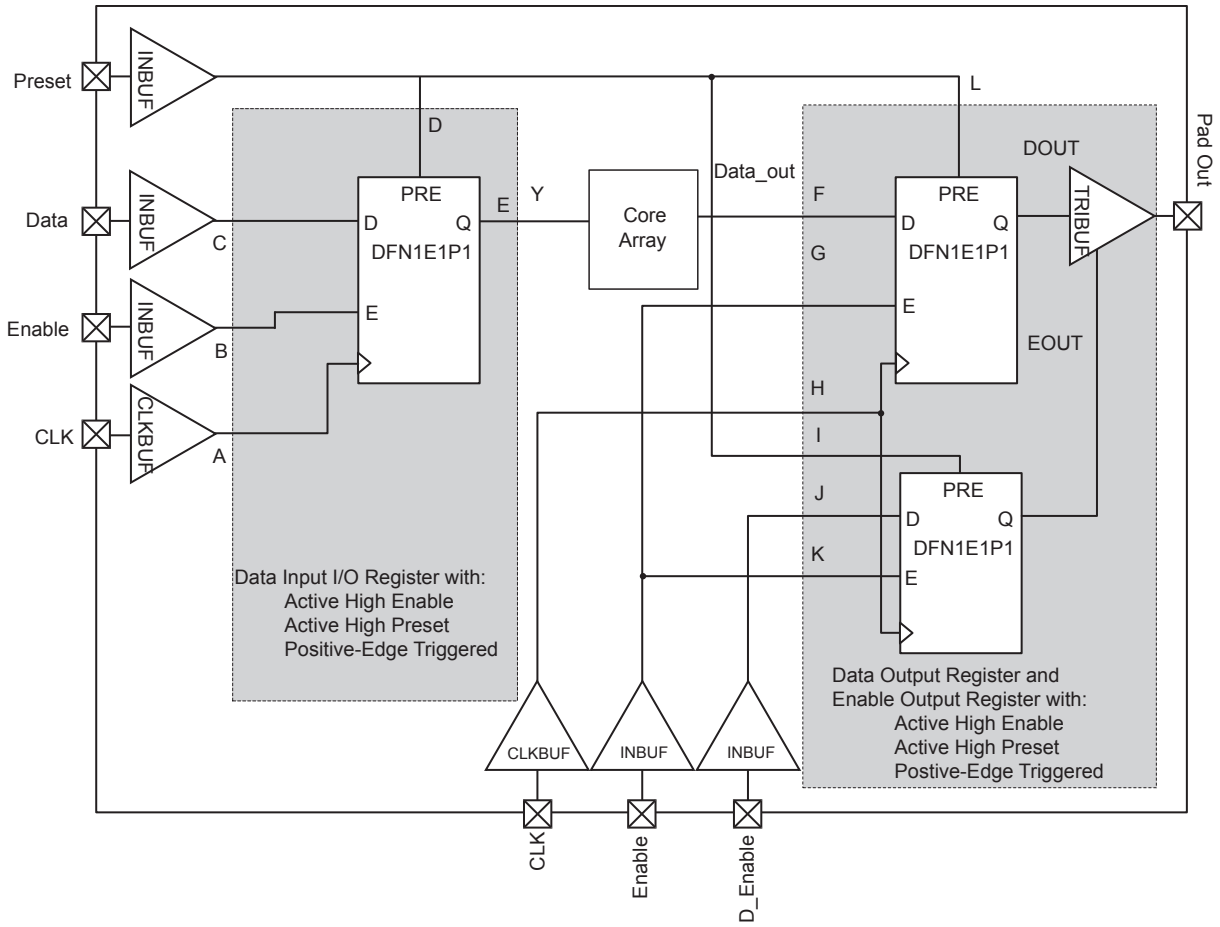

Figure 2-14 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

***Table 2-69* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-14 on page 2-44 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

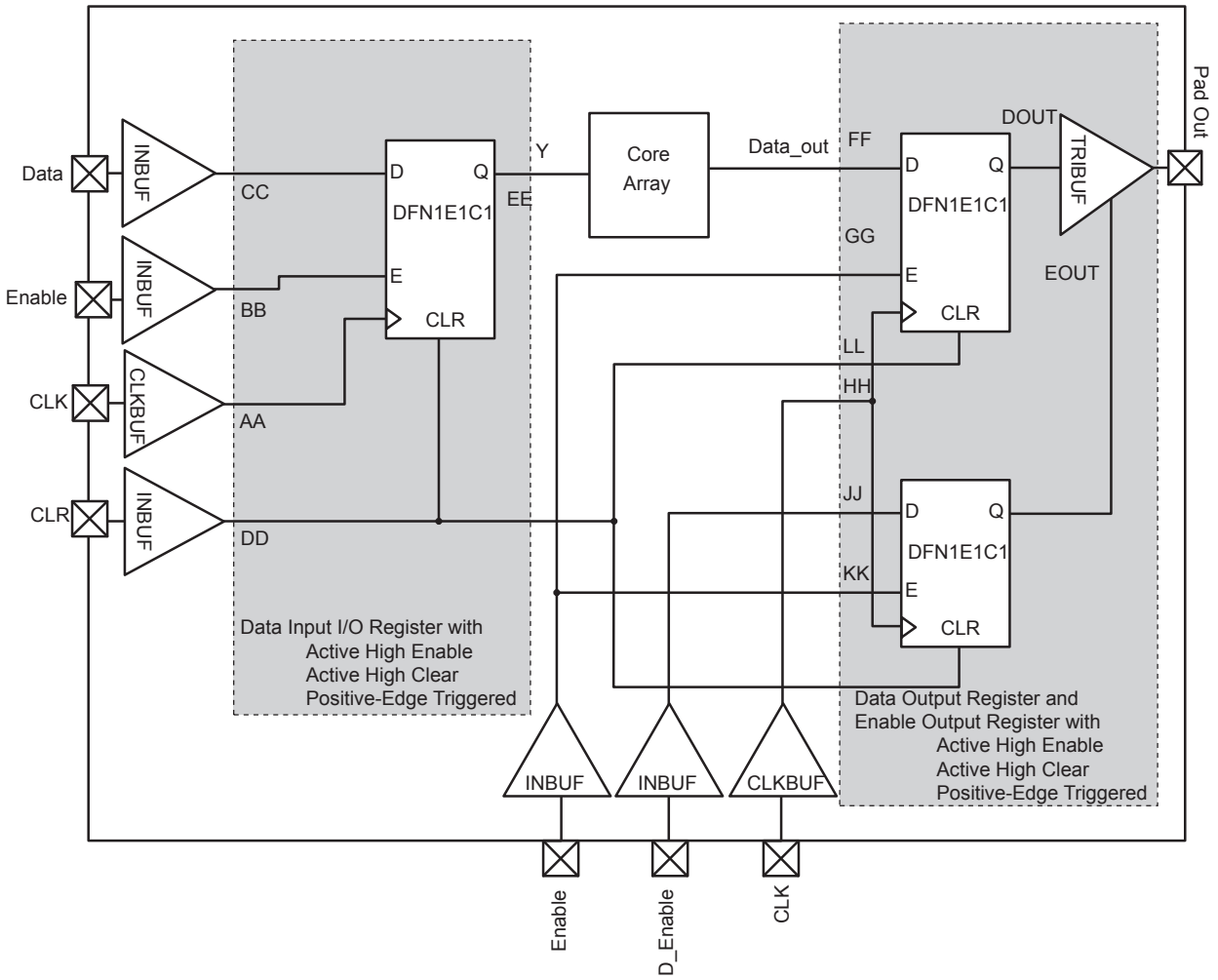

Figure 2-15 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Output Register

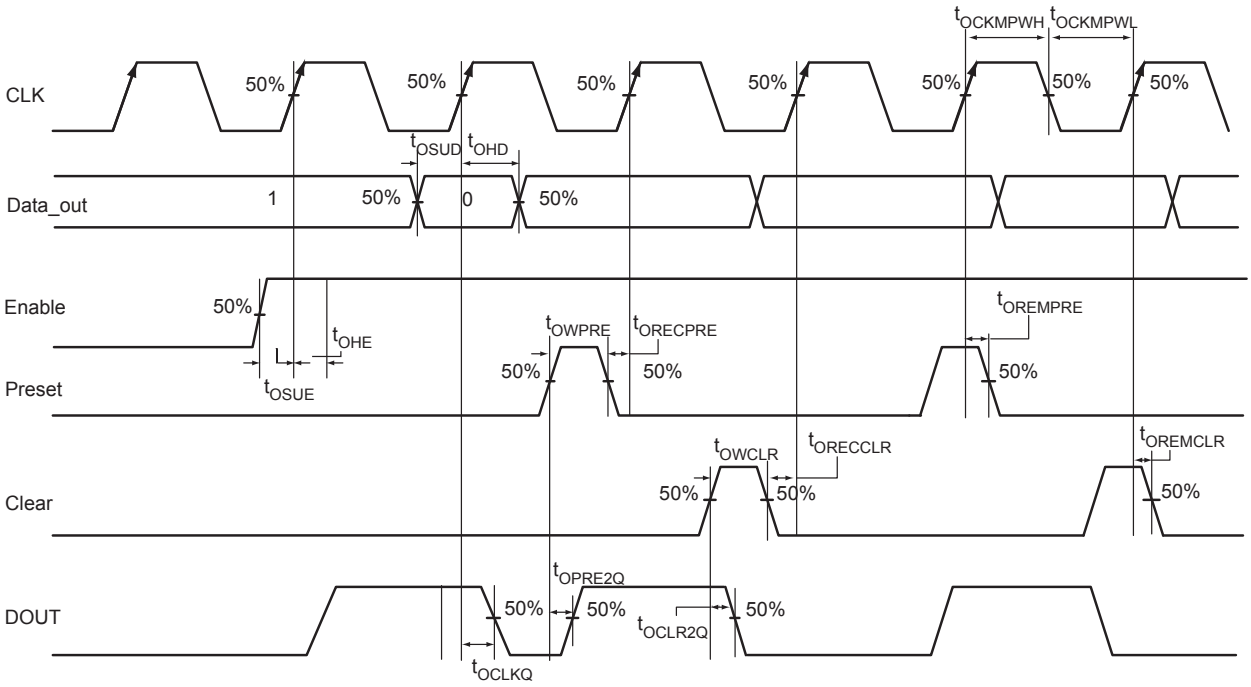

Figure 2-17 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-72 • **Output Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.72	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.38	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.98	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.98	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

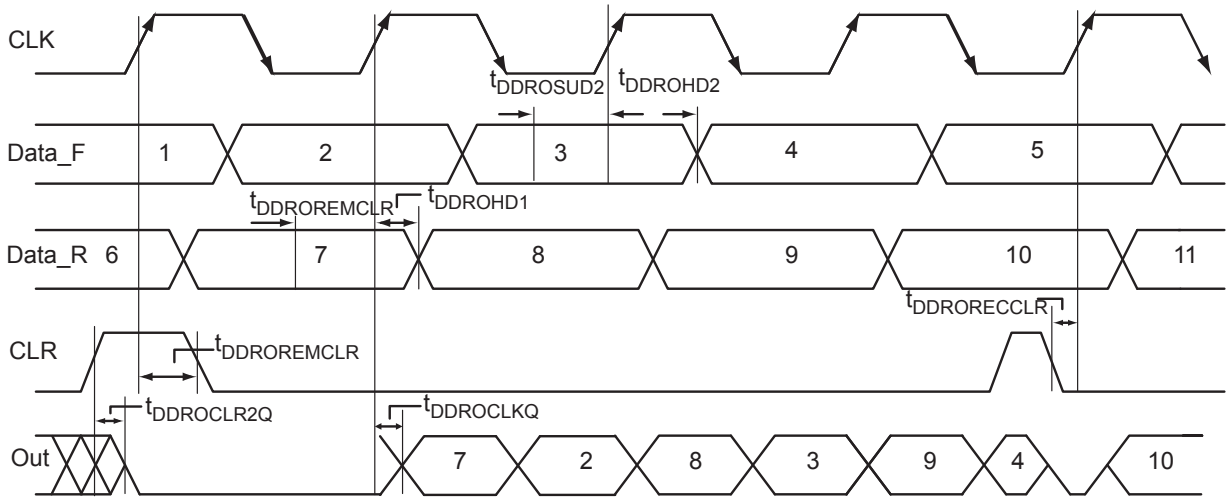

Figure 2-22 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-77 • **Output DDR Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.71	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.81	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-86* • SmartFusion CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350[1]	MHz
Delay Increments in Programmable Delay Blocks[2,3,4]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		5.15	%
Delay Range in Block: Programmable Delay 1[2,3]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[2,3]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[2,3]		2.2		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6,7]	Maximum Peak-to-Peak Period Jitter			

	SSO ≤ 2		SSO ≤ 4		SSO ≤ 8		SSO ≤ 16	
	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*

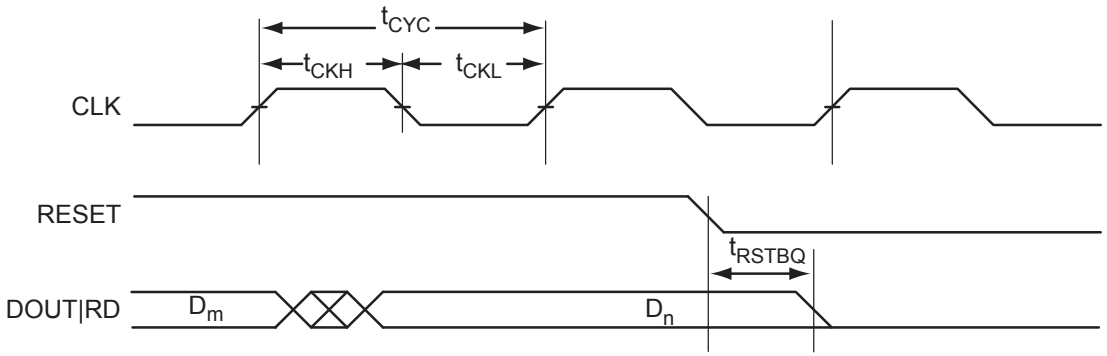

***Figure 2-34* • RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

Table 2-88 • RAM512X18
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.22	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.19	2.63	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.91	1.09	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.38	0.43	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.44	0.50	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to data out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.22	ns
t_{CYC}	Clock cycle time	3.28	3.28	ns
F_{MAX}	Maximum clock frequency	305	305	MHz

Notes:

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

The JTAGSEL pin selects the FPGA TAP controller or the Cortex-M3 debug logic. When JTAGSEL is asserted, the FPGA TAP controller is selected and the TRSTB input into the Cortex-M3 is held in a reset state (logic 0), as depicted in Figure 4-1. Users should tie the JTAGSEL pin high externally.

Microsemi's free Eclipse-based IDE, SoftConsole, has the ability to control the JTAGSEL pin directly with the FlashPro4 programmer. Manual jumpers are provided on the evaluation and development kits to allow manual selection of this function for the J-Link and ULINK debuggers.

Note: Standard ARM JTAG connectors do not have access to the JTAGSEL pin. SoftConsole automatically selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care."

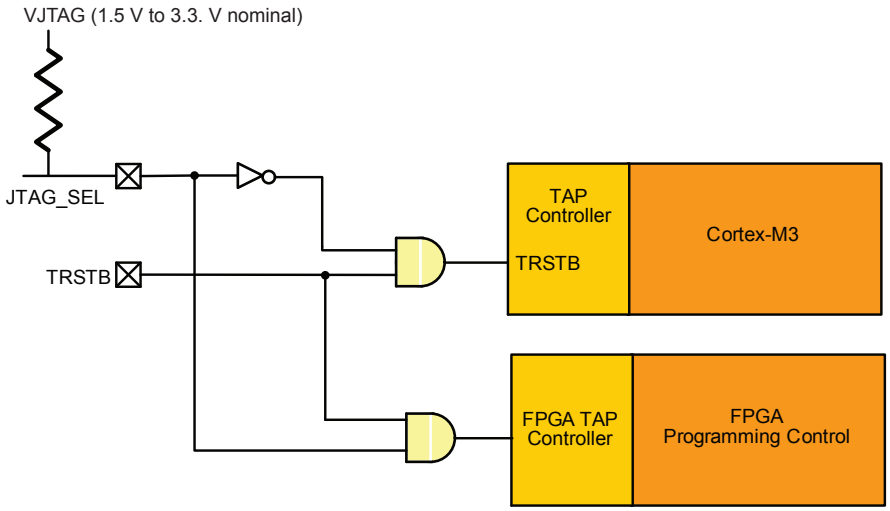

Figure 4-1 • **TRSTB Logic**

In-Application Programming

In-application programming refers to the ability to reprogram the various flash areas under direct supervision of the Cortex-M3.

Reprogramming the FPGA Fabric Using the Cortex-M3

In this mode, the Cortex-M3 is executing the programming algorithm on-chip. The IAP driver can be incorporated into the design project and executed from eNVM or eSRAM. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog. The new bitstream to be programmed into the FPGA can reside on the user's printed circuit board (PCB) in a separate SPI flash memory. Alternately, the user can modify the existing projects supplied by the SoC Products Group and, via custom handshaking software, throttle the download of the new image and program the FPGA a piece at a time in real time. A cost-effective and reliable approach would be to store the bitstream in an external SPI flash. Another option is storing a redundant bitstream image in an external SPI flash and loading the newest version into the FPGA only when receiving an IAP command. Since the FPGA I/Os are tristated or held at predefined or last known state during FPGA programming, the user must use MSS I/Os to interface to external memories. Since there are two SPI controllers in the MSS, the user can dedicate one to an SPI flash and the other to the particulars of an application. The amount of flash memory required to program the FPGA always exceeds the size of the eNVM block that is on-chip. The external memory controller (EMC) cannot be used as an interface to a memory device for storage of a bitstream because its I/O pads are FPGA I/Os; hence they are tristated when the FPGA is in a programming state.

The MSS resets itself after IAP of the FPGA fabric. This reset is internally asserted on MSS_RESETN by the power supply monitor (PSM) and reset controller of the MSS.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

TQ144	
Pin Number	**A2F060 Function**
73	VCC33A
74	PTEM
75	PTBASE
76	SPI_0_DO/GPIO_16
77	SPI_0_DI/GPIO_17
78	SPI_0_CLK/GPIO_18
79	SPI_0_SS/GPIO_19
80	UART_0_RXD/GPIO_21
81	UART_0_TXD/GPIO_20
82	UART_1_RXD/GPIO_29
83	UART_1_TXD/GPIO_28
84	VCC
85	VCCMSSIOB2
86	GND
87	I2C_1_SDA/GPIO_30
88	I2C_1_SCL/GPIO_31
89	I2C_0_SDA/GPIO_22
90	I2C_0_SCL/GPIO_23
91	GNDENVM
92	VCCENVM
93	JTAGSEL
94	TCK
95	TDI
96	TMS
97	TDO
98	TRSTB
99	VJTAG
100	VDDBAT
101	VCCLPXTAL
102	LPXOUT
103	LPXIN
104	GNDLPXTAL
105	GNDMAINXTAL
106	MAINXOUT
107	MAINXIN
108	VCCMAINXTAL

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
H19	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
H21	NC	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J3	EMC_DB[8]/IO40NPB5V0	EMC_DB[8]/GEC0/IO63NPB5V0	EMC_DB[8]/GEC0/IO80NPB5V0
J5	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
J6	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
J8	VCC	VCC	VCC
J9	GND	GND	GND
J10	VCC	VCC	VCC
J11	GND	GND	GND
J12	VCC	VCC	VCC
J13	GND	GND	GND
J14	VCC	VCC	VCC
J15	VPP	VPP	VPP
J16	NC	IO32NPB1V0	IO41NPB1V0
J17	NC	GNDQ	GNDQ
J19	VCCMAINXTAL	VCCMAINXTAL	VCCMAINXTAL
J21	NC	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
K1	GND	GND	GND
K3	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
K5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K6	EMC_DB[3]/IO37PPB5V0	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
K8	GND	GND	GND
K9	VCC	VCC	VCC
K10	GND	GND	GND
K11	VCC	VCC	VCC
K12	GND	GND	GND
K13	VCC	VCC	VCC
K14	GND	GND	GND
K16	LPXOUT	LPXOUT	LPXOUT

Notes:

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2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

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Pin Number	PQ208	
	A2F200	A2F500
32	VCCRCOSC	VCCRCOSC
33	MSS_RESET_N	MSS_RESET_N
34	VCCESRAM	VCCESRAM
35	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
36	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
37	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
38	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
39	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
40	GND	GND
41	VCCMSSIOB4	VCCMSSIOB4
42	VCC	VCC
43	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
44	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
45	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
46	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
47	MAC_CLK	MAC_CLK
48	GNDSDD0	GNDSDD0
49	VCC33SDD0	VCC33SDD0
50	VCC15A	VCC15A
51	PCAP	PCAP
52	NCAP	NCAP
53	VCC33AP	VCC33AP
54	VCC33N	VCC33N
55	SDD0	SDD0
56	GNDA	GNDA
57	GNDAQ	GNDAQ
58	ABPS0	ABPS0
59	ABPS1	ABPS1
60	CM0	CM0
61	TM0	TM0
62	GNDTM0	GNDTM0

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Pin Number	PQ208	
	A2F200	A2F500
125	TMS	TMS
126	TDO	TDO
127	TRSTB	TRSTB
128	VJTAG	VJTAG
129	VDDBAT	VDDBAT
130	VCCLPXTAL	VCCLPXTAL
131	LPXOUT	LPXOUT
132	LPXIN	LPXIN
133	GNDLPXTAL	GNDLPXTAL
134	GNDMAINXTAL	GNDMAINXTAL
135	MAINXOUT	MAINXOUT
136	MAINXIN	MAINXIN
137	VCCMAINXTAL	VCCMAINXTAL
138	GND	GND
139	VCC	VCC
140	VPP	VPP
141	VCCFPGAIOB1	VCCFPGAIOB1
142	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
143	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
144	GDC0/IO29NSB1V0	GDC0/IO38NSB1V0
145	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
146	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
147	VCCFPGAIOB1	VCCFPGAIOB1
148	GND	GND
149	VCC	VCC
150	IO25NDB1V0	IO30NDB1V0
151	GCC2/IO25PDB1V0	GBC2/IO30PDB1V0
152	IO23NDB1V0	IO28NDB1V0
153	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
154	GBC2/IO21PSB1V0	GBB2/IO27NDB1V0
155	GBA2/IO20PSB1V0	GBA2/IO27PDB1V0

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Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
T9	VAREF0	VAREF1	VAREF1
T10	ABPS0	ABPS6	ABPS6
T11	NC	ABPS5	ABPS5
T12	NC	SDD1	SDD1
T13	GNDVAREF	GNDVAREF	GNDVAREF
T14	GNDMAINXTAL	GNDMAINXTAL	GNDMAINXTAL
T15	VCCLPXTAL	VCCLPXTAL	VCCLPXTAL
T16	PU_N	PU_N	PU_N

Notes:

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Pin Number	FG484	
	A2F200 Function	A2F500 Function
AA13	NC	ADC10
AA14	NC	ADC9
AA15	NC	GND15ADC2
AA16	MAINXIN	MAINXIN
AA17	MAINXOUT	MAINXOUT
AA18	LPXIN	LPXIN
AA19	LPXOUT	LPXOUT
AA20	NC	NC
AA21	NC	NC
AA22	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
AB1	GND	GND
AB2	GPIO_13/IO36RSB4V0	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO35RSB4V0	GPIO_14/IO44RSB4V0
AB4	GND	GND
AB5	PCAP	PCAP
AB6	NCAP	NCAP
AB7	ABPS3	ABPS3
AB8	ADC3	ADC3
AB9	GND15ADC0	GND15ADC0
AB10	VCC33ADC1	VCC33ADC1
AB11	VAREF1	VAREF1
AB12	TM2	TM2
AB13	CM2	CM2
AB14	ABPS4	ABPS4
AB15	GNDAQ	GNDAQ
AB16	GNDMAINXTAL	GNDMAINXTAL
AB17	GNDLPXTAL	GNDLPXTAL
AB18	VCCLPXTAL	VCCLPXTAL
AB19	VDDBAT	VDDBAT
AB20	PTBASE	PTBASE
AB21	NC	NC
AB22	GND	GND
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND

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Pin Number	FG484	
	A2F200 Function	A2F500 Function
T1	GND	GND
T2	VCCMSSIOB4	VCCMSSIOB4
T3	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO57RSB4V0	GPIO_11/IO66RSB4V0
T5	GND	GND
T6	MAC_CLK	MAC_CLK
T7	VCCMSSIOB4	VCCMSSIOB4
T8	VCC33SDD0	VCC33SDD0
T9	VCC15A	VCC15A
T10	GNDAQ	GNDAQ
T11	GND33ADC0	GND33ADC0
T12	ADC7	ADC7
T13	NC	TM4
T14	NC	VAREF2
T15	VAREFOUT	VAREFOUT
T16	VCCMSSIOB2	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
T18	GND	GND
T19	NC	NC
T20	NC	NC
T21	VCCMSSIOB2	VCCMSSIOB2
T22	GND	GND
U1	GND	GND
U2	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO58RSB4V0	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4	VCCMSSIOB4
U5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
U6	NC	NC
U7	VCC33AP	VCC33AP
U8	VCC33N	VCC33N
U9	CM1	CM1
U10	VAREF0	VAREF0
U11	GND33ADC1	GND33ADC1
U12	ADC4	ADC4

Notes:

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