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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1csg288

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Standby Mode

$P_{DYN} = P_{RC\text{-}OSC} + P_{LPXTAL\text{-}OSC}$

Time Keeping Mode

$P_{DYN} = P_{LPXTAL\text{-}OSC}$

Global Clock Dynamic Contribution—P_{CLOCK}

SoC Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Time Keeping Mode

$P_{CLOCK} = 0 W$

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

SoC Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{S\text{-}CELL} = 0 W$

Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

SoC Mode

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{C\text{-}CELL} = 0 W$

Routing Net Dynamic Contribution—P_{NET}

SoC Mode

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the frequency of the clock driving the logic including these nets.

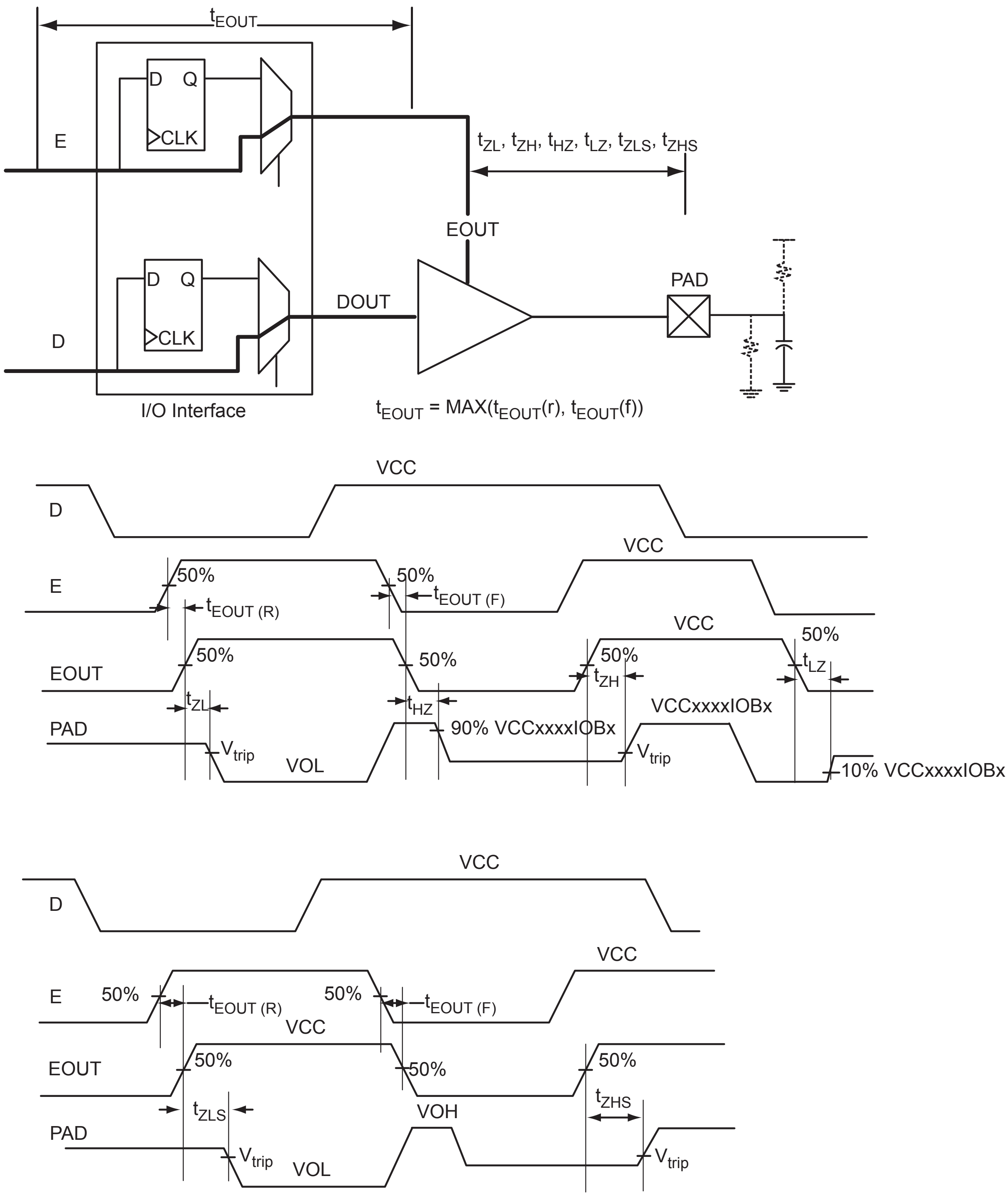

Figure 2-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Timing Characteristics

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	7.20	0.04	0.97	0.39	7.34	6.18	2.52	2.46	9.39	8.23	ns
	–1	0.50	6.00	0.03	0.81	0.32	6.11	5.15	2.10	2.05	7.83	6.86	ns
8 mA	Std.	0.60	4.64	0.04	0.97	0.39	4.73	3.84	2.85	3.02	6.79	5.90	ns
	–1	0.50	3.87	0.03	0.81	0.32	3.94	3.20	2.37	2.52	5.65	4.91	ns
12 mA	Std.	0.60	3.37	0.04	0.97	0.39	3.43	2.67	3.07	3.39	5.49	4.73	ns
	–1	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
16 mA	Std.	0.60	3.18	0.04	0.97	0.39	3.24	2.43	3.11	3.48	5.30	4.49	ns
	–1	0.50	2.65	0.03	0.81	0.32	2.70	2.03	2.59	2.90	4.42	3.74	ns
24 mA	Std.	0.60	2.93	0.04	0.97	0.39	2.99	2.03	3.17	3.83	5.05	4.09	ns
	–1	0.50	2.45	0.03	0.81	0.32	2.49	1.69	2.64	3.19	4.21	3.41	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	9.75	0.04	0.97	0.39	9.93	8.22	2.52	2.31	11.99	10.28	ns
	–1	0.50	8.12	0.03	0.81	0.32	8.27	6.85	2.10	1.93	9.99	8.57	ns
8 mA	Std.	0.60	6.96	0.04	0.97	0.39	7.09	5.85	2.84	2.87	9.15	7.91	ns
	–1	0.50	5.80	0.03	0.81	0.32	5.91	4.88	2.37	2.39	7.62	6.59	ns
12 mA	Std.	0.60	5.35	0.04	0.97	0.39	5.45	4.58	3.06	3.23	7.51	6.64	ns
	–1	0.50	4.46	0.03	0.81	0.32	4.54	3.82	2.55	2.69	6.26	5.53	ns
16 mA	Std.	0.60	5.01	0.04	0.97	0.39	5.10	4.30	3.11	3.32	7.16	6.36	ns
	–1	0.50	4.17	0.03	0.81	0.32	4.25	3.58	2.59	2.77	5.97	5.30	ns
24 mA	Std.	0.60	4.67	0.04	0.97	0.39	4.75	4.28	3.16	3.66	6.81	6.34	ns
	–1	0.50	3.89	0.03	0.81	0.32	3.96	3.57	2.64	3.05	5.68	5.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-40 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.31	0.09	0.94	1.30	0.22	2.35	1.86	2.20	2.45	ns
	–1	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Timing Characteristics

Table 2-56 • 1.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx = 1.425 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 m	Std.	0.60	7.79	0.04	1.34	0.39	6.43	7.79	3.19	2.59	8.49	9.85	ns
	–1	0.50	6.49	0.03	1.12	0.32	5.36	6.49	2.66	2.16	7.08	8.21	ns
4 mA	Std.	0.60	4.95	0.04	1.34	0.39	4.61	4.96	3.53	3.19	6.67	7.02	ns
	–1	0.50	4.13	0.03	1.12	0.32	3.85	4.13	2.94	2.66	5.56	5.85	ns
6 mA	Std.	0.60	4.36	0.04	1.34	0.39	4.34	4.36	3.60	3.34	6.40	6.42	ns
	–1	0.50	3.64	0.03	1.12	0.32	3.62	3.64	3.00	2.78	5.33	5.35	ns
8 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
12 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-57 • 1.5 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.96	0.04	1.34	0.39	12.18	11.70	3.20	2.47	14.24	13.76	ns
	–1	0.50	9.96	0.03	1.12	0.32	10.15	9.75	2.67	2.06	11.86	11.46	ns
4 mA	Std.	0.60	9.51	0.04	1.34	0.39	9.68	8.76	3.54	3.07	11.74	10.82	ns
	–1	0.50	7.92	0.03	1.12	0.32	8.07	7.30	2.95	2.56	9.79	9.02	ns
6 mA	Std.	0.60	8.86	0.04	1.34	0.39	9.03	8.17	3.61	3.22	11.08	10.23	ns
	–1	0.50	7.39	0.03	1.12	0.32	7.52	6.81	3.01	2.68	9.24	8.52	ns
8 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns
12 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-58 • 1.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.22	3.24	0.09	1.28	1.86	0.22	3.30	3.20	2.24	2.21	ns
	–1	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Output Enable Register

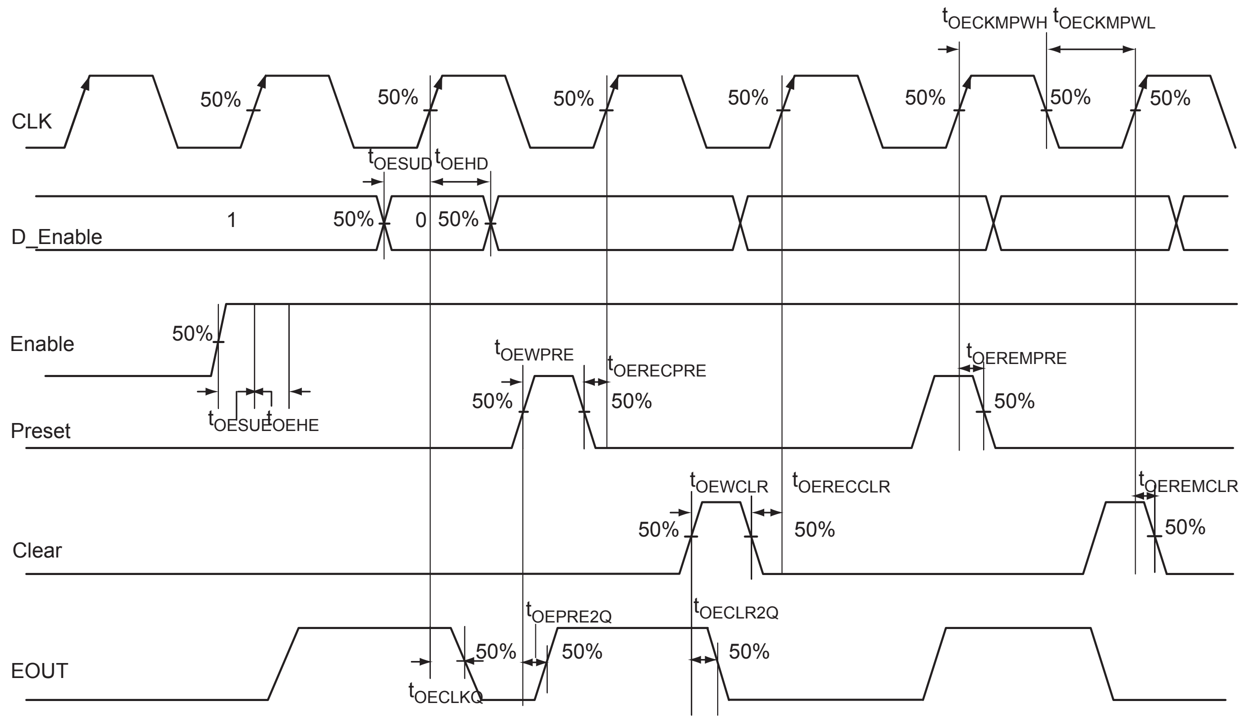

Figure 2-18 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-73 • Output Enable Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.54	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.38	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.53	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

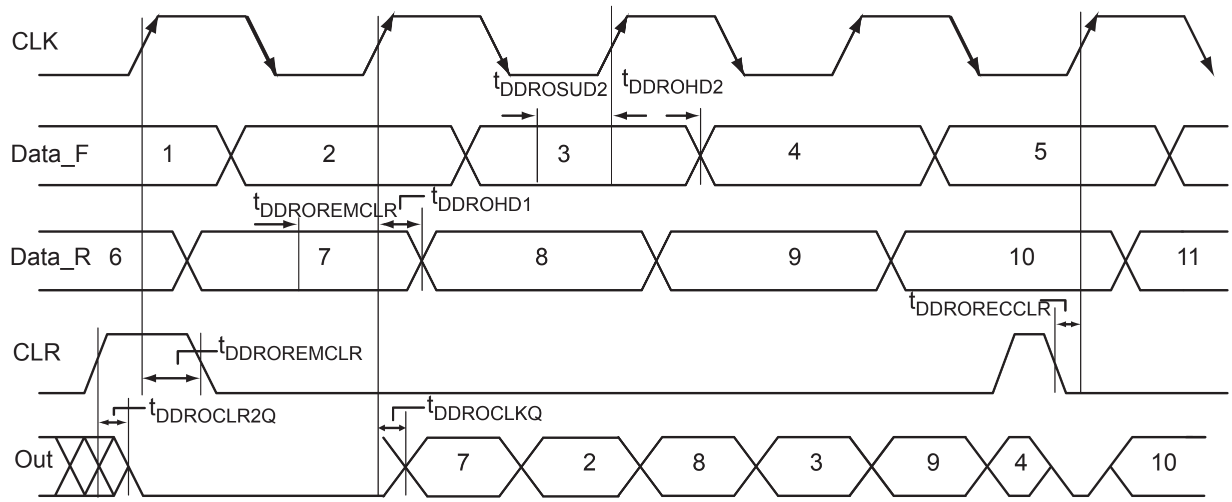

***Figure 2-22* • Output DDR Timing Diagram**

Timing Characteristics

***Table 2-77* • Output DDR Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.71	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.81	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

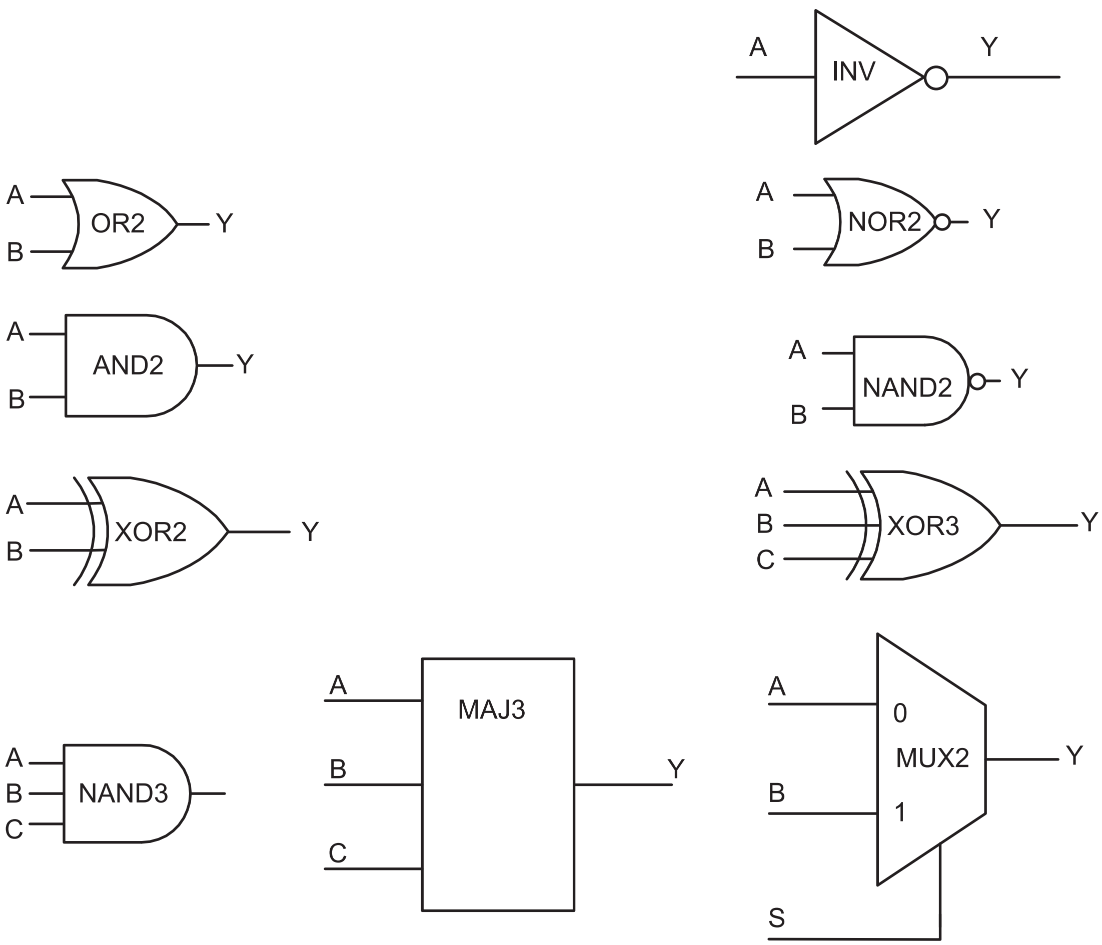

Figure 2-23 **• Sample of Combinatorial Cells**

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-86* • SmartFusion CCC/PLL Specification**

Parameter	Minimum		Typical		Maximum		Units	
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5				350		MHz	
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75				350[1]		MHz	
Delay Increments in Programmable Delay Blocks[2,3,4]			160				ps	
Number of Programmable Values in Each Programmable Delay Block					32			
Input Period Jitter					1.5		ns	
Acquisition Time								
LockControl = 0					300		µs	
LockControl = 1					6.0		ms	
Tracking Jitter[5]								
LockControl = 0					1.6		ns	
LockControl = 1					0.8		ns	
Output Duty Cycle	48.5				5.15		%	
Delay Range in Block: Programmable Delay 1[2,3]	0.6				5.56		ns	
Delay Range in Block: Programmable Delay 2[2,3]	0.025				5.56		ns	
Delay Range in Block: Fixed Delay[2,3]			2.2				ns	
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6,7]	Maximum Peak-to-Peak Period Jitter							
	SSO ≤ 2		SSO ≤ 4		SSO ≤ 8		SSO ≤ 16	
	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*

Timing Waveforms

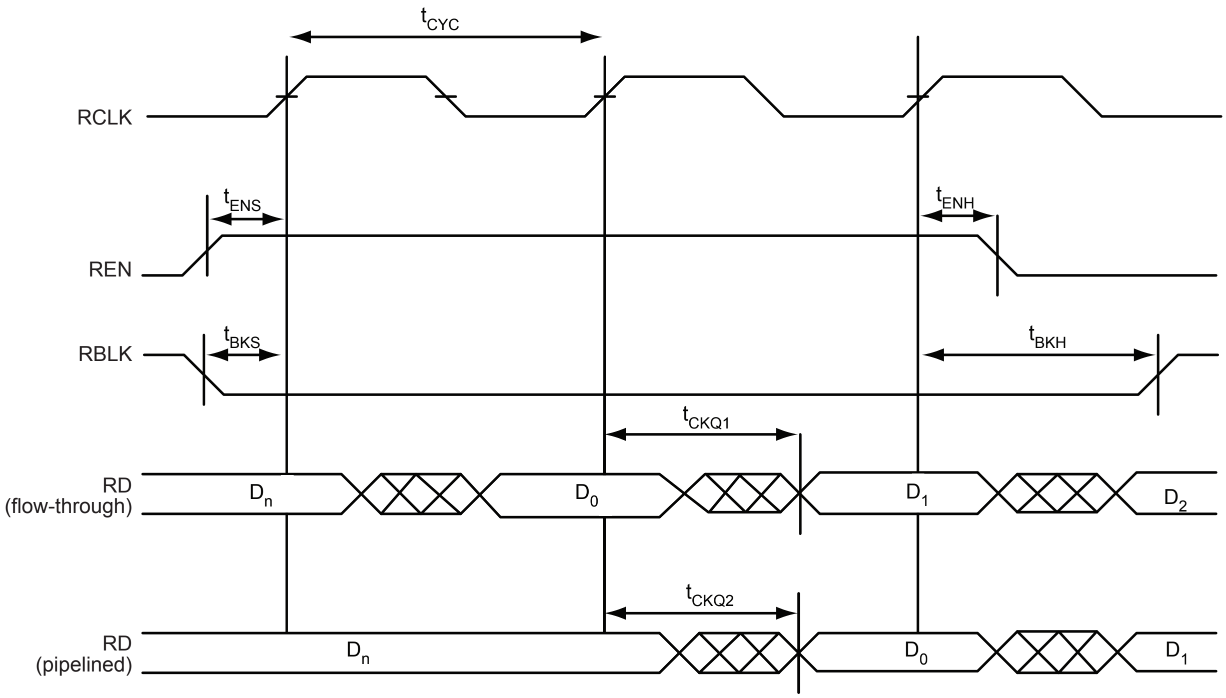

Figure 2-36 • **FIFO Read**

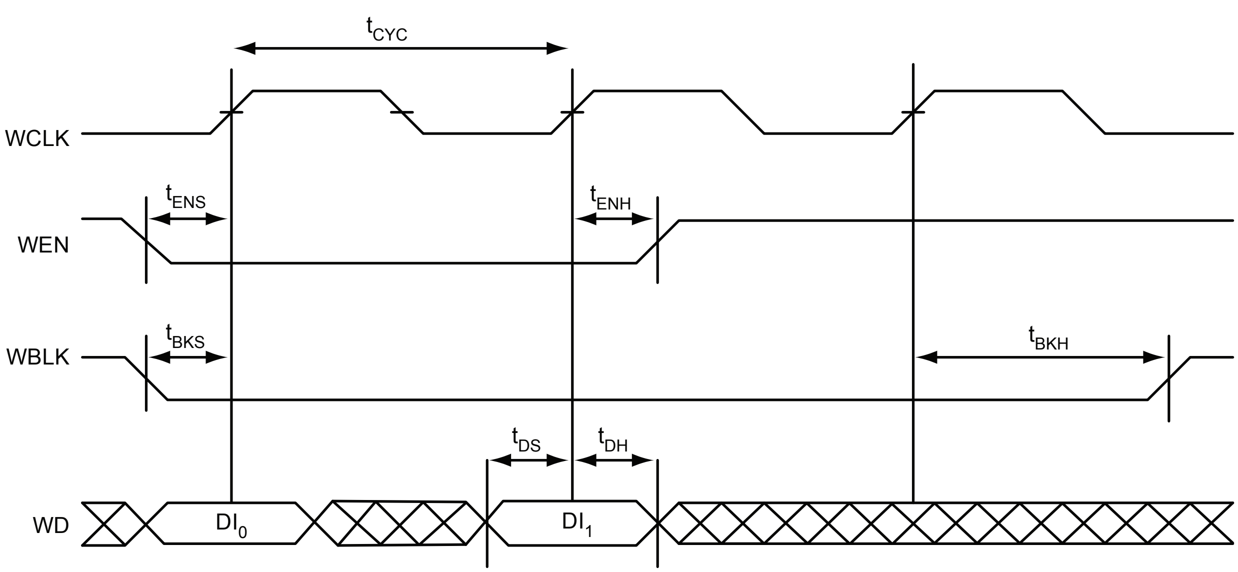

Figure 2-37 • **FIFO Write**

Programmable Analog Specifications

Current Monitor

Unless otherwise noted, current monitor performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

***Table 2-93* • Current Monitor Performance Specification**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input voltage range (for driving ADC over full range)		0 – 48	0 – 50	1 – 51	mV
Analog gain	From the differential voltage across the input pads to the ADC input		50		V/V
Input referred offset voltage	Input referred offset voltage	0	0.1	0.5	mV
	–40ºC to +100ºC	0	0.1	0.5	mV
Gain error	Slope of BFSL vs. 50 V/V		±0.1	±0.5	% nom.
	–40ºC to +100ºC			±0.5	% nom.
Overall Accuracy	Peak error from ideal transfer function, 25°C		±(0.1 + 0.25%)	±(0.4 + 1.5%)	mV plus % reading
Input referred noise	0 VDC input (no output averaging)	0.3	0.4	0.5	mVrms
Common-mode rejection ratio	0 V to 12 VDC common-mode voltage	–86	–87		dB
Analog settling time	To 0.1% of final value (with ADC load)				
	From CM_STB (High)	5			µs
	From ADC_START (High)	5		200	µs
Input capacitance			8		pF
Input biased current	CM[n] or TM[n] pad, –40°C to +100°C over maximum input voltage range (plus is into pad)				
	Strobe = 0; IBIAS on CM[n]		0		µA
	Strobe = 1; IBIAS on CM[n]		1		µA
	Strobe = 0; IBIAS on TM[n]		2		µA
	Strobe = 1; IBIAS on TM[n]		1		µA
Power supply rejection ratio	DC (0 – 10 KHz)	41	42		dB
Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREFx)	VCC33A		150		µA
	VCC33AP		140		µA
	VCC15A		50		µA

Note: Under no condition should the TM pad ever be greater than 10 mV above the CM pad. This restriction is applicable only if current monitor is used.

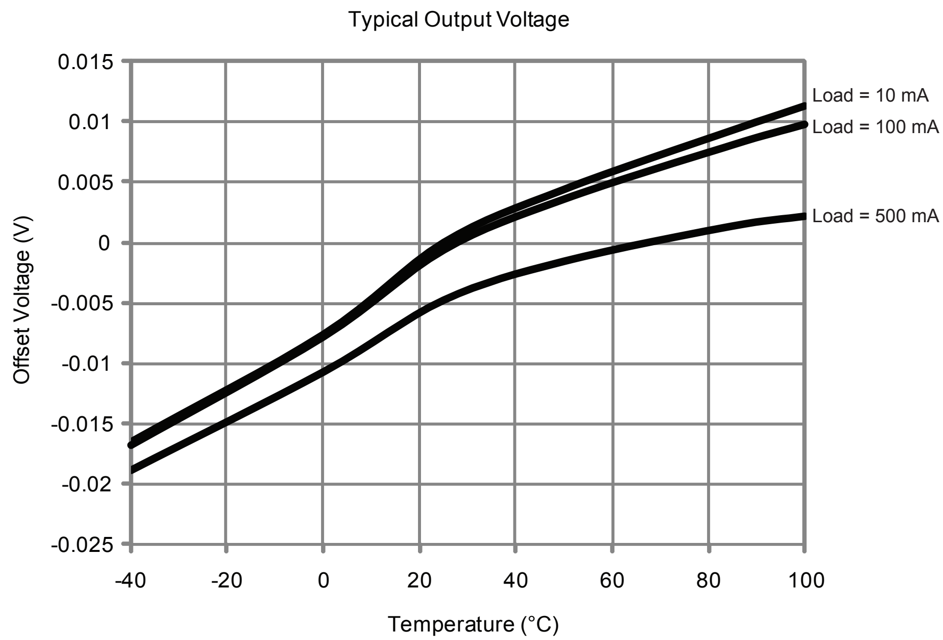

Figure 2-45 **• Typical Output Voltage**

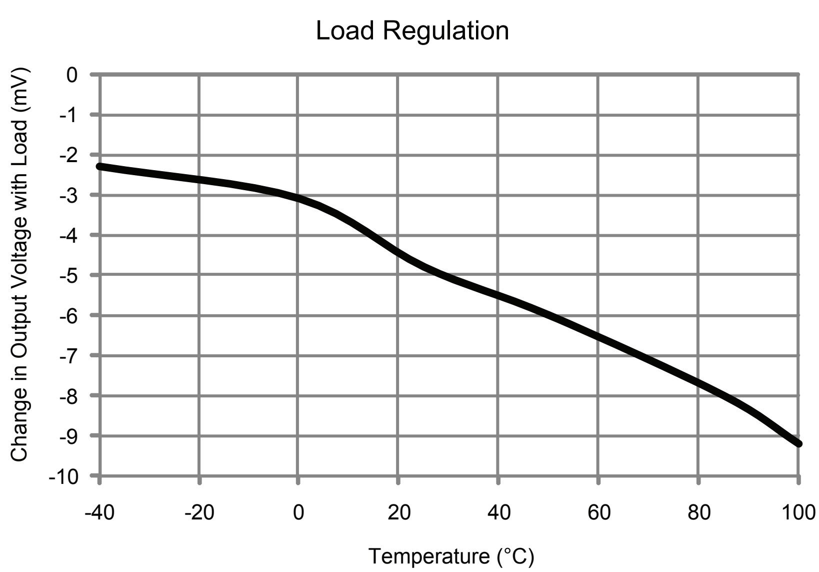

Figure 2-46 **• Load Regulation**

Table 2-100 • SPI Characteristics
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp6	Data from master (SPI_x_DO) setup time [2]	1	1	1	pclk cycles
sp7	Data from master (SPI_x_DO) hold time [2]	1	1	1	pclk cycles
sp8	SPI_x_DI setup time [2]	1	1	1	pclk cycles
sp9	SPI_x_DI hold time [2]	1	1	1	pclk cycles

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

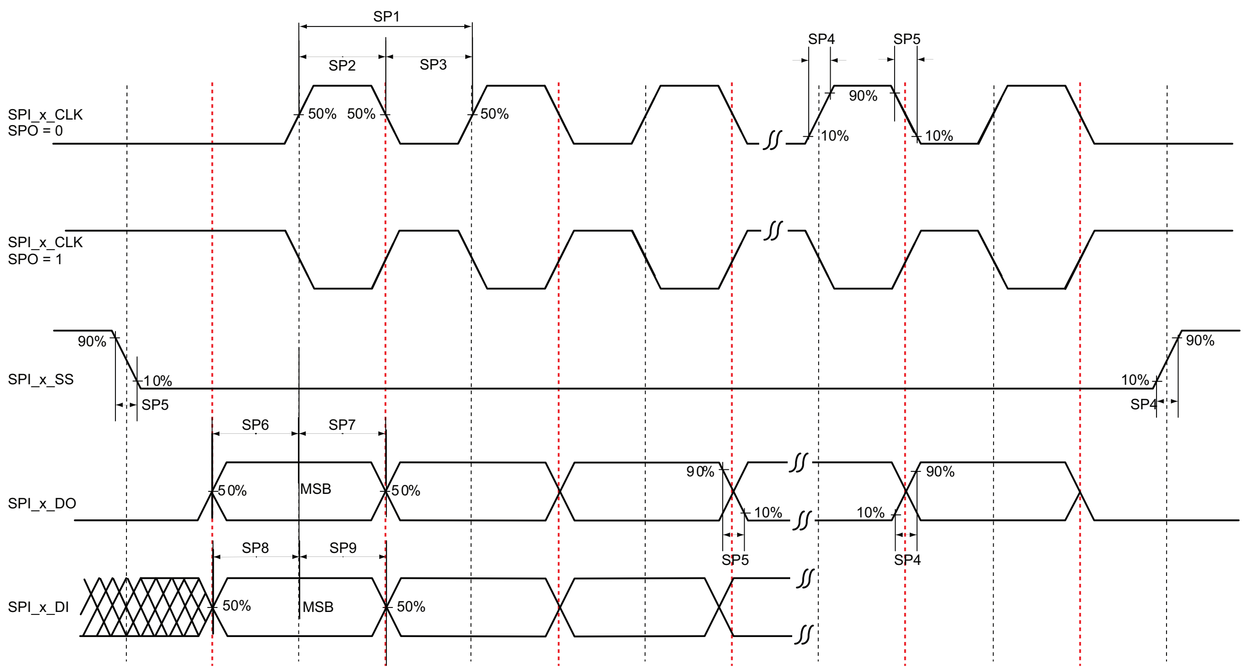

***Figure 2-47* • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

Pin No.	CS288		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
U5	VCC33SDD0	VCC33SDD0	VCC33SDD0
U6	VCC15A	VCC15A	VCC15A
U7	NC	ABPS3	ABPS3
U8	NC	ADC2	ADC2
U9	NC	VCC33ADC0	VCC33ADC0
U10	GND15ADC0	GND15ADC1	GND15ADC1
U11	VCC33ADC0	VCC33ADC1	VCC33ADC1
U12	ADC10	ADC7	ADC7
U13	ABPS0	ABPS6	ABPS6
U14	GNDTM0	GNDTM1	GNDTM1
U15	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
U16	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
U17	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
U19	GND	GND	GND
U21	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
V1	NC	MAC_CLK	MAC_CLK
V3	GNDSDD0	GNDSDD0	GNDSDD0
V19	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
V21	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
W1	PCAP	PCAP	PCAP
W3	NCAP	NCAP	NCAP
W4	ADC2	CM0	CM0
W5	ADC3	TM0	TM0
W6	ADC4	TM1	TM1
W7	NC	ADC0	ADC0
W8	NC	ADC3	ADC3
W9	NC	GND33ADC0	GND33ADC0
W10	VCC15ADC0	VCC15ADC1	VCC15ADC1
W11	GND33ADC0	GND33ADC1	GND33ADC1
W12	ADC8	ADC5	ADC5
W13	CM0	CM3	CM3

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
63	TM1	TM1
64	CM1	CM1
65	ABPS3	ABPS3
66	ABPS2	ABPS2
67	ADC0	ADC0
68	ADC1	ADC1
69	ADC2	ADC2
70	ADC3	ADC3
71	VAREF0	VAREF0
72	GND33ADC0	GND33ADC0
73	VCC33ADC0	VCC33ADC0
74	GND33ADC0	GND33ADC0
75	VCC15ADC0	VCC15ADC0
76	GND15ADC0	GND15ADC0
77	GND15ADC1	GND15ADC1
78	VCC15ADC1	VCC15ADC1
79	GND33ADC1	GND33ADC1
80	VCC33ADC1	VCC33ADC1
81	GND33ADC1	GND33ADC1
82	VAREF1	VAREF1
83	ADC7	ADC7
84	ADC6	ADC6
85	ADC5	ADC5
86	ADC4	ADC4
87	ABPS6	ABPS6
88	ABPS7	ABPS7
89	CM3	CM3
90	TM3	TM3
91	GNDTM1	GNDTM1
92	TM2	TM2
93	CM2	CM2

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
94	ABPS5	ABPS5
95	ABPS4	ABPS4
96	GNDAQ	GNDAQ
97	GNDA	GNDA
98	NC	NC
99	GNDVAREF	GNDVAREF
100	VAREFOUT	VAREFOUT
101	PU_N	PU_N
102	VCC33A	VCC33A
103	PTEM	PTEM
104	PTBASE	PTBASE
105	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
106	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
107	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
108	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
109	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
110	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
111	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
112	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
113	VCC	VCC
114	VCCMSSIOB2	VCCMSSIOB2
115	GND	GND
116	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
117	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
118	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
119	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
120	GNDENVM	GNDENVM
121	VCCENVM	VCCENVM
122	JTAGSEL	JTAGSEL
123	TCK	TCK
124	TDI	TDI

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
156	GNDQ	GNDQ
157	GNDQ	GNDQ
158	VCCFPGAIOB0	VCCFPGAIOB0
159	GBA1/IO19PDB0V0	GBA1/IO23PDB0V0
160	GBA0/IO19NDB0V0	GBA0/IO23NDB0V0
161	VCCFPGAIOB0	VCCFPGAIOB0
162	GND	GND
163	VCC	VCC
164	EMC_AB[25]/IO16PDB0V0	IO21PDB0V0
165	EMC_AB[24]/IO16NDB0V0	IO21NDB0V0
166	EMC_AB[23]/IO15PDB0V0	IO20PDB0V0
167	EMC_AB[22]/IO15NDB0V0	IO20NDB0V0
168	EMC_AB[21]/IO14PDB0V0	IO19PDB0V0
169	EMC_AB[20]/IO14NDB0V0	IO19NDB0V0
170	EMC_AB[19]/IO13PDB0V0	IO18PDB0V0
171	EMC_AB[18]/IO13NDB0V0	IO18NDB0V0
172	EMC_AB[17]/IO12PDB0V0	IO17PDB0V0
173	EMC_AB[16]/IO12NDB0V0	IO17NDB0V0
174	VCCFPGAIOB0	VCCFPGAIOB0
175	GND	GND
176	VCC	VCC
177	EMC_AB[15]/IO11PDB0V0	IO14PDB0V0
178	EMC_AB[14]/IO11NDB0V0	IO14NDB0V0
179	EMC_AB[13]/IO10PDB0V0	IO13PDB0V0
180	EMC_AB[12]/IO10NDB0V0	IO13NDB0V0
181	EMC_AB[11]/IO09PDB0V0	IO12PDB0V0
182	EMC_AB[10]/IO09NDB0V0	IO12NDB0V0
183	EMC_AB[9]/IO08PDB0V0	IO11PDB0V0
184	EMC_AB[8]/IO08NDB0V0	IO11NDB0V0
185	EMC_AB[7]/IO07PDB0V0	IO10PDB0V0
186	EMC_AB[6]/IO07NDB0V0	IO10NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
A1	GND	GND	GND
A2	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A3	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A4	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A5	GND	GND	GND
A6	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
A7	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
A8	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A9	GND	GND	GND
A10	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
A11	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
A12	GND	GND	GND
A13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A14	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A15	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A16	GND	GND	GND
B1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND	GND
B3	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
B4	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
B5	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
B6	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B7	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
B8	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
B9	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
B10	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
B11	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
B12	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B13	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
B14	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
B15	GND	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
H7	GND	GND
H8	VCC	VCC
H9	GND	GND
H10	VCC	VCC
H11	GND	GND
H12	VCC	VCC
H13	GND	GND
H14	VCC	VCC
H15	GND	GND
H16	VCCFPGAIOB1	VCCFPGAIOB1
H17	IO25NDB1V0	IO29NDB1V0
H18	GCC2/IO25PDB1V0	GCC2/IO29PDB1V0
H19	GND	GND
H20	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
H21	VCCFPGAIOB1	VCCFPGAIOB1
H22	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
J1	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J2	EMC_DB[5]/GEA1/IO61PDB5V0	EMC_DB[5]/GEA1/IO78PDB5V0
J3	EMC_DB[4]/GEA0/IO61NDB5V0	EMC_DB[4]/GEA0/IO78NDB5V0
J4	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
J5	VCCFPGAIOB5	VCCFPGAIOB5
J6	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5
J8	GND	GND
J9	VCC	VCC
J10	GND	GND
J11	VCC	VCC
J12	GND	GND
J13	VCC	VCC
J14	GND	GND
J15	VCC	VCC
J16	GND	GND
J17	NC	IO37PDB1V0
J18	VCCFPGAIOB1	VCCFPGAIOB1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

6 – Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 13 (March 2015)	Updated Unused MSS I/O Configuration information in "User I/O Naming Conventions" (SAR 62994).	5-7
	Updated Table 2-90: "eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V". Changed the maximum clock frequency for the control logic – 5 cycles to 50 MHz for A2F060 and A2F200 devices (SAR 63920). Added the following Note: "Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%" (SAR 63920).	2-76
Revision 12 (November 2013)	CS288 package dimensions added to "SmartFusion cSoC Package Sizes Dimensions" table (SAR 43730).	1-III
	Added "Typical Programming and Erase Times" table (SAR 43732).	4-9
	Definition of Ethernet MAC clarified in the "General Description" section (SAR 50083).	1-1
	Clarified GC and GF global inputs in "Global I/O Naming Conventions" section and link to SF Fabric UG added (SAR 42802).	5-6
Revision 11 (September 2013)	Modified the description for VAREF0 in the "User-Defined Supply Pins"(SAR 30204).	5-5
	Updated the "Pin Assignment Tables" section with a note for A2F500, all packages with GCAx saying: "Signal assigned to those pins as a CLKBUF or CLKBUF_LVPECL or CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal (SAR 45985).	5-18

Revision	Changes	Page
Revision 5 (continued)	Available values for the Std. speed were added to the timing tables from Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew to Table 2-92 • JTAG 1532 (SAR 29331). One or more values changed for the –1 speed in tables covering 3.3 V LVCMOS, 2.5 V LVCMOS, 1.8 V LVCMOS, 1.5 V LVCMOS, Combinatorial Cell Propagation Delays, and A2F200 Global Resources.	2-31 to 2-76
	Table 2-80 • A2F500 Global Resource is new.	2-60
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised (SAR 27585).	2-76
	The programmable analog specifications tables were revised with updated information.	2-78 to 2-87
	Table 4-1 • Supported JTAG Programming Hardware was revised by adding a note to indicate "planned support" for several of the items in the table.	4-7
	The note on JTAGSEL in the "In-System Programming" section was revised to state that SoftConsole selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care" (SAR 29261).	4-7
	The "CS288" and "FG256" pin tables for A2F060 are new, comparing the A2F060 function with the A2F200 function (SAR 29353).	5-24
	The "Handling When Unused" column was removed from the "FG256" pin table for A2F200 and A2F500 (SAR 29691).	5-42
Revision 4 (September 2010)	Table 2-8 • Power Supplies Configuration was revised. VCCRCOSC was moved to a column of its own with new values. VCCENVM was added to the table. Standby mode for VJTAG and VPP was changed from 0 V to N/A. "Disable" was changed to "Off" in the eNVM column. The column for RCOSC was deleted.	2-10
	The "Power-Down and Sleep Mode Implementation" section was revised to include VCCROSC.	2-11
Revision 3 (September 2010)	The "I/Os and Operating Voltage" section was revised to list "single 3.3 V power supply with on-chip 1.5 V regulator" and "external 1.5 V is allowed" (SAR 27663).	I
	The CS288 package was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 27101), "Product Ordering Codes" table, and "Temperature Grade Offerings" table (SAR 27044). The number of direct analog inputs for the FG256 package in A2F060 was changed from 8 to 6.	III, VI, VI
	Two notes were added to the "SmartFusion cSoC Family Product Table" indicating limitations for features of the A2F500 device: *Two PLLs are available in CS288 and FG484 (one PLL in FG256).* *[ADCs, DACs, SCBs, comparators, current monitors, and bipolar high voltage monitors are] Available on FG484 only. FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.* Table cells were merged in rows containing the same values for easier reading (SAR 24748).	II
	The security feature option was added to the "Product Ordering Codes" table.	VI