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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1csg288i

SmartFusion cSoC Family Product Table

	A2F060			A2F200				A2F500			
FPGA Fabric	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
System Gates	60,000			200,000				500,000			
Tiles (D-flip-flops)	1,536			4,608				11,520			
RAM Blocks (4,608 bits)	8			8				24			
	A2F060			**A2F200**				**A2F500**			
Microcontroller Subsystem (MSS)	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Flash (Kbytes)	128			256				512			
SRAM (Kbytes)	16			64				64			
Cortex-M3 processor with MPU	Yes			Yes				Yes			
10/100 Ethernet MAC	No			Yes				Yes			
External Memory Controller (EMC)	–	26-/16-bit address/data		26-bit address,16-bit data				–	26-/16-bit address/data		
DMA	8 Ch			8 Ch				8 Ch			
I^2C	2			2				2			
SPI	1	2		1	2			1	2		
16550 UART	2			2				2			
32-Bit Timer	2			2				2			
PLL	1			1				1	2	1	2
32 KHz Low Power Oscillator	1			1				1			
100 MHz On-Chip RC Oscillator	1			1				1			
Main Oscillator (32 KHz to 20 MHz)	1			1				1			
	A2F060			**A2F200**				**A2F500**			
Programmable Analog	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
ADCs (8-/10-/12-bit SAR)	1			2				2			3
DACs (8-/16-/24-bit sigma-delta)	1			2				2			3
Signal Conditioning Blocks (SCBs)	1			4				4			5
Comparator*	2			8				8			10
Current Monitors*	1			4				4			5
Temperature Monitors*	1			4				4			5
Bipolar High Voltage Monitors*	2			8				8			10

Note: **These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130925 for details.*

Package I/Os: MSS + FPGA I/Os

Device	A2F060[1]			A2F200[2]				A2F500[2]			
Package	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Inputs	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Inputs	4	4	4	16	16	16	16	16	16	16	20
Total Analog Inputs	15	15	15	24	24	24	24	24	24	24	32
Analog Outputs	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[3,4]	21[5]	28[5]	26[5]	22	31	25	41	22	31	25	41
FPGA I/Os	33[6]	68	66	66	78	66	94	66[6]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:
1. *There are no LVTTL capable direct inputs available on A2F060 devices.*
2. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
3. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
4. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
5. *10/100 Ethernet MAC is not available on A2F060.*
6. *EMC is not available on the A2F500 PQ208 and A2F060 TQ144 package.*

Table 1 • SmartFusion cSoC Package Sizes Dimensions

Package	TQ144	PQ208	CS288	FG256	FG484
Length × Width (mm\mm)	20 × 20	28 × 28	11 × 11	17 × 17	23 × 23
Nominal Area (mm^2)	400	784	121	289	529
Pitch (mm)	0.5	0.5	0.5	1.0	1.0
Height (mm)	1.40	3.40	1.05	1.60	2.23

SmartFusion cSoC Device Status

Device	Status
A2F060	Preliminary: CS288, FG256, TQ144
A2F200	Production: CS288, FG256, FG484, PQ208
A2F500	Production: CS288, FG256, FG484, PQ208

This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User’s Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

2 – SmartFusion DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond the operating conditions listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-3 on page 2-3 is not implied.

***Table 2-1* • Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPP	Programming voltage	–0.3 to 3.75	V
VCCPLLx	Analog power supply (PLL)	–0.3 to 1.65	V
VCCFPGAIOBx	DC FPGA I/O buffer supply voltage	–0.3 to 3.75	V
VCCMSSIOBx	DC MSS I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCxxxxIOBx + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	Analog clean 3.3 V supply to the analog circuitry	–0.3 to 3.75	V
VCC33ADCx	Analog 3.3 V supply to ADC	–0.3 to 3.75	V
VCC33AP	Analog clean 3.3 V supply to the charge pump	–0.3 to 3.75	V
VCC33SDDx	Analog 3.3 V supply to the sigma-delta DAC	–0.3 to 3.75	V
VAREFx	Voltage reference for ADC	1.0 to 3.75	V
VCCRCOSC	Analog supply to the integrated RC oscillator	–0.3 to 3.75	V
VDDBAT	External battery supply	–0.3 to 3.75	V
VCCMAINXTAL	Analog supply to the main crystal oscillator	–0.3 to 3.75	V
VCCLPXTAL	Analog supply to the low power 32 kHz crystal oscillator	–0.3 to 3.75	V
VCCENVM	Embedded nonvolatile memory supply	–0.3 to 1.65	V
VCCESRAM	Embedded SRAM supply	–0.3 to 1.65	V
VCC15A	Analog 1.5 V supply to the analog circuitry	–0.3 to 1.65	V
VCC15ADCx	Analog 1.5 V supply to the ADC	–0.3 to 1.65	V
T_{STG} [1]	Storage temperature	–65 to +150	°C
T_J [1]	Junction temperature	125	°C

Notes:

1. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-4. For recommended operating conditions, refer to Table 2-3 on page 2-3.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-5 on page 2-4.*

Standby Mode

$P_{DYN} = P_{RC\text{-}OSC} + P_{LPXTAL\text{-}OSC}$

Time Keeping Mode

$P_{DYN} = P_{LPXTAL\text{-}OSC}$

Global Clock Dynamic Contribution—P_{CLOCK}

SoC Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Time Keeping Mode

$P_{CLOCK} = 0\ W$

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

SoC Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{S\text{-}CELL} = 0\ W$

Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

SoC Mode

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{C\text{-}CELL} = 0\ W$

Routing Net Dynamic Contribution—P_{NET}

SoC Mode

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the frequency of the clock driving the logic including these nets.

User I/O Characteristics

Timing Model

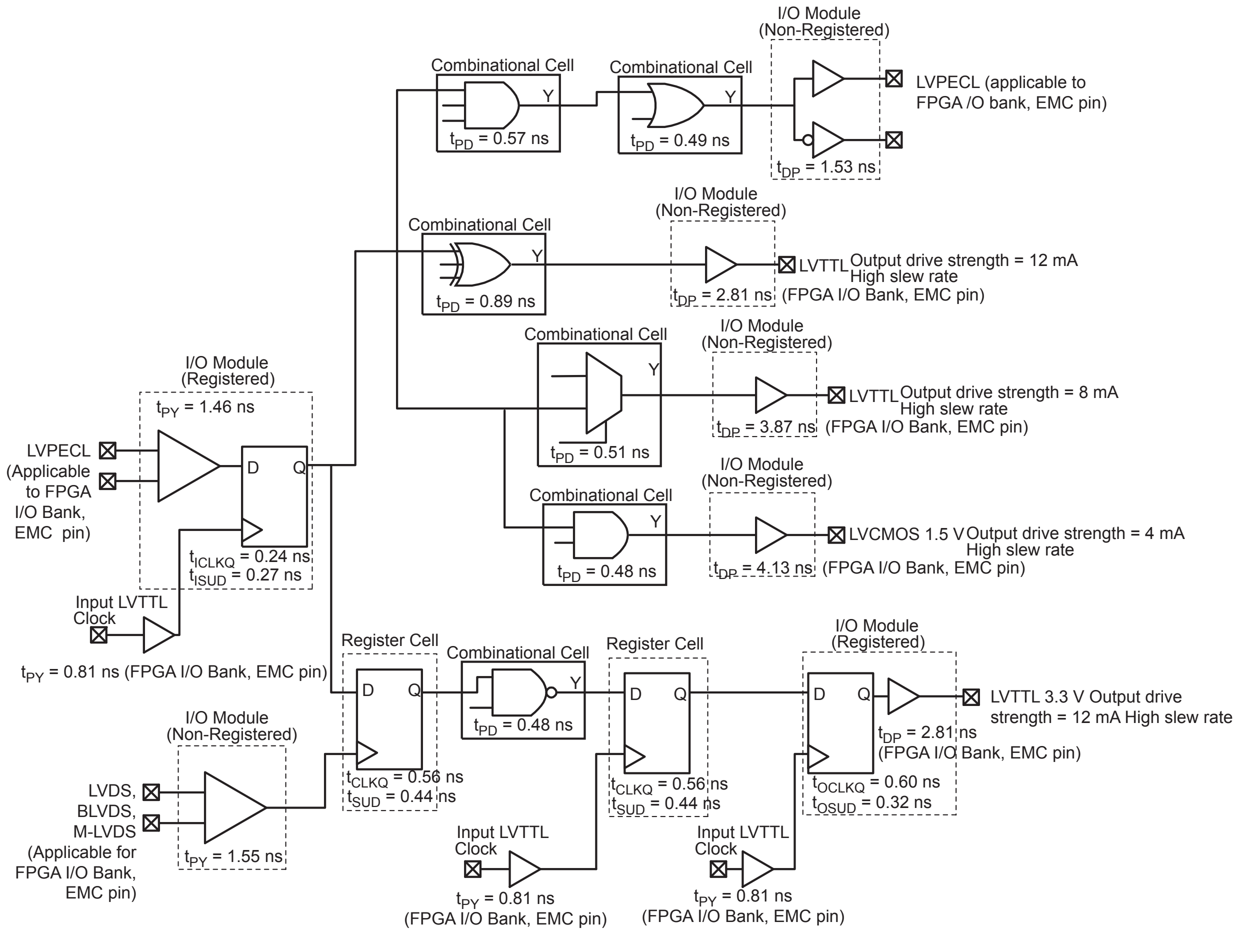

Figure 2-2 • **Timing Model**
Operating Conditions: –1 Speed, Commercial Temperature Range (T_J = 85°C), Worst Case VCC = 1.425 V

Timing Characteristics

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	7.20	0.04	0.97	0.39	7.34	6.18	2.52	2.46	9.39	8.23	ns
	–1	0.50	6.00	0.03	0.81	0.32	6.11	5.15	2.10	2.05	7.83	6.86	ns
8 mA	Std.	0.60	4.64	0.04	0.97	0.39	4.73	3.84	2.85	3.02	6.79	5.90	ns
	–1	0.50	3.87	0.03	0.81	0.32	3.94	3.20	2.37	2.52	5.65	4.91	ns
12 mA	Std.	0.60	3.37	0.04	0.97	0.39	3.43	2.67	3.07	3.39	5.49	4.73	ns
	–1	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
16 mA	Std.	0.60	3.18	0.04	0.97	0.39	3.24	2.43	3.11	3.48	5.30	4.49	ns
	–1	0.50	2.65	0.03	0.81	0.32	2.70	2.03	2.59	2.90	4.42	3.74	ns
24 mA	Std.	0.60	2.93	0.04	0.97	0.39	2.99	2.03	3.17	3.83	5.05	4.09	ns
	–1	0.50	2.45	0.03	0.81	0.32	2.49	1.69	2.64	3.19	4.21	3.41	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	9.75	0.04	0.97	0.39	9.93	8.22	2.52	2.31	11.99	10.28	ns
	–1	0.50	8.12	0.03	0.81	0.32	8.27	6.85	2.10	1.93	9.99	8.57	ns
8 mA	Std.	0.60	6.96	0.04	0.97	0.39	7.09	5.85	2.84	2.87	9.15	7.91	ns
	–1	0.50	5.80	0.03	0.81	0.32	5.91	4.88	2.37	2.39	7.62	6.59	ns
12 mA	Std.	0.60	5.35	0.04	0.97	0.39	5.45	4.58	3.06	3.23	7.51	6.64	ns
	–1	0.50	4.46	0.03	0.81	0.32	4.54	3.82	2.55	2.69	6.26	5.53	ns
16 mA	Std.	0.60	5.01	0.04	0.97	0.39	5.10	4.30	3.11	3.32	7.16	6.36	ns
	–1	0.50	4.17	0.03	0.81	0.32	4.25	3.58	2.59	2.77	5.97	5.30	ns
24 mA	Std.	0.60	4.67	0.04	0.97	0.39	4.75	4.28	3.16	3.66	6.81	6.34	ns
	–1	0.50	3.89	0.03	0.81	0.32	3.96	3.57	2.64	3.05	5.68	5.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-40 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.31	0.09	0.94	1.30	0.22	2.35	1.86	2.20	2.45	ns
	–1	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-52 • 1.8 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	Std.	0.22	2.77	0.09	1.09	1.64	0.22	2.82	2.72	2.21	2.25	ns
	–1	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-69 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* See Figure 2-14 on page 2-44 for more information.

Input Register

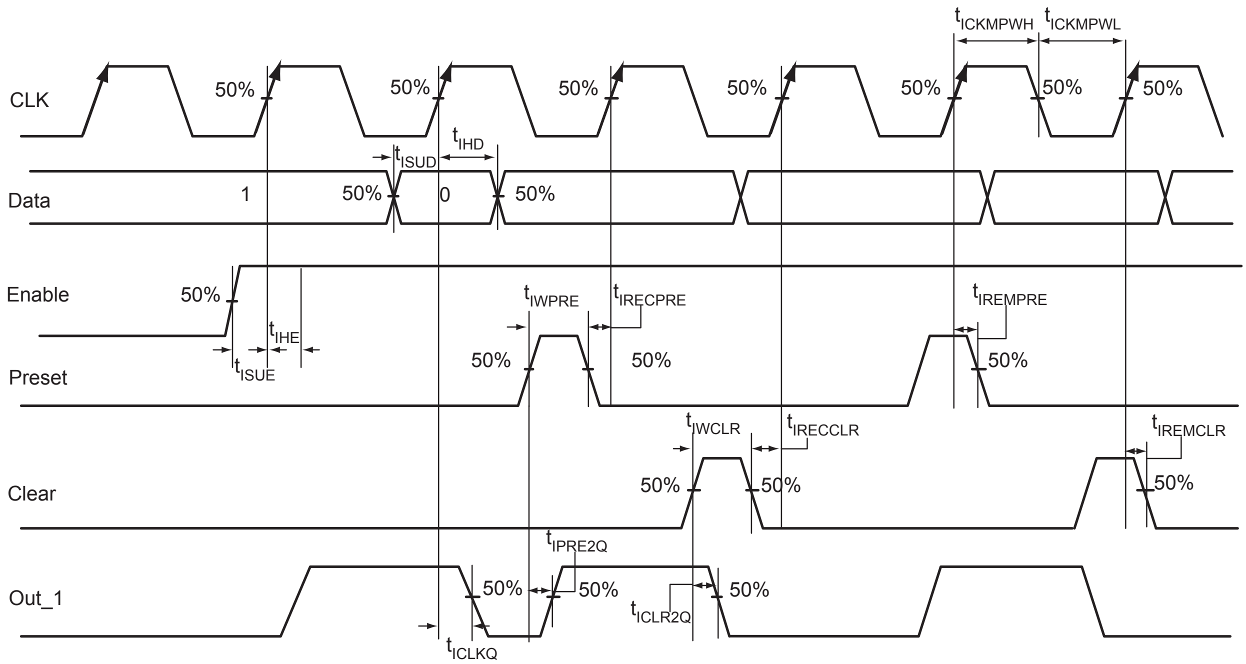

Figure 2-16 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-71 • **Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.55	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.55	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.32	ns

Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Output Enable Register

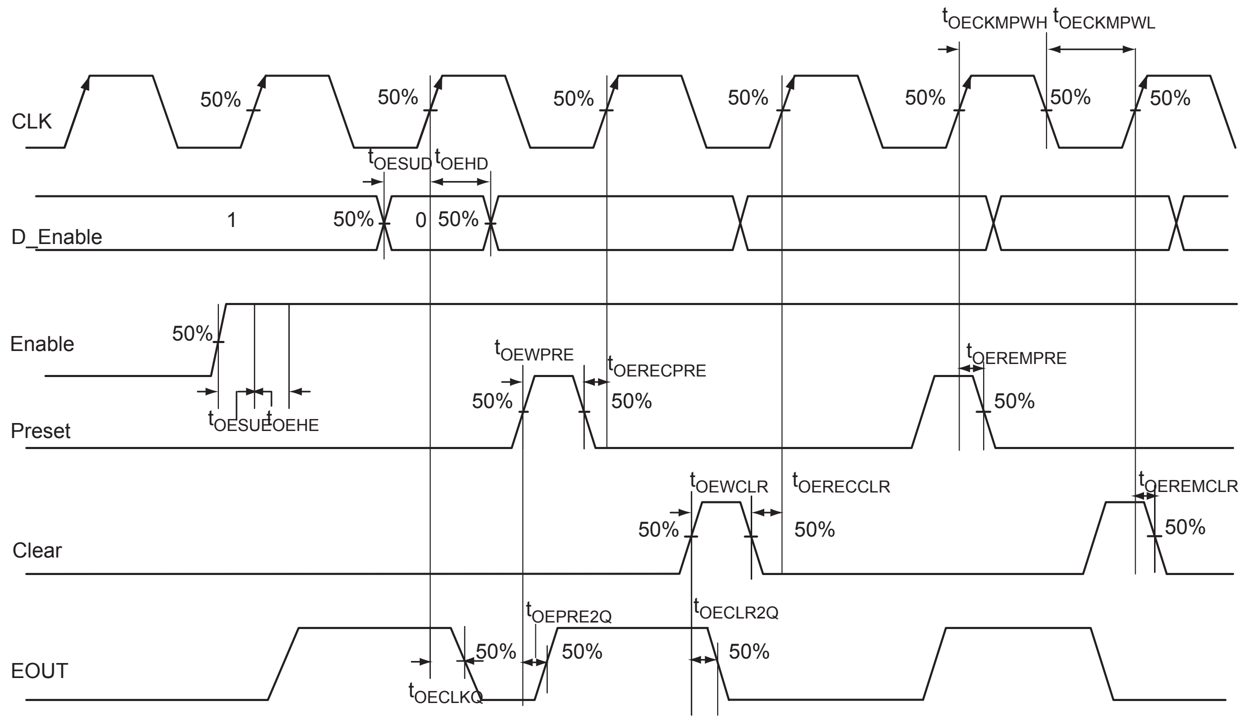

Figure 2-18 **• Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-73 **• Output Enable Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.54	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.38	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.53	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-78 • **Combinatorial Cell Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

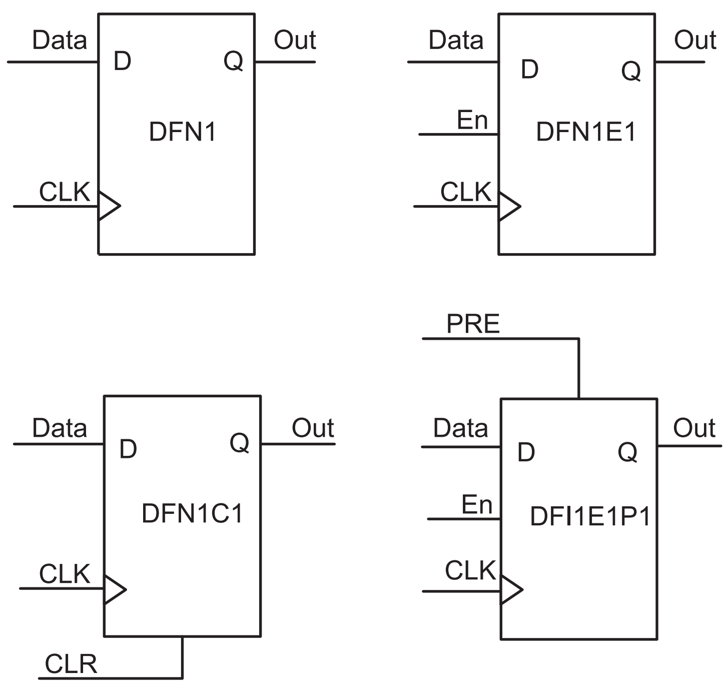

Figure 2-25 • **Sample of Sequential Cells**

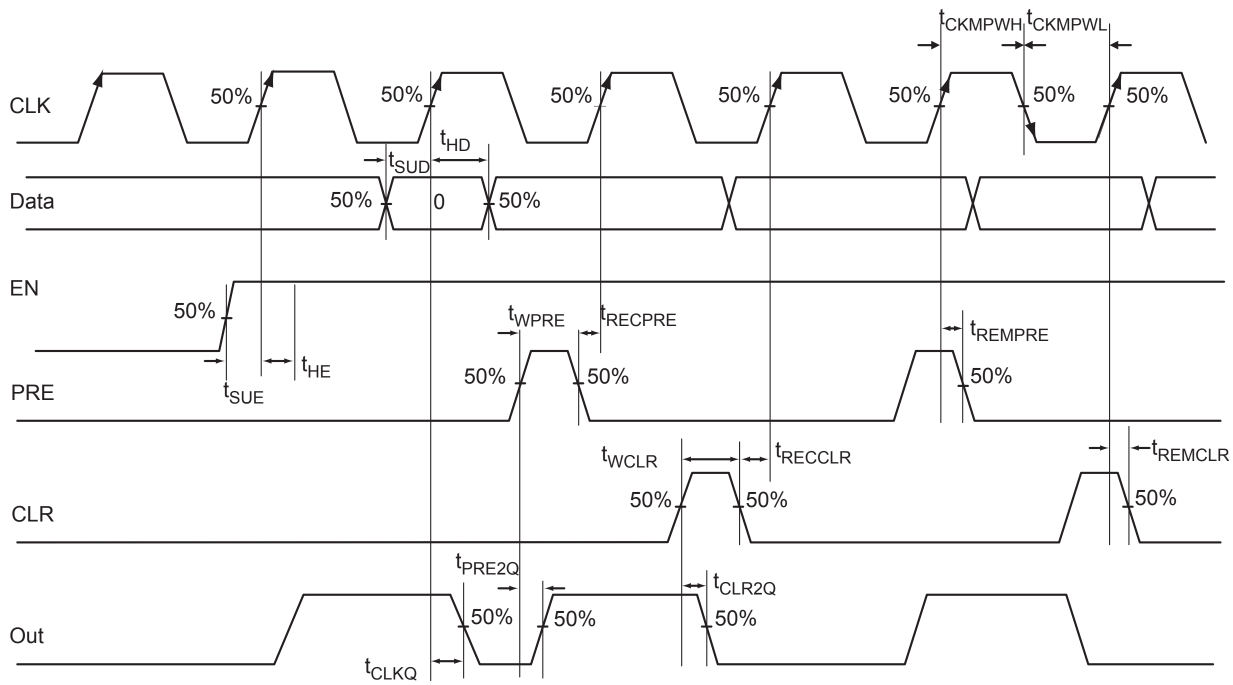

Figure 2-26 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-79 • **Register Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.56	0.67	ns
t_{SUD}	Data Setup Time for the Core Register	0.44	0.52	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.46	0.55	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.41	0.49	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.41	0.49	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.23	0.27	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	0.27	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.22	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.22	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.32	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

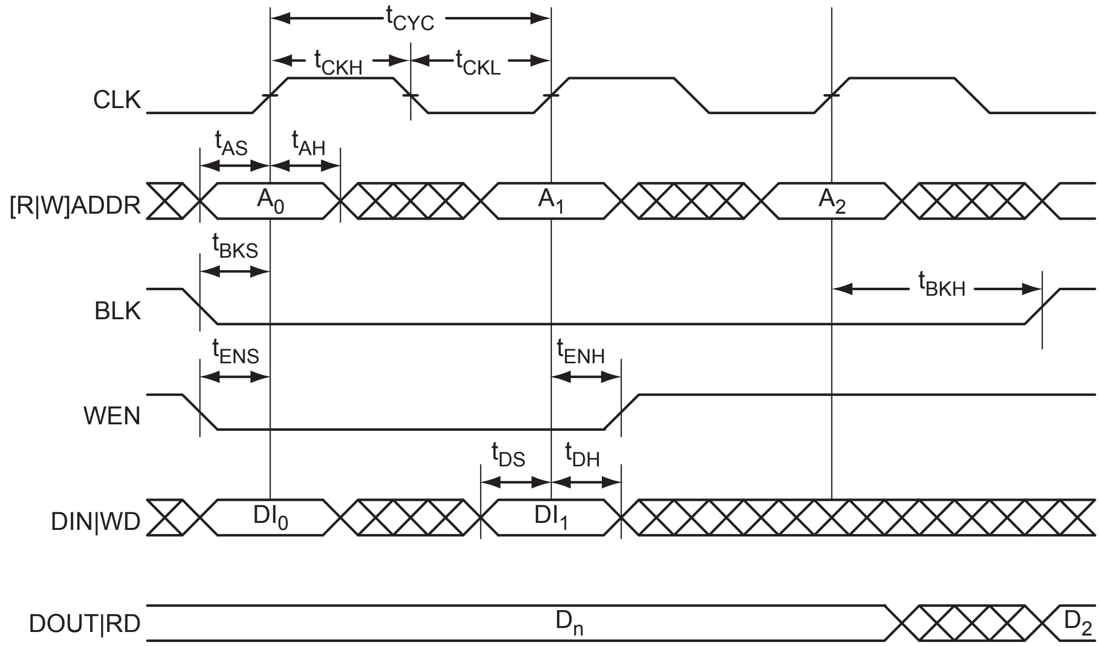

Figure 2-32 • **RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.**

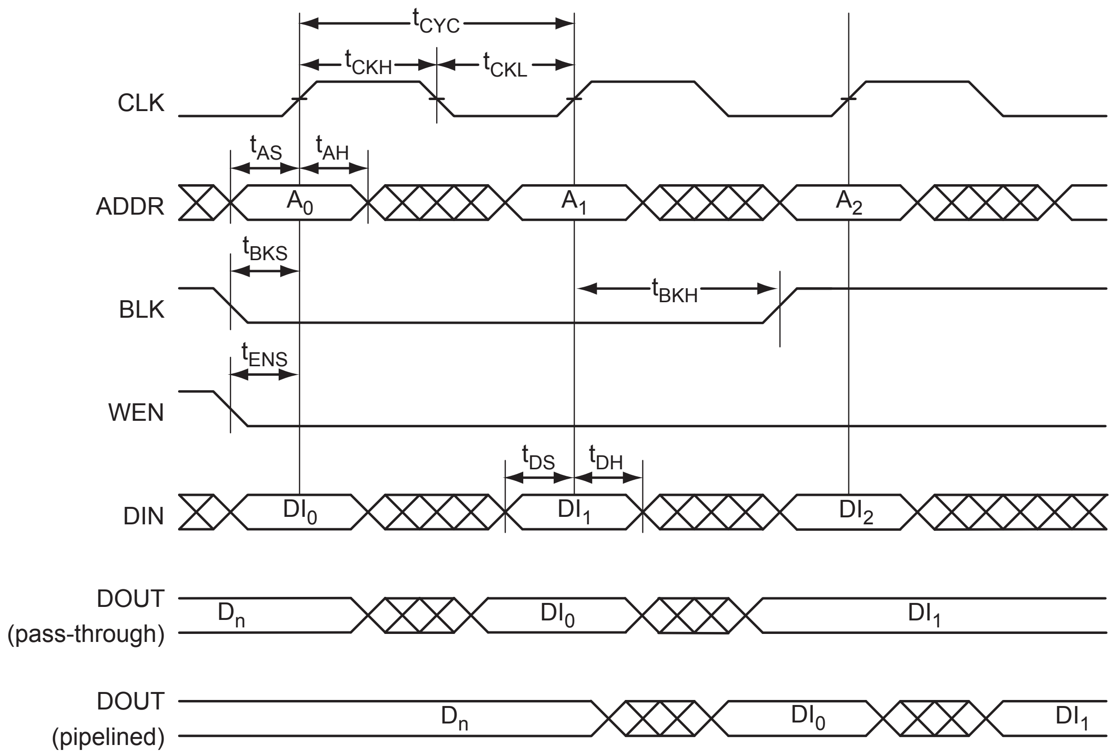

Figure 2-33 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-47 on page 2-90.

Table 2-100 **• SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp1	SPI_x_CLK minimum period				
	SPI_x_CLK = PCLK/2	20	NA	20	ns
	SPI_x_CLK = PCLK/4	40	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [1]	4.7	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [1]	3.4	3.4	3.4	ns

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

TQ144	
Pin Number	**A2F060 Function**
1	VCCPLL0
2	VCOMPLA0
3	GNDQ
4	GFA2/IO42PDB5V0
5	GFB2/IO42NDB5V0
6	GFC2/IO41PDB5V0
7	IO41NDB5V0
8	VCC
9	GND
10	VCCFPGAIOB5
11	IO38PDB5V0
12	IO38NDB5V0
13	IO36PDB5V0
14	IO36NDB5V0
15	GND
16	GNDRCOSC
17	VCCRCOSC
18	MSS_RESET_N
19	GPIO_0/IO33RSB4V0
20	GPIO_1/IO32RSB4V0
21	GPIO_2/IO31RSB4V0
22	GPIO_3/IO30RSB4V0
23	GPIO_4/IO29RSB4V0
24	GND
25	VCCMSSIOB4
26	VCC
27	GPIO_5/IO28RSB4V0
28	GPIO_6/IO27RSB4V0
29	GPIO_7/IO26RSB4V0
30	GPIO_8/IO25RSB4V0
31	VCCESRAM
32	GNDSDD0
33	VCC33SDD0
34	VCC15A
35	PCAP
36	NCAP

PQ208

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 8 (continued)	The description of "In-application programming (IAP)" methodology was changed to state the difference for A2F060 and A2F500 compared to A2F200 (SAR 37808).	4-7
	The "Global I/O Naming Conventions" section is new (SARs 28996, 31147). The description for IO "User Pins" was revised accordingly and moved out of the table and into a new section: "User I/O Naming Conventions".	5-6, 5-6
	The descriptions for "MAINXIN" and "MAINXOUT" were revised to state how they should be handled if using an external RC network or clock input (SAR 32594).	5-8
	The description and type was revised for the "MSS_RESET_N" pin (SAR 34133).	5-9
	The "TQ144" section and pin table for A2F060 are new (SAR 36246).	5-18
Revision 7 (August 2011)	The title of the datasheet was changed from SmartFusion Intelligent Mixed Signal FPGAs to SmartFusion Customizable System-on-Chip (cSoC). Terminology throughout was changed accordingly. The term cSoC defines a category of devices that include at least FPGA fabric and a processor subsystem of some sort. It can also include any of the following: analog, SerDes, ASIC blocks, customer specific IP, or application-specific IP. SmartFusion is Microsemi's first cSoC (SAR 33071).	N/A
	The "SmartFusion cSoC Family Product Table" was revised to remove the note stating that the A2F060 device is under definition and subject to change (SAR 33070). A note was added for EMC, stating that it is not available on A2F500 for the PQ208 package (SAR 33041).	II
	The "SmartFusion cSoC Device Status" table was revised. The status for A2F060 CS288 and FG256 moved from Advance to Preliminary. A2F200 PQ208 and A2F500 PQ208 moved from Advance to Production (SAR 33069).	III
	The "Package I/Os: MSS + FPGA I/Os" table was revised. The number of direct analog inputs for A2F060 packages increased from 6 to 11. The number of MSS I/Os for the A2F060 FG256 package increased from 25 to 26 (SAR 33070). A note was added stating that EMC is not available for the A2F500 PQ208 package (SAR 33041).	III
	The note associated with the "SmartFusion cSoC System Architecture" diagram was corrected from "Architecture for A2F500" to "Architecture for A2F200" (SAR 32578).	V
	The Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 32151).	VI
	The "Security" section and "Secure Programming" section were updated to clarify that although no existing security measures can give an absolute guarantee, SmartFusion cSoCs implement the best security available in the industry (SAR 32865).	1-2, 4-9
	Storage temperature, T_{STG}, and junction temperature, T_J, were added to Table 2-1 • Absolute Maximum Ratings (SAR 30863).	2-1
	AC/DC characteristics for A2F060 were added to the "SmartFusion DC and Switching Characteristics" chapter (SAR 33132). The following tables were updated: Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V Table 2-98 • Analog Sigma-Delta DAC Table 2-100 • SPI Characteristics	 2-12 2-13 2-76 2-85 2-89

Revision	Changes	Page
Revision 3 (continued)	Two notes were added to the "Supply Pins" table (SAR 27109): *1. The following supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* *2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	5-1
	The descriptions for the "VCC33N", "NCAP", and "PCAP" pins were revised to include information on what to do if analog SCB features and SDDs are not used (SAR 26744).	5-2, 5-9, 5-9
	Information was added to the "User Pins" table regarding tristating of used and unused GPIO pins. The IO portion of the table was revised to state that unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor (SAR 26890). Information was added regarding behavior of used I/O pins during power-up.	5-6
	The type for "EMC_RW_N" was changed from In/out to Out (SAR 25113).	5-12
	A note was added to the "Analog Front-End (AFE)" table stating that unused analog inputs should be grounded (SAR 26744).	5-14
	The "TQ144" section is new, with pin tables for A2F200 and A2F500 (SAR 27044).	5-18
	The "FG256" pin table was replaced and now includes "Handling When Unused" information (SAR 27709).	5-42
Revision 2 (May 2010)	Embedded nonvolatile flash memory (eNVM) was changed from "64 to 512 Kbytes" to "128 to 512 Kbytes" in the "Microcontroller Subsystem (MSS)" section and "SmartFusion cSoC Family Product Table" (SAR 26005).	I, II
	The main oscillator range of values was changed to "32 KHz to 20 MHz" in the "Microcontroller Subsystem (MSS)" section and the "SmartFusion cSoC Family Product Table" (SAR 24906).	I, II
	The value for t_{PD} was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the "Analog Front-End (AFE)" section (SAR 26005).	I
	The number of PLLs for A2F200 was changed from 2 to 1 in the "SmartFusion cSoC Family Product Table" (SAR 25093).	II
	Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the "Package I/Os: MSS + FPGA I/Os" table. The Max. column was removed from the table (SAR 26005).	III
	The Speed Grade section of the "Product Ordering Codes" table was revised (SAR 25257).	VI
Revision 1 (March 2010)	The "Product Ordering Codes" table was revised to add "blank" as an option for lead-free packaging and application (junction temperature range).	VI
	Table 2-3 • Recommended Operating Conditions[5,6] was revised. Ta (ambient temperature) was replaced with T_J (junction temperature).	2-3
	PDC5 was deleted from Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs.	2-13
	The formulas in the footnotes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised.	2-27
	The values for input biased current were revised in Table 2-93 • Current Monitor Performance Specification.	2-78
Revision 0 (March 2010)	The "Analog Front-End (AFE)" section was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps.	I