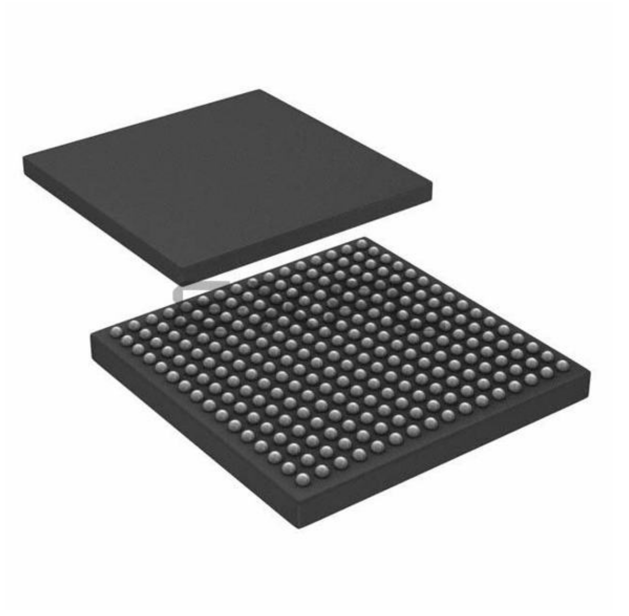
Microchip Technology - A2F500M3G-1FGG256 Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

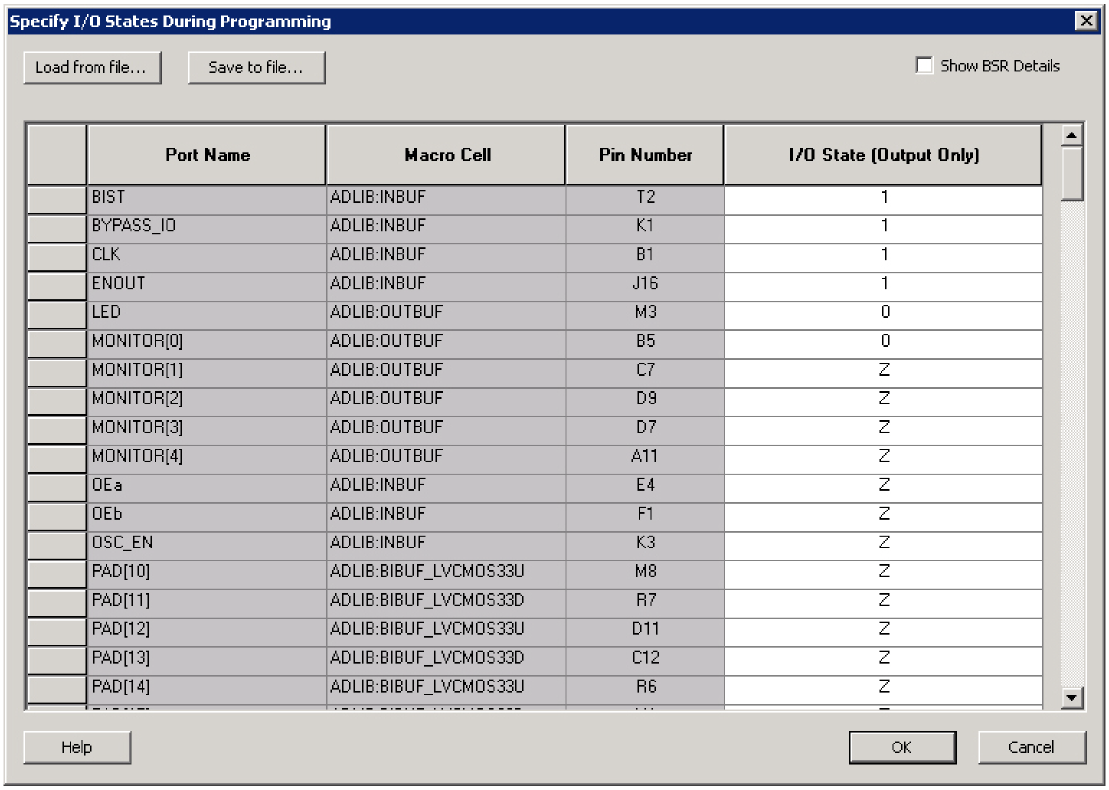
What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1fgg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Port Name	Macro Cell	Pin Number	I/O State (Output Only)
BIST	ADLIB:INBUF	T2	1
BYPASS_IO	ADLIB:INBUF	K1	1
CLK	ADLIB:INBUF	B1	1
ENOUT	ADLIB:INBUF	J16	1
LED	ADLIB:OUTBUF	M3	0
MONITOR[0]	ADLIB:OUTBUF	B5	0
MONITOR[1]	ADLIB:OUTBUF	C7	Z
MONITOR[2]	ADLIB:OUTBUF	D9	Z
MONITOR[3]	ADLIB:OUTBUF	D7	Z
MONITOR[4]	ADLIB:OUTBUF	A11	Z
OEa	ADLIB:INBUF	E4	Z
OEb	ADLIB:INBUF	F1	Z
OSC_EN	ADLIB:INBUF	K3	Z
PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

Figure 1-1 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – SmartFusion DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond the operating conditions listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-3 on page 2-3 is not implied.

***Table 2-1* • Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPP	Programming voltage	–0.3 to 3.75	V
VCCPLLx	Analog power supply (PLL)	–0.3 to 1.65	V
VCCFPGAIOBx	DC FPGA I/O buffer supply voltage	–0.3 to 3.75	V
VCCMSSIOBx	DC MSS I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCxxxxIOBx + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	Analog clean 3.3 V supply to the analog circuitry	–0.3 to 3.75	V
VCC33ADCx	Analog 3.3 V supply to ADC	–0.3 to 3.75	V
VCC33AP	Analog clean 3.3 V supply to the charge pump	–0.3 to 3.75	V
VCC33SDDx	Analog 3.3 V supply to the sigma-delta DAC	–0.3 to 3.75	V
VAREFx	Voltage reference for ADC	1.0 to 3.75	V
VCCRCOSC	Analog supply to the integrated RC oscillator	–0.3 to 3.75	V
VDDBAT	External battery supply	–0.3 to 3.75	V
VCCMAINXTAL	Analog supply to the main crystal oscillator	–0.3 to 3.75	V
VCCLPXTAL	Analog supply to the low power 32 kHz crystal oscillator	–0.3 to 3.75	V
VCCENVM	Embedded nonvolatile memory supply	–0.3 to 1.65	V
VCCESRAM	Embedded SRAM supply	–0.3 to 1.65	V
VCC15A	Analog 1.5 V supply to the analog circuitry	–0.3 to 1.65	V
VCC15ADCx	Analog 1.5 V supply to the ADC	–0.3 to 1.65	V
T_{STG}[1]	Storage temperature	–65 to +150	°C
T_J[1]	Junction temperature	125	°C

Notes:

1. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-4. For recommended operating conditions, refer to Table 2-3 on page 2-3.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-5 on page 2-4.*

Table 2-3 • **Recommended Operating Conditions**[5,6]

Symbol	Parameter[1]		Commercial	Industrial	Units
T_J	Junction temperature		0 to +85	–40 to +100	°C
VCC [2]	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.425 to 3.6	1.425 to 3.6	V
VPP	Programming voltage	Programming mode[3]	3.15 to 3.45	3.15 to 3.45	V
		Operation[4]	0 to 3.6	0 to 3.6	V
VCCPLLx	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCFPGAIOBx/ VCCMSSIOBx[5]	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A[6]	Analog clean 3.3 V supply to the analog circuitry		3.15 to 3.45	3.15 to 3.45	V
VCC33ADCx[6]	Analog 3.3 V supply to ADC		3.15 to 3.45	3.15 to 3.45	V
VCC33AP[6]	Analog clean 3.3 V supply to the charge pump		3.15 to 3.45	3.15 to 3.45	V
VCC33SDDx[6]	Analog 3.3 V supply to sigma-delta DAC		3.15 to 3.45	3.15 to 3.45	V
VAREFx	Voltage reference for ADC		2.527 to 3.3	2.527 to 3.3	V
VCCRCOSC	Analog supply to the integrated RC oscillator		3.15 to 3.45	3.15 to 3.45	V
VDDBAT	External battery supply		2.7 to 3.63	2.7 to 3.63	V
VCCMAINXTAL[6]	Analog supply to the main crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCLPXTAL[6]	Analog supply to the low power 32 KHz crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCENVM	Embedded nonvolatile memory supply		1.425 to 1.575	1.425 to 1.575	V
VCCESRAM	Embedded SRAM supply		1.425 to 1.575	1.425 to 1.575	V
VCC15A[2]	Analog 1.5 V supply to the analog circuitry		1.425 to 1.575	1.425 to 1.575	V
VCC15ADCx[2]	Analog 1.5 V supply to the ADC		1.425 to 1.575	1.425 to 1.575	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *The Programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.*
4. *VPP can be left floating during operation (not programming mode).*
5. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-19 on page 2-23. VCCxxxxIOBx should be at the same voltage within a given I/O bank.*
6. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*

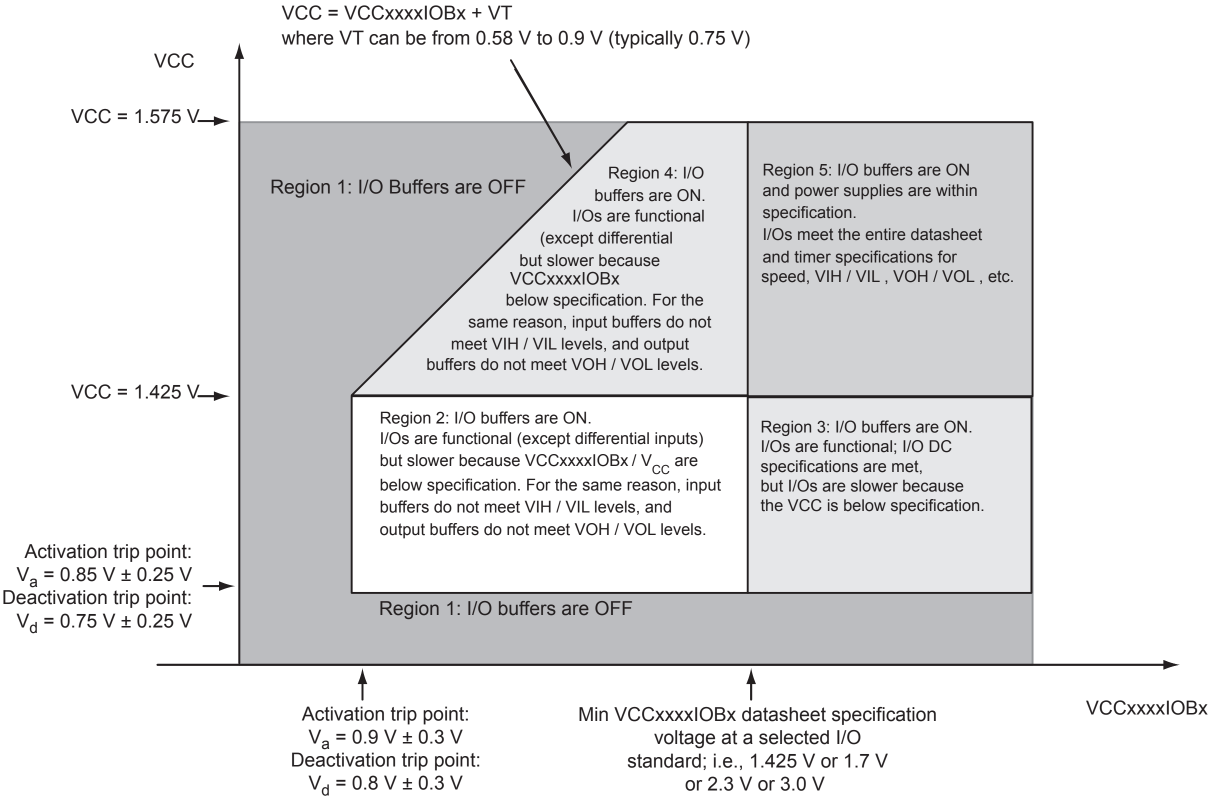


Figure 2-1 • **I/O State as a Function of VCCxxxxIOBx and VCC Voltage Levels**

Table 2-11 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks**

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-12 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings*[*] Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins**

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.74	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks**

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	155.65
2.5 V LVCMOS	10	2.5	–	88.23
1.8 V LVCMOS	10	1.8	–	45.03
1.5 V LVCMOS (JESD8-11)	10	1.5	–	31.01

Standby Mode and Time Keeping Mode

$P_{NET} = 0\ W$

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

SoC Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{INPUTS} = 0\ W$

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

SoC Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-18.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-18 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{OUTPUTS} = 0\ W$

FPGA Fabric SRAM Dynamic Contribution—P_{MEMORY}

SoC Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

Where:

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-18 on page 2-18.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 2-18 on page 2-18.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

Standby Mode and Time Keeping Mode

$P_{MEMORY} = 0\ W$

PLL/CCC Dynamic Contribution—P_{PLL}

SoC Mode

$P_{PLL} = P_{AC13} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Standby Mode and Time Keeping Mode

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[1] *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Detailed I/O DC Characteristics

Table 2-26 **• Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-27 **• I/O Output Buffer Maximum Resistances[1]**
Applicable to FPGA I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website (also generated by the SoC Products Group Libero SoC toolset).*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Timing Characteristics

Table 2-38 **• 3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	7.20	0.04	0.97	0.39	7.34	6.18	2.52	2.46	9.39	8.23	ns
	–1	0.50	6.00	0.03	0.81	0.32	6.11	5.15	2.10	2.05	7.83	6.86	ns
8 mA	Std.	0.60	4.64	0.04	0.97	0.39	4.73	3.84	2.85	3.02	6.79	5.90	ns
	–1	0.50	3.87	0.03	0.81	0.32	3.94	3.20	2.37	2.52	5.65	4.91	ns
12 mA	Std.	0.60	3.37	0.04	0.97	0.39	3.43	2.67	3.07	3.39	5.49	4.73	ns
	–1	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
16 mA	Std.	0.60	3.18	0.04	0.97	0.39	3.24	2.43	3.11	3.48	5.30	4.49	ns
	–1	0.50	2.65	0.03	0.81	0.32	2.70	2.03	2.59	2.90	4.42	3.74	ns
24 mA	Std.	0.60	2.93	0.04	0.97	0.39	2.99	2.03	3.17	3.83	5.05	4.09	ns
	–1	0.50	2.45	0.03	0.81	0.32	2.49	1.69	2.64	3.19	4.21	3.41	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-39 **• 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	9.75	0.04	0.97	0.39	9.93	8.22	2.52	2.31	11.99	10.28	ns
	–1	0.50	8.12	0.03	0.81	0.32	8.27	6.85	2.10	1.93	9.99	8.57	ns
8 mA	Std.	0.60	6.96	0.04	0.97	0.39	7.09	5.85	2.84	2.87	9.15	7.91	ns
	–1	0.50	5.80	0.03	0.81	0.32	5.91	4.88	2.37	2.39	7.62	6.59	ns
12 mA	Std.	0.60	5.35	0.04	0.97	0.39	5.45	4.58	3.06	3.23	7.51	6.64	ns
	–1	0.50	4.46	0.03	0.81	0.32	4.54	3.82	2.55	2.69	6.26	5.53	ns
16 mA	Std.	0.60	5.01	0.04	0.97	0.39	5.10	4.30	3.11	3.32	7.16	6.36	ns
	–1	0.50	4.17	0.03	0.81	0.32	4.25	3.58	2.59	2.77	5.97	5.30	ns
24 mA	Std.	0.60	4.67	0.04	0.97	0.39	4.75	4.28	3.16	3.66	6.81	6.34	ns
	–1	0.50	3.89	0.03	0.81	0.32	3.96	3.57	2.64	3.05	5.68	5.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-40 **• 3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.31	0.09	0.94	1.30	0.22	2.35	1.86	2.20	2.45	ns
	–1	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Timing Characteristics

***Table 2-56* • 1.5 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.425 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 m	Std.	0.60	7.79	0.04	1.34	0.39	6.43	7.79	3.19	2.59	8.49	9.85	ns
	–1	0.50	6.49	0.03	1.12	0.32	5.36	6.49	2.66	2.16	7.08	8.21	ns
4 mA	Std.	0.60	4.95	0.04	1.34	0.39	4.61	4.96	3.53	3.19	6.67	7.02	ns
	–1	0.50	4.13	0.03	1.12	0.32	3.85	4.13	2.94	2.66	5.56	5.85	ns
6 mA	Std.	0.60	4.36	0.04	1.34	0.39	4.34	4.36	3.60	3.34	6.40	6.42	ns
	–1	0.50	3.64	0.03	1.12	0.32	3.62	3.64	3.00	2.78	5.33	5.35	ns
8 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
12 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

***Table 2-57* • 1.5 V LVCMOS Low Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.96	0.04	1.34	0.39	12.18	11.70	3.20	2.47	14.24	13.76	ns
	–1	0.50	9.96	0.03	1.12	0.32	10.15	9.75	2.67	2.06	11.86	11.46	ns
4 mA	Std.	0.60	9.51	0.04	1.34	0.39	9.68	8.76	3.54	3.07	11.74	10.82	ns
	–1	0.50	7.92	0.03	1.12	0.32	8.07	7.30	2.95	2.56	9.79	9.02	ns
6 mA	Std.	0.60	8.86	0.04	1.34	0.39	9.03	8.17	3.61	3.22	11.08	10.23	ns
	–1	0.50	7.39	0.03	1.12	0.32	7.52	6.81	3.01	2.68	9.24	8.52	ns
8 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns
12 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

***Table 2-58* • 1.5 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.22	3.24	0.09	1.28	1.86	0.22	3.30	3.20	2.24	2.21	ns
	–1	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-66 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCFPGAIOBx	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-67 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

* *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-68 • **LVPECL**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.76	0.04	1.76	ns
–1	0.50	1.46	0.03	1.46	ns

Notes:

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

Output Register

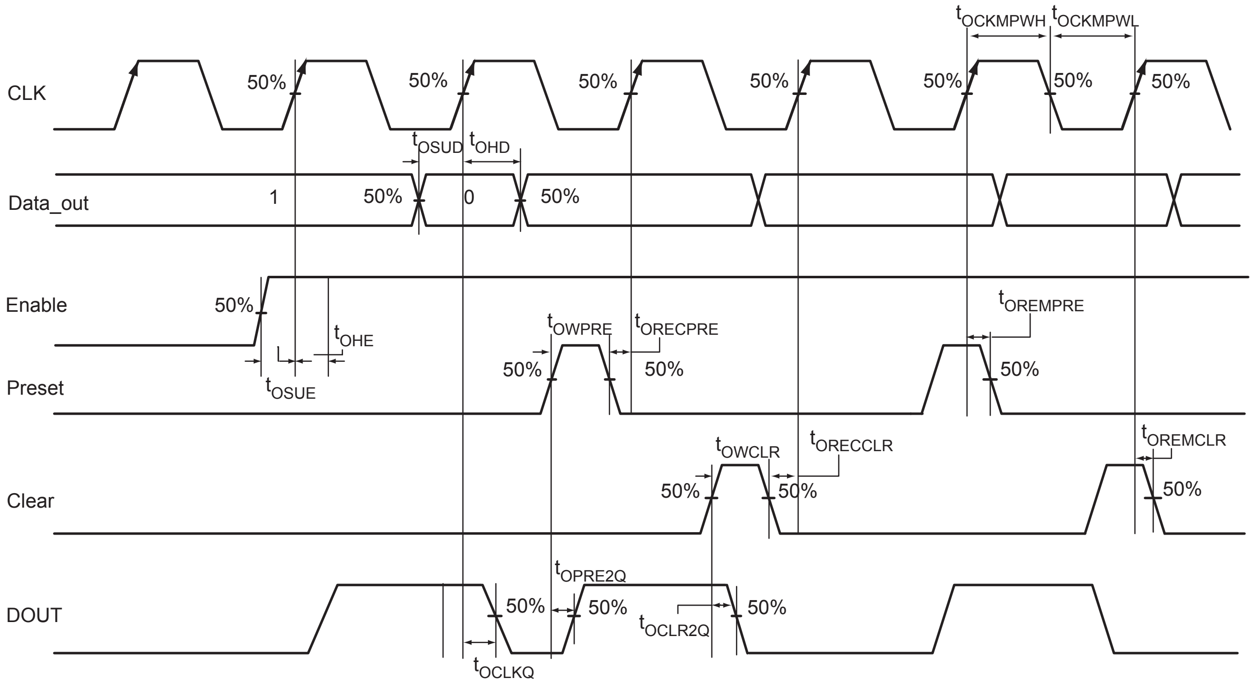


Figure 2-17 **• Output Register Timing Diagram**

Timing Characteristics

Table 2-72 **• Output Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.72	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.38	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.98	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.98	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-98 **• Analog Sigma-Delta DAC (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Sigma-delta DAC power supply current requirements (not including VAREFx)	Input = 0, EN = 1 (operational mode)				
	VCC33SDDx		30	35	µA
	VCC15A		3	5	µA
	Input = Half scale, EN = 1 (operational mode)				
	VCC33SDDx		160	165	µA
	VCC15A		33	35	µA
	Input = Full scale, EN = 1 (operational mode)				
	VCC33SDDx		280	285	µA
	VCC15A		70	75	µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

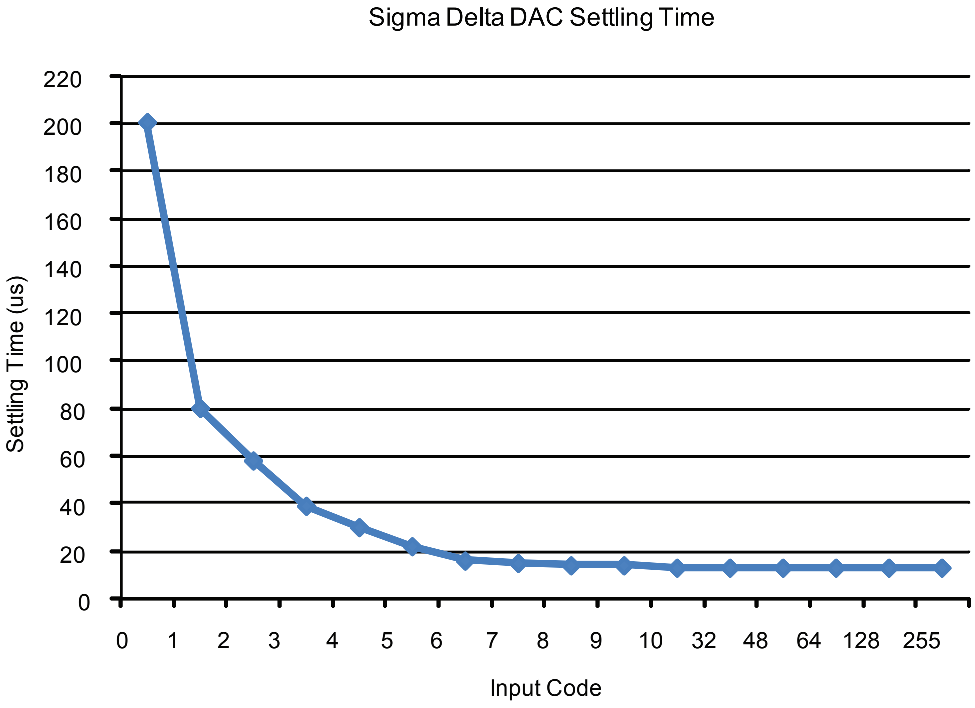


Figure 2-44 **• Sigma-Delta DAC Setting Time**

Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 2-48 on page 2-92.

Table 2-101 **• I^2C Characteristics**
Commercial Case Conditions: T_J = 85ºC, V_{DD} = 1.425 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
V_{IL}	Minimum input low voltage	–	See Table 2-36 on page 2-30	–
	Maximum input low voltage	–	See Table 2-36	–
V_{IH}	Minimum input high voltage	–	See Table 2-36	–
	Maximum input high voltage	–	See Table 2-36	–
V_{OL}	Maximum output voltage low	I_{OL} = 8 mA	See Table 2-36	–
I_{IL}	Input current high	–	See Table 2-36	–
I_{IH}	Input current low	–	See Table 2-36	–
V_{hyst}	Hysteresis of Schmitt trigger inputs	–	See Table 2-33 on page 2-29	V
T_{FALL}	Fall time [2]	VIHmin to VILMax, C_{load} = 400 pF	15.0	ns
		VIHmin to VILMax, C_{load} = 100 pF	4.0	ns
T_{RISE}	Rise time [2]	VILMax to VIHmin, C_{load} = 400pF	19.5	ns
		VILMax to VIHmin, C_{load} = 100pF	5.2	ns
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	8.0	pF
$R_{pull-up}$	Output buffer maximum pull-down Resistance [1]	–	50	Ω
$R_{pull-down}$	Output buffer maximum pull-up Resistance [1]	–	150	Ω
D_{max}	Maximum data rate	Fast mode	400	Kbps
t_{LOW}	Low period of I2C_x_SCL [3]	–	1	pclk cycles
t_{HIGH}	High period of I2C_x_SCL [3]	–	1	pclk cycles
$t_{HD;STA}$	START hold time [3]	–	1	pclk cycles
$t_{SU;STA}$	START setup time [3]	–	1	pclk cycles
$t_{HD;DAT}$	DATA hold time [3]	–	1	pclk cycles
$t_{SU;DAT}$	DATA setup time [3]	–	1	pclk cycles

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
3. *For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I^2C) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide.*

Embedded Design

Microsemi offers FREE SoftConsole Eclipse based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microsemi also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.

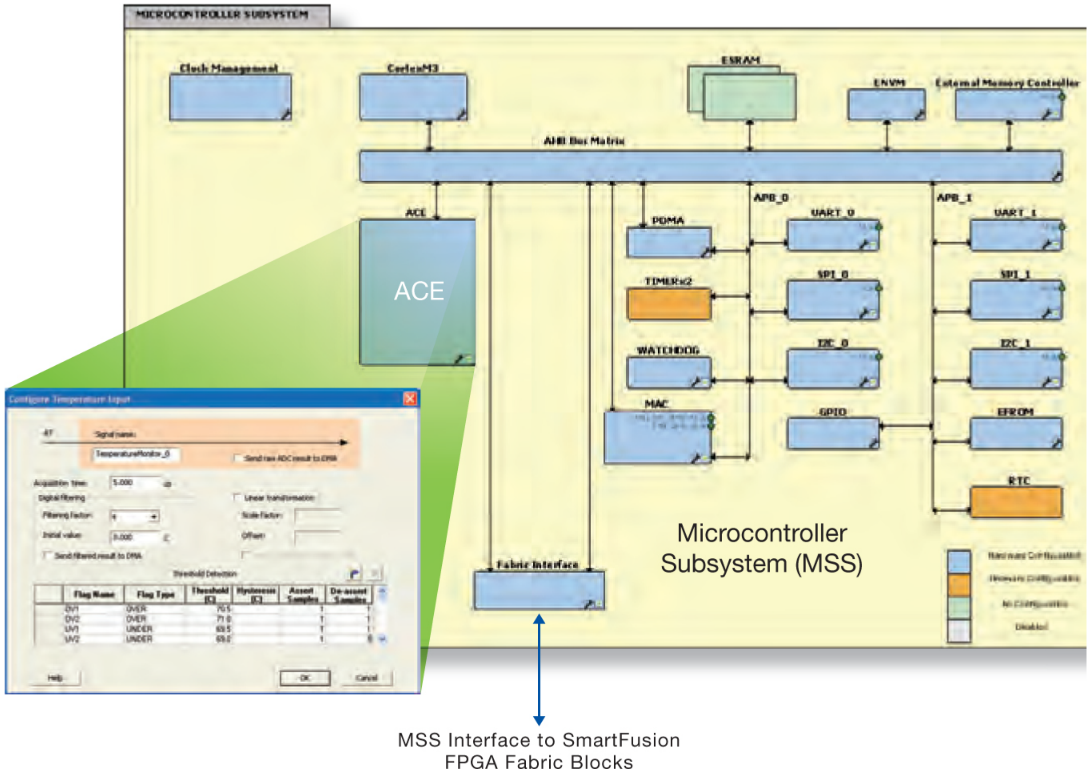
Analog Design

The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, as well as DAC output.

The MSS configurator creates a bridge between the FPGA fabric and embedded designers so device configuration can be easily shared between multiple developers.

The MSS configurator includes the following:

- A simple configurator for the embedded designer to control the MSS peripherals and I/Os
- A method to import and view a hardware configuration from the FPGA flow into the embedded flow containing the memory map
- Automatic generation of drivers for any peripherals or soft IP used in the system configuration
- Comprehensive analog configuration for the programmable analog components
- Creation of a standard MSS block to be used in SmartDesign for connection of FPGA fabric designs and IP



Configure Temperature Input

Signal name: TemperatureMonitor_0

☐ Send raw ADC result to DMA

Acquisition time: 5.000 µs

Digital filtering

Filtering Factor: 4

Initial value: 0.000 C

☐ Send filtered result to DMA

☐ Linear transformation

Scale Factor:

Offset:

Threshold Detection

Flag Name	Flag Type	Threshold (C)	Hysteresis (C)	Assert Samples	De-assert Samples
OV1	OVER	70.5		1	1
OV2	OVER	71.0		1	1
UV1	UNDER	69.5		1	1
UV2	UNDER	69.0		1	[illegible]

Figure 3-2 • **MSS Configurator**

SmartFusion Ecosystem

The Microsemi SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in Figure 3-3.

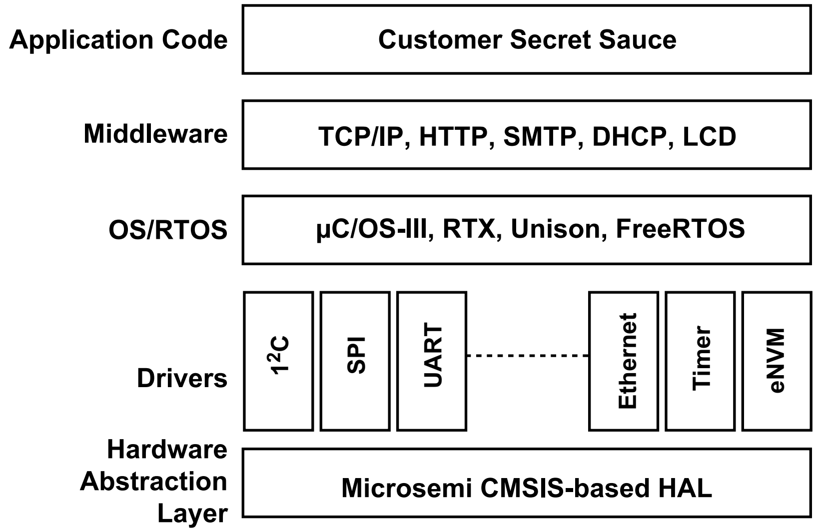


Figure 3-3 • **SmartFusion Ecosystem**

Figure 3-3 shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

ARM

Because an ARM processor was chosen for SmartFusion cSoCs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers* White Paper

4 – SmartFusion Programming

SmartFusion cSoCs have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
    a. A2F060 and A2F500: The FPGA fabric, eNVM, and eFROM
    b. A2F200: Only the FPGA fabric and the eNVM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. Table 4-1 describes the JTAG programming hardware that will program a SmartFusion cSoC and Table 4-2 defines the JTAG pins that provide the interface for the programming hardware.

Table 4-1 **• Supported JTAG Programming Hardware**

Dongle	**Source**	**JTAG**	**SWD**[1]	**SWV**[2]	**Program FPGA**	**Program eFROM**	**Program eNVM**
FlashPro3/4	SoC Products Group	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes

Notes:

1. *SWD = ARM Serial Wire Debug*
2. *SWV = ARM Serial Wire Viewer*
3. *Planned support*

Table 4-2 **• JTAG Pin Descriptions**

Pin Name	**Description**
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

Analog Front-End (AFE)

Name	Type	Description	Associated With	
			ADC/SDD	**SCB**
ABPS0	In	SCB 0 / active bipolar prescaler input 1. See the Active Bipolar Prescaler (ABPS) section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ABPS1	In	SCB 0 / active bipolar prescaler Input 2	ADC0	SCB0
ABPS2	In	SCB 1 / active bipolar prescaler Input 1	ADC0	SCB1
ABPS3	In	SCB 1 / active bipolar prescaler Input 2	ADC0	SCB1
ABPS4	In	SCB 2 / active bipolar prescaler Input 1	ADC1	SCB2
ABPS5	In	SCB 2 / active bipolar prescaler Input 2	ADC1	SCB2
ABPS6	In	SCB 3 / active bipolar prescaler Input 1	ADC1	SCB3
ABPS7	In	SCB 3 / active bipolar prescaler input 2	ADC1	SCB3
ABPS8	In	SCB 4 / active bipolar prescaler input 1	ADC2	SCB4
ABPS9	In	SCB 4 / active bipolar prescaler input 2	ADC2	SCB4
ADC0	In	ADC 0 direct input 0 / FPGA Input. See the "Sigma-Delta Digital-to-Analog Converter (DAC)" section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ADC1	In	ADC 0 direct input 1 / FPGA input	ADC0	SCB0
ADC2	In	ADC 0 direct input 2 / FPGA input	ADC0	SCB1
ADC3	In	ADC 0 direct input 3 / FPGA input	ADC0	SCB1
ADC4	In	ADC 1 direct input 0 / FPGA input	ADC1	SCB2
ADC5	In	ADC 1 direct input 1 / FPGA input	ADC1	SCB2
ADC6	In	ADC 1 direct input 2 / FPGA input	ADC1	SCB3
ADC7	In	ADC 1 direct input 3 / FPGA input	ADC1	SCB3
ADC8	In	ADC 2 direct input 0 / FPGA input	ADC2	SCB4
ADC9	In	ADC 2 direct input 1 / FPGA input	ADC2	SCB4
ADC10	In	ADC 2 direct input 2 / FPGA input	ADC2	N/A
ADC11	In	ADC 2 direct input 3 / FPGA input	ADC2	N/A
CM0	In	SCB 0 / high side of current monitor / comparator Positive input. See the Current Monitor section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
CM1	In	SCB 1 / high side of current monitor / comparator. Positive input.	ADC0	SCB1
CM2	In	SCB 2 / high side of current monitor / comparator. Positive input.	ADC1	SCB2
CM3	In	SCB 3 / high side of current monitor / comparator. Positive input.	ADC1	SCB3
CM4	In	SCB 4 / high side of current monitor / comparator. Positive input.	ADC2	SCB4

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

TQ144	
Pin Number	**A2F060 Function**
1	VCCPLL0
2	VCOMPLA0
3	GNDQ
4	GFA2/IO42PDB5V0
5	GFB2/IO42NDB5V0
6	GFC2/IO41PDB5V0
7	IO41NDB5V0
8	VCC
9	GND
10	VCCFPGAIOB5
11	IO38PDB5V0
12	IO38NDB5V0
13	IO36PDB5V0
14	IO36NDB5V0
15	GND
16	GNDRCOSC
17	VCCRCOSC
18	MSS_RESET_N
19	GPIO_0/IO33RSB4V0
20	GPIO_1/IO32RSB4V0
21	GPIO_2/IO31RSB4V0
22	GPIO_3/IO30RSB4V0
23	GPIO_4/IO29RSB4V0
24	GND
25	VCCMSSIOB4
26	VCC
27	GPIO_5/IO28RSB4V0
28	GPIO_6/IO27RSB4V0
29	GPIO_7/IO26RSB4V0
30	GPIO_8/IO25RSB4V0
31	VCCESRAM
32	GNDSDD0
33	VCC33SDD0
34	VCC15A
35	PCAP
36	NCAP

Pin Number	FG484	
	A2F200 Function	**A2F500 Function**
AA13	NC	ADC10
AA14	NC	ADC9
AA15	NC	GND15ADC2
AA16	MAINXIN	MAINXIN
AA17	MAINXOUT	MAINXOUT
AA18	LPXIN	LPXIN
AA19	LPXOUT	LPXOUT
AA20	NC	NC
AA21	NC	NC
AA22	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
AB1	GND	GND
AB2	GPIO_13/IO36RSB4V0	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO35RSB4V0	GPIO_14/IO44RSB4V0
AB4	GND	GND
AB5	PCAP	PCAP
AB6	NCAP	NCAP
AB7	ABPS3	ABPS3
AB8	ADC3	ADC3
AB9	GND15ADC0	GND15ADC0
AB10	VCC33ADC1	VCC33ADC1
AB11	VAREF1	VAREF1
AB12	TM2	TM2
AB13	CM2	CM2
AB14	ABPS4	ABPS4
AB15	GNDAQ	GNDAQ
AB16	GNDMAINXTAL	GNDMAINXTAL
AB17	GNDLPXTAL	GNDLPXTAL
AB18	VCCLPXTAL	VCCLPXTAL
AB19	VDDBAT	VDDBAT
AB20	PTBASE	PTBASE
AB21	NC	NC
AB22	GND	GND
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*