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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1pq208

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of eNVM blocks used in the design
- The analog block used in the design, including the temperature monitor, current monitor, ABPS, sigma-delta DAC, comparator, low power crystal oscillator, RC oscillator and the main crystal oscillator
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-17 on page 2-18.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate to the eNVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

SoC Mode, Standby Mode, and Time Keeping Mode.

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

SoC Mode

$P_{STAT} = P_{DC1} + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = P_{DC2}$

Time Keeping Mode

$P_{STAT} = P_{DC3}$

Total Dynamic Power Consumption—P_{DYN}

SoC Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{eNVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB} + P_{LPXTAL\text{-}OSC} + P_{MSS}$

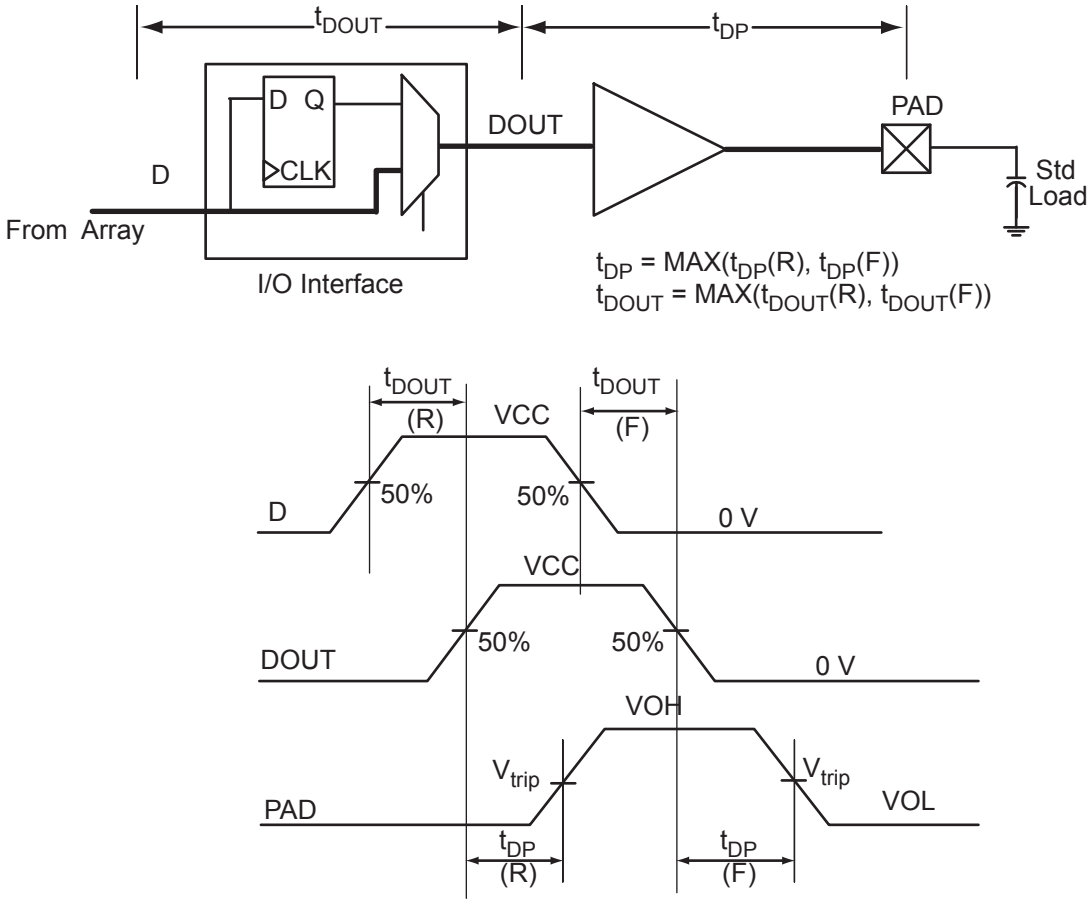


Figure 2-4 • **Output Buffer Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions—Software Default Settings Applicable to FPGA I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}[1]	I_{OH}[1]
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25 * VCCxxxxIOBx	0.75* VCCxxxxIOBx	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

Table 2-20 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions—Software Default Settings Applicable to MSS I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}[1]	I_{OH}[1]
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25* VCCxxxxIOBx	0.75* VCCxxxxIOBx	2	2

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
2.5 V LVCMOS	12 mA	High	35	–	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
1.8 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
1.5 V LVCMOS	12 mA	High	35	–	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
3.3 V PCI	Per PCI spec	High	10	25[1]	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25[1]	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
LVDS	24 mA	High	–	–	0.50	1.53	0.03	1.55	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.50	1.46	0.03	1.46	–	–	–	–	–	–	–	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns
2.5 V LVCMOS	8 mA	High	10	–	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns
1.8 V LVCMOS	4 mA	High	10	–	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns
1.5 V LVCMOS	2 mA	High	10	–	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than 2200 operation hours to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-32* • Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

***Table 2-33* • Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical)
3.3 V LVTTL / LVCMOS / PCI / PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

***Table 2-34* • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (100°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi SoC Products Group recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

***Table 2-69* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-14 on page 2-44 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

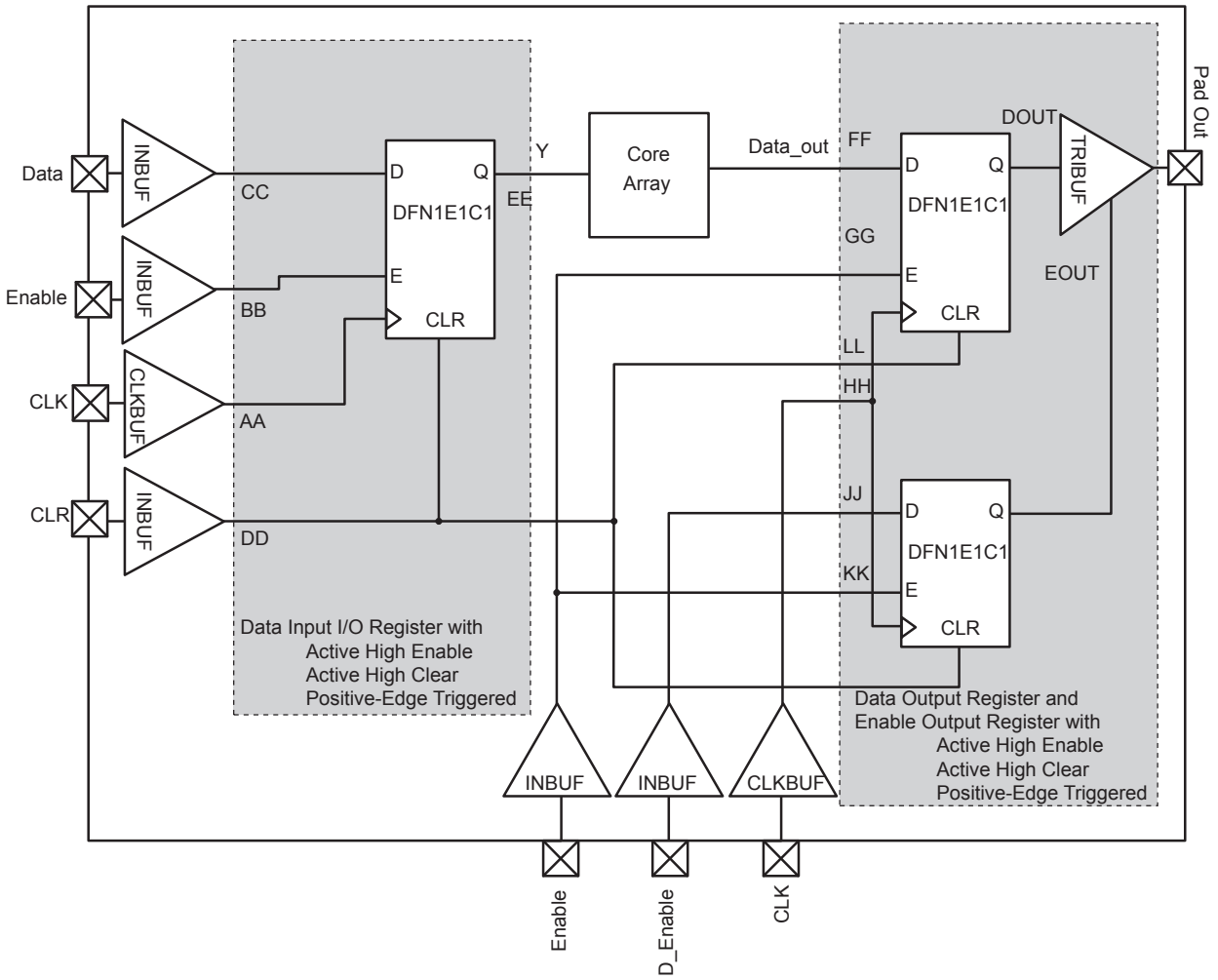


Figure 2-15 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-82 • A2F060 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.75	0.96	0.90	1.15	ns
t_{RCKH}	Input High Delay for Global Clock	0.72	0.98	0.86	1.17	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.31	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

RC Oscillator

The table below describes the electrical characteristics of the RC oscillator.

RC Oscillator Characteristics

Table 2-83 • Electrical Characteristics of the RC Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FRC	Operating frequency			100		MHz
	Accuracy	Temperature: –40°C to 100°C Voltage: 3.3 V ± 5%		1		%
	Output jitter	Period jitter (at 5 K cycles)		100		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles)		100		ps RMS
		Period jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
	Output duty cycle			50		%
IDYNRC	Operating current	3.3 V domain		1		mA
		1.5 V domain		2		mA

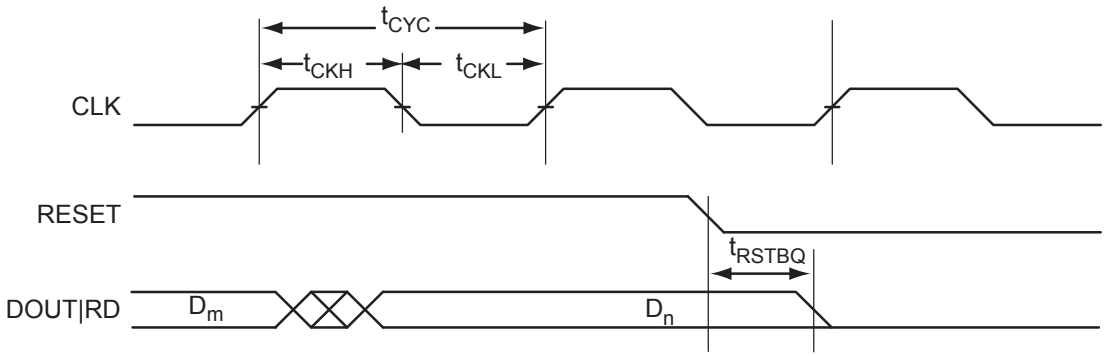


***Figure 2-34* • RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-96 • ABPS Performance Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%

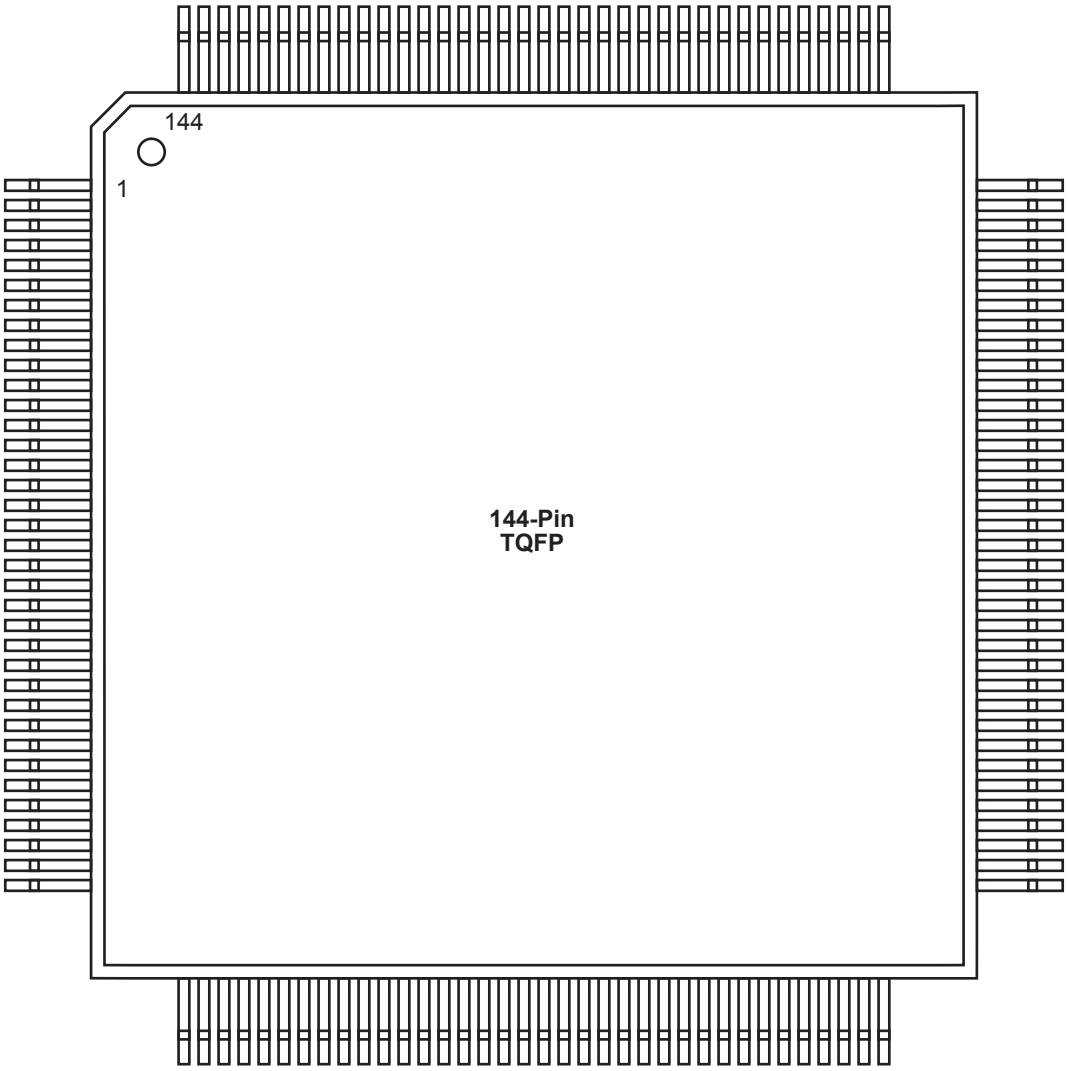
*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the *SmartFusion Programmable Analog User's Guide*.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Pin Assignment Tables

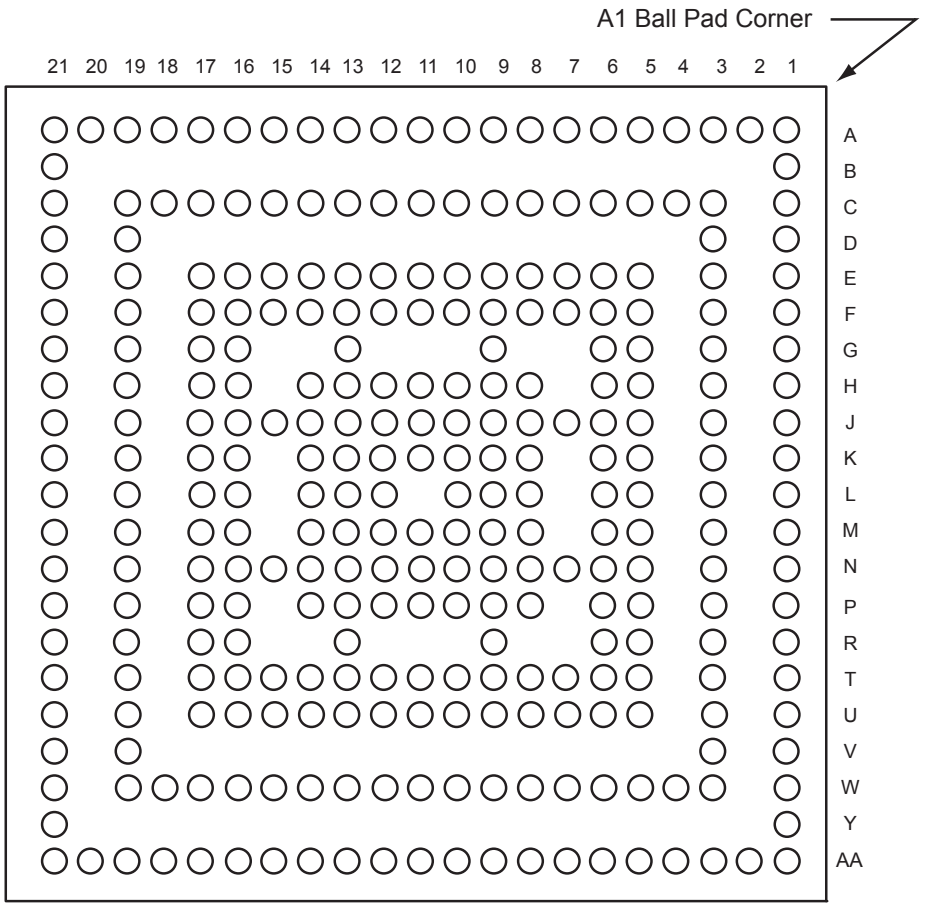
TQ144



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS288



Note: Bottom view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
AA11	ADC9	ADC6	ADC6
AA12	ABPS1	ABPS7	ABPS7
AA13	ADC6	TM2	TM2
AA14	NC	ABPS4	ABPS4
AA15	NC	SDD1	SDD1
AA16	GNDVAREF	GNDVAREF	GNDVAREF
AA17	VAREFOUT	VAREFOUT	VAREFOUT
AA18	PU_N	PU_N	PU_N
AA19	VCC33A	VCC33A	VCC33A
AA20	PTEM	PTEM	PTEM
AA21	GND	GND	GND
B1	GND	GND	GND
B21	IO17PDB0V0	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
C1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
C3	VCOMPLA0	VCOMPLA	VCOMPLA0
C4	VCCPLL0	VCCPLL	VCCPLL0
C5	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C6	EMC_AB[1]/IO04PPB0V0	EMC_AB[1]/IO04PPB0V0	EMC_AB[1]/IO06PPB0V0
C7	GND	GND	GND
C8	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
C9	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
C10	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
C11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C12	EMC_AB[9]/IO08PPB0V0	EMC_AB[9]/IO08PPB0V0	EMC_AB[9]/IO13PPB0V0
C13	EMC_AB[15]/IO11PPB0V0	EMC_AB[15]/IO11PPB0V0	EMC_AB[15]/IO15PPB0V0
C14	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C15	GND	GND	GND
C16	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C17	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C18	NC	NC	VCCPLL1
C19	NC	NC	VCOMPLA1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
M21	TRSTB	TRSTB	TRSTB
N1	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
N3	GND	GND	GND
N5	GPIO_4/IO29RSB4V0	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
N6	GPIO_8/IO25RSB4V0	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
N7	GPIO_9/IO24RSB4V0	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
N8	VCC	VCC	VCC
N9	GND	GND	GND
N10	VCC	VCC	VCC
N11	GND	GND	GND
N12	VCC	VCC	VCC
N13	GND	GND	GND
N14	VCC	VCC	VCC
N15	GND	GND	GND
N16	TCK	TCK	TCK
N17	TDI	TDI	TDI
N19	GNDENVM	GNDENVM	GNDENVM
N21	VCCENVM	VCCENVM	VCCENVM
P1	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
P3	GPIO_7/IO26RSB4V0	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0
P5	GPIO_6/IO27RSB4V0	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
P6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
P8	GND	GND	GND
P9	VCC	VCC	VCC
P10	GND	GND	GND
P11	VCC	VCC	VCC
P12	GND	GND	GND
P13	VCC	VCC	VCC
P14	GND	GND	GND
P16	JTAGSEL	JTAGSEL	JTAGSEL
P17	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
W14	ADC5	CM2	CM2
W15	NC	ABPS5	ABPS5
W16	GNDAQ	GNDAQ	GNDAQ
W17	NC	VCC33SDD1	VCC33SDD1
W18	NC	GNDSDD1	GNDSDD1
W19	PTBASE	PTBASE	PTBASE
W21	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
Y1	VCC33AP	VCC33AP	VCC33AP
Y21	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
156	GNDQ	GNDQ
157	GNDQ	GNDQ
158	VCCFPGAIOB0	VCCFPGAIOB0
159	GBA1/IO19PDB0V0	GBA1/IO23PDB0V0
160	GBA0/IO19NDB0V0	GBA0/IO23NDB0V0
161	VCCFPGAIOB0	VCCFPGAIOB0
162	GND	GND
163	VCC	VCC
164	EMC_AB[25]/IO16PDB0V0	IO21PDB0V0
165	EMC_AB[24]/IO16NDB0V0	IO21NDB0V0
166	EMC_AB[23]/IO15PDB0V0	IO20PDB0V0
167	EMC_AB[22]/IO15NDB0V0	IO20NDB0V0
168	EMC_AB[21]/IO14PDB0V0	IO19PDB0V0
169	EMC_AB[20]/IO14NDB0V0	IO19NDB0V0
170	EMC_AB[19]/IO13PDB0V0	IO18PDB0V0
171	EMC_AB[18]/IO13NDB0V0	IO18NDB0V0
172	EMC_AB[17]/IO12PDB0V0	IO17PDB0V0
173	EMC_AB[16]/IO12NDB0V0	IO17NDB0V0
174	VCCFPGAIOB0	VCCFPGAIOB0
175	GND	GND
176	VCC	VCC
177	EMC_AB[15]/IO11PDB0V0	IO14PDB0V0
178	EMC_AB[14]/IO11NDB0V0	IO14NDB0V0
179	EMC_AB[13]/IO10PDB0V0	IO13PDB0V0
180	EMC_AB[12]/IO10NDB0V0	IO13NDB0V0
181	EMC_AB[11]/IO09PDB0V0	IO12PDB0V0
182	EMC_AB[10]/IO09NDB0V0	IO12NDB0V0
183	EMC_AB[9]/IO08PDB0V0	IO11PDB0V0
184	EMC_AB[8]/IO08NDB0V0	IO11NDB0V0
185	EMC_AB[7]/IO07PDB0V0	IO10PDB0V0
186	EMC_AB[6]/IO07NDB0V0	IO10NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
A1	GND	GND
A2	NC	NC
A3	NC	NC
A4	GND	GND
A5	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
A6	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
A7	GND	GND
A8	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A9	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A10	GND	GND
A11	NC	NC
A12	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
A13	GND	GND
A14	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
A15	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
A16	GND	GND
A17	NC	IO16NDB0V0
A18	NC	IO16PDB0V0
A19	GND	GND
A20	NC	NC
A21	NC	NC
A22	GND	GND
AA1	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
AA2	GPIO_12/IO37RSB4V0	GPIO_12/IO46RSB4V0
AA3	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
AA4	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
AA5	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
AA6	ABPS0	ABPS0
AA7	TM1	TM1
AA8	ADC1	ADC1
AA9	GND15ADC1	GND15ADC1
AA10	GND33ADC1	GND33ADC1
AA11	CM3	CM3
AA12	GNDTM1	GNDTM1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
M21	VPP	VPP
M22	IO32NDB1V0	IO41NDB1V0
N1	GND	GND
N2	NC	IO70PDB5V0
N3	NC	IO70NDB5V0
N4	VCCRCOSC	VCCRCOSC
N5	VCCFPGAIOB5	VCCFPGAIOB5
N6	NC	IO68NDB5V0
N7	VCCFPGAIOB5	VCCFPGAIOB5
N8	GND	GND
N9	VCC	VCC
N10	GND	GND
N11	VCC	VCC
N12	GND	GND
N13	VCC	VCC
N14	GND	GND
N15	VCC	VCC
N16	NC	GND
N17	NC	NC
N18	VCCFPGAIOB1	VCCFPGAIOB1
N19	VCCENVM	VCCENVM
N20	GNDENVM	GNDENVM
N21	NC	NC
N22	GND	GND
P1	NC	IO69NDB5V0
P2	NC	IO69PDB5V0
P3	GNDRCOSC	GNDRCOSC
P4	GND	GND
P5	NC	NC
P6	NC	NC
P7	GND	GND
P8	VCC	VCC
P9	GND	GND
P10	VCC	VCC

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
	The A2F060 device was added to product information tables.	N/A
	The "Product Ordering Codes" table was updated to removed Std. speed and add speed grade 1. Pre-production was removed from the application ordering code category.	VI
	The "SmartFusion cSoC Block Diagram" was revised.	IV
	The "Datasheet Categories" section was updated, referencing the "SmartFusion cSoC Block Diagram" table, which is new.	1-4, IV
	The "VCCI" parameter was renamed to "VCCxxxxIOBx." "Advanced I/Os" were renamed to "FPGA I/Os." Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREFx designates VAREF0, VAREF1, and VAREF2. Modes were renamed as follows: Operating mode was renamed to SoC mode. 32KHz Active mode was renamed to Standby mode. Battery mode was renamed to Time Keeping mode. Table entries have been filled with values as data has become available.	N/A
	Table 2-1 • Absolute Maximum Ratings, Table 2-2 • Analog Maximum Ratings, and Table 2-3 • Recommended Operating Conditions[5,6] were revised extensively.	2-1 through 2-3
	Device names were updated in Table 2-6 • Package Thermal Resistance.	2-7
	Table 2-8 • Power Supplies Configuration was revised extensively.	2-10
	Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings was revised extensively.	2-11
	Removed "Example of Power Calculation."	N/A
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs was revised extensively.	2-12
	Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs was revised extensively.	2-13
	The "Power Calculation Methodology" section was revised.	2-14
	Table 2-83 • Electrical Characteristics of the RC Oscillator was revised extensively.	2-61
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator was revised extensively.	2-62
	The parameter t_{RSTBQ} was changed to T_{C2CWRH} in Table 2-87 • RAM4K9.	2-69
	The 12-bit mode row for integral non-linearity was removed from Table 2-95 • ADC Specifications. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear.	2-81
	Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted.	N/A
	Table 2-99 • Voltage Regulator was revised extensively.	2-87
	The "Serial Peripheral Interface (SPI) Characteristics" section and "Inter-Integrated Circuit (I^2C) Characteristics" section are new.	2-89, 2-91