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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1pqg208

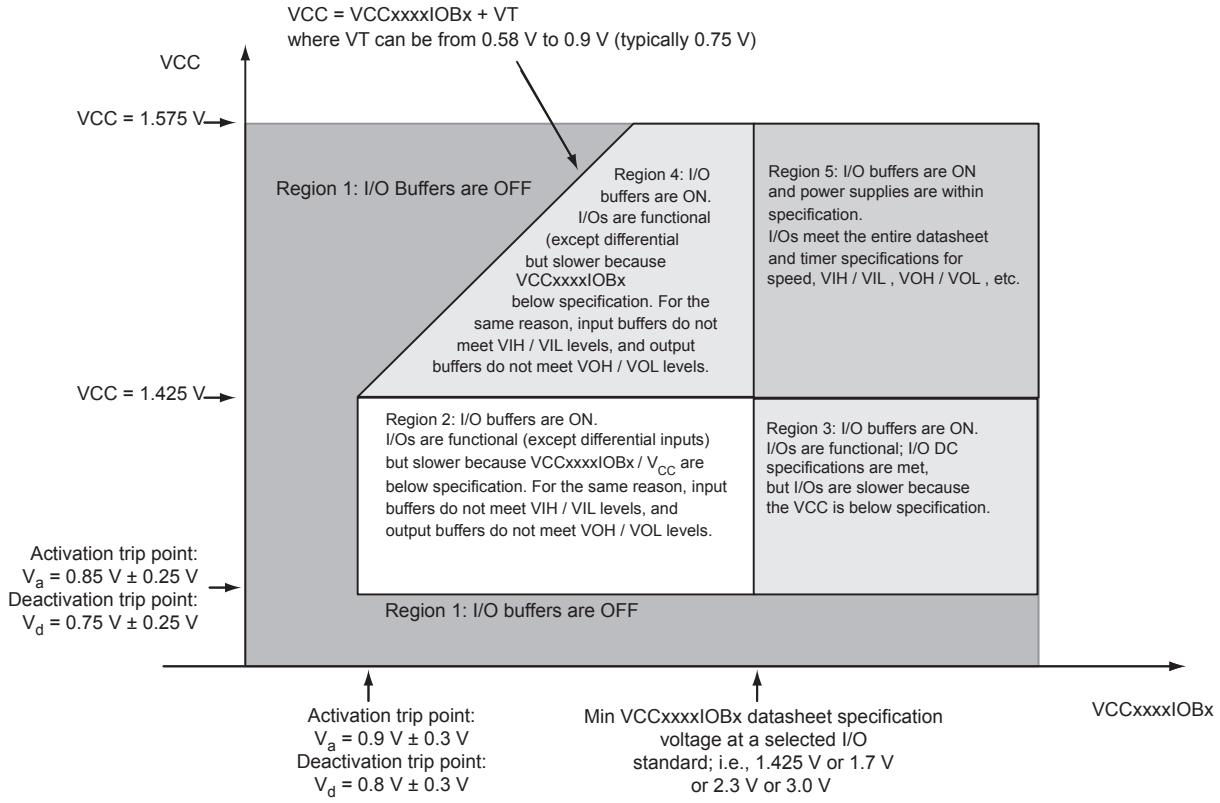

Figure 2-1 • **I/O State as a Function of VCCxxxxIOBx and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 2-6 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
A2F200M3F-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
A2F200M3F-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
A2F200M3F-CS288	26.6	20.2	18.1	7.3	9.4	°C/W
A2F200M3F-PQG208I	38.5	34.6	33.1	0.7	31.6	°C/W

Timing Characteristics

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	7.20	0.04	0.97	0.39	7.34	6.18	2.52	2.46	9.39	8.23	ns
	–1	0.50	6.00	0.03	0.81	0.32	6.11	5.15	2.10	2.05	7.83	6.86	ns
8 mA	Std.	0.60	4.64	0.04	0.97	0.39	4.73	3.84	2.85	3.02	6.79	5.90	ns
	–1	0.50	3.87	0.03	0.81	0.32	3.94	3.20	2.37	2.52	5.65	4.91	ns
12 mA	Std.	0.60	3.37	0.04	0.97	0.39	3.43	2.67	3.07	3.39	5.49	4.73	ns
	–1	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
16 mA	Std.	0.60	3.18	0.04	0.97	0.39	3.24	2.43	3.11	3.48	5.30	4.49	ns
	–1	0.50	2.65	0.03	0.81	0.32	2.70	2.03	2.59	2.90	4.42	3.74	ns
24 mA	Std.	0.60	2.93	0.04	0.97	0.39	2.99	2.03	3.17	3.83	5.05	4.09	ns
	–1	0.50	2.45	0.03	0.81	0.32	2.49	1.69	2.64	3.19	4.21	3.41	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	9.75	0.04	0.97	0.39	9.93	8.22	2.52	2.31	11.99	10.28	ns
	–1	0.50	8.12	0.03	0.81	0.32	8.27	6.85	2.10	1.93	9.99	8.57	ns
8 mA	Std.	0.60	6.96	0.04	0.97	0.39	7.09	5.85	2.84	2.87	9.15	7.91	ns
	–1	0.50	5.80	0.03	0.81	0.32	5.91	4.88	2.37	2.39	7.62	6.59	ns
12 mA	Std.	0.60	5.35	0.04	0.97	0.39	5.45	4.58	3.06	3.23	7.51	6.64	ns
	–1	0.50	4.46	0.03	0.81	0.32	4.54	3.82	2.55	2.69	6.26	5.53	ns
16 mA	Std.	0.60	5.01	0.04	0.97	0.39	5.10	4.30	3.11	3.32	7.16	6.36	ns
	–1	0.50	4.17	0.03	0.81	0.32	4.25	3.58	2.59	2.77	5.97	5.30	ns
24 mA	Std.	0.60	4.67	0.04	0.97	0.39	4.75	4.28	3.16	3.66	6.81	6.34	ns
	–1	0.50	3.89	0.03	0.81	0.32	3.96	3.57	2.64	3.05	5.68	5.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-40 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.31	0.09	0.94	1.30	0.22	2.35	1.86	2.20	2.45	ns
	–1	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

DDR Module Specifications

Input DDR Module

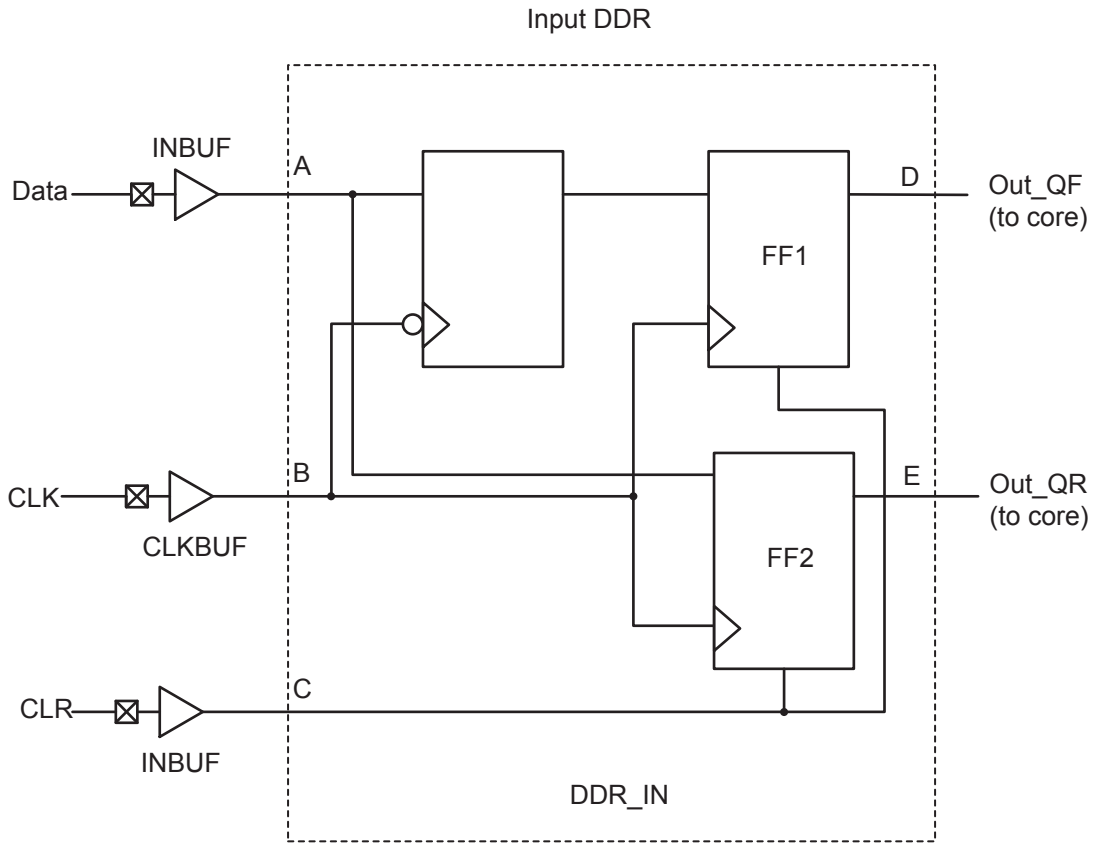

Figure 2-19 • **Input DDR Timing Model**

Table 2-74 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

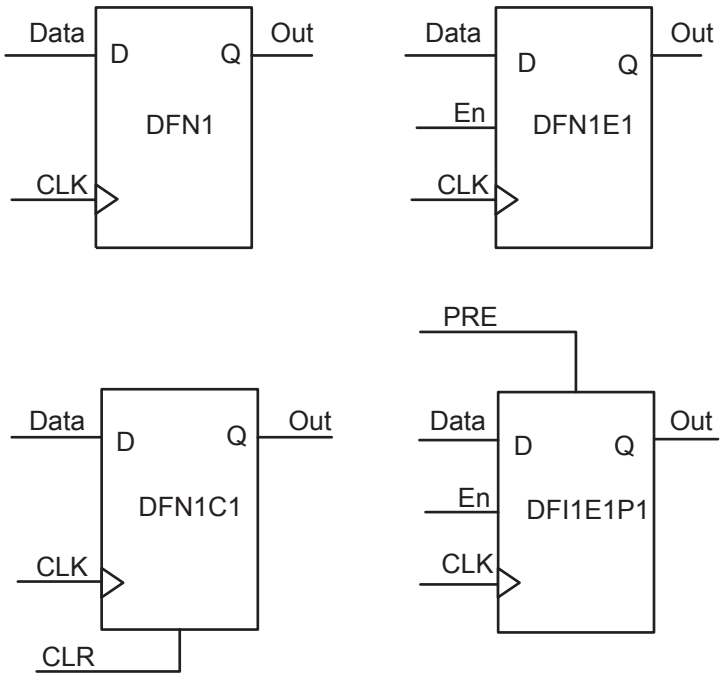

Figure 2-25 • Sample of Sequential Cells

Global Resource Characteristics

A2F200 Clock Tree Topology

Clock delays are device-specific. Figure 2-27 is an example of a global tree used for clock routing. The global tree presented in Figure 2-27 is driven by a CCC located on the west side of the A2F200 device. It is used to drive all D-flip-flops in the device.

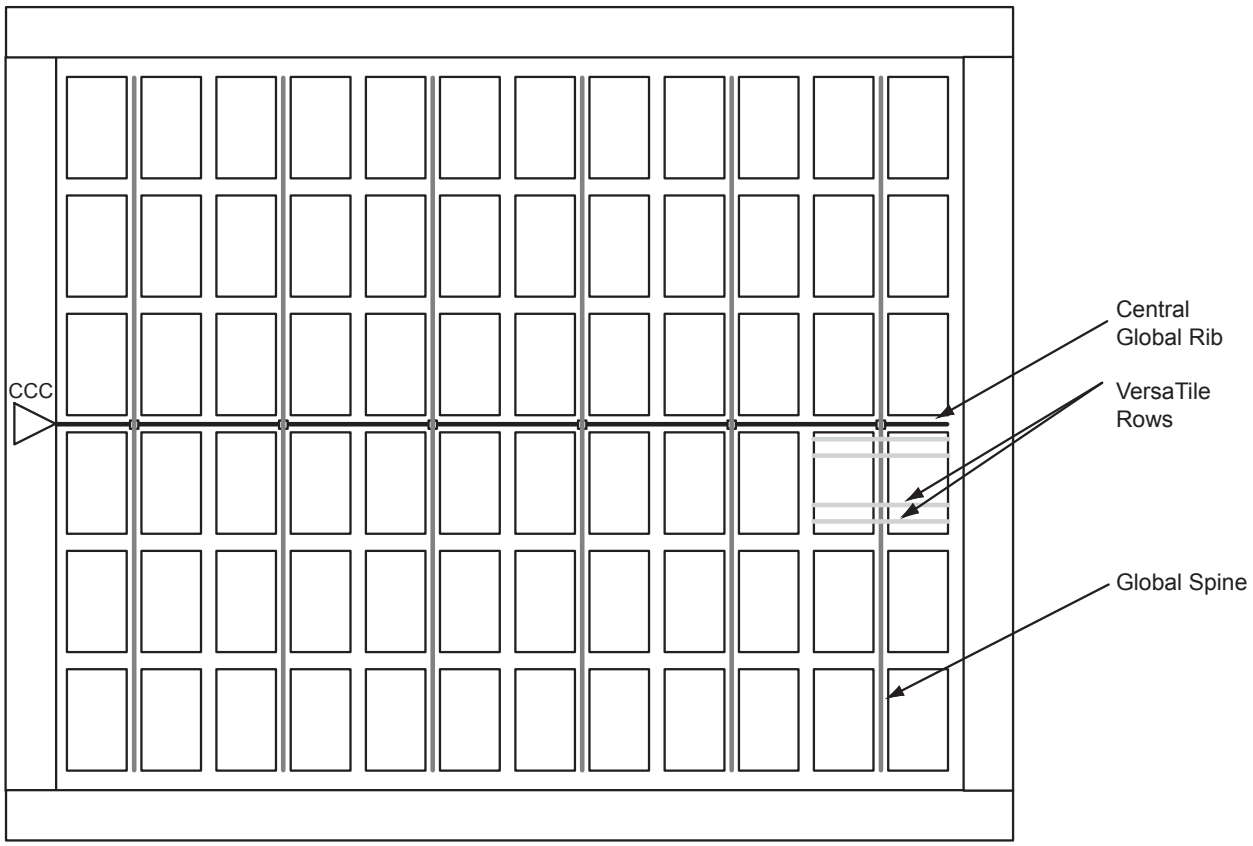

Figure 2-27 • **Example of Global Tree Use in an A2F200 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-63. Table 2-80 through Table 2-82 on page 2-61 present minimum and maximum global clock delays for the SmartFusion cSoCs. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Waveforms

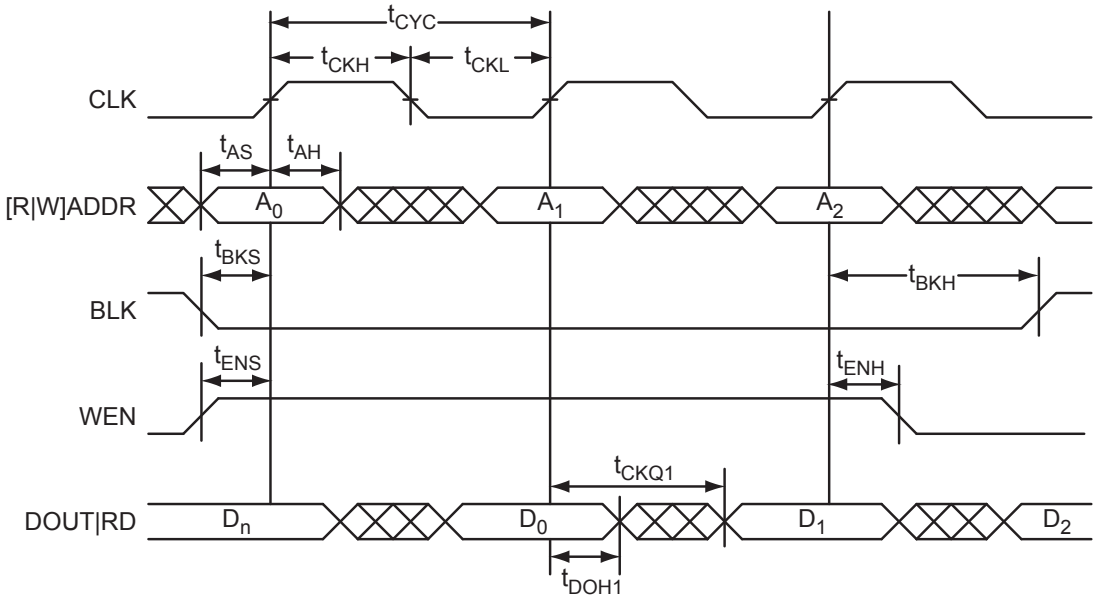

Figure 2-30 • **RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18**.

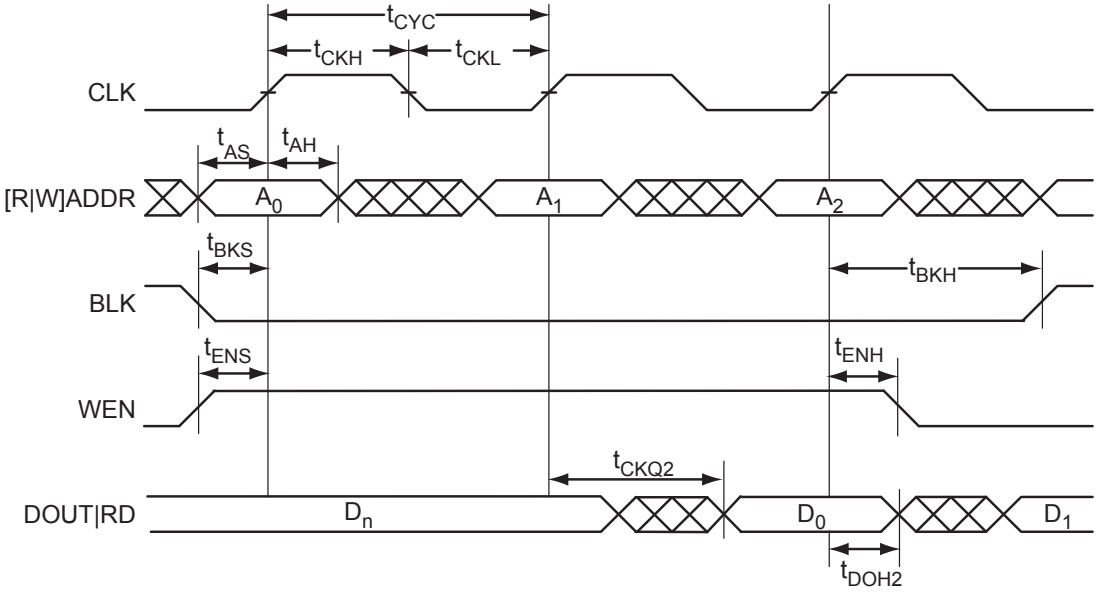

Figure 2-31 • **RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18.**

Embedded Nonvolatile Memory Block (eNVM)

Electrical Characteristics

Table 2-90 describes the eNVM maximum performance.

***Table 2-90* • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V**

Parameter	Description	A2F060		A2F200		A2F500		Units
		–1	Std.	–1	Std.	–1	Std.	
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 5 cycles (5:1:1:1*)	50	50	50	50	50	50	MHz
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 6 cycles (6:1:1:1*)	100	80	100	80	100	80	MHz

*Note: *6:1:1:1 indicates 6 cycles for the first access and 1 each for the next three accesses. 5:1:1:1 indicates 5 cycles for the first access and 1 each for the next three accesses.*

*Note: *Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%.*

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-91 describes the eFROM maximum performance

***Table 2-91* • FlashROM Access Time, Worse Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V**

Parameter	Description	–1	Std.	Units
t_{CK2Q}	Clock to out per configuration*	28.68	32.98	ns
F_{max}	Maximum Clock frequency	15.00	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-19 for more details.

Timing Characteristics

***Table 2-92* • JTAG 1532**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.67	0.77	ns
t_{DIHD}	Test Data Input Hold Time	1.33	1.53	ns
t_{TMSSU}	Test Mode Select Setup Time	0.67	0.77	ns
t_{TMDHD}	Test Mode Select Hold Time	1.33	1.53	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	9.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Comparator

Unless otherwise specified, performance is specified at 25°C with nominal power supply voltages.

***Table 2-97* • Comparator Performance Specifications**

Specification	Test Conditions		Min.	Typ.	Max.	Units
Input voltage range	Minimum			0		V
	Maximum			2.56		V
Input offset voltage	HYS[1:0] = 00 (no hysteresis)			±1	±3	mV
Input bias current	Comparator 1, 3, 5, 7, 9 (measured at 2.56 V)			40	100	nA
	Comparator 0, 2, 4, 6, 8 (measured at 2.56 V)			150	300	nA
Input resistance			10			MΩ
Power supply rejection ratio	DC (0 – 10 KHz)		50	60		dB
Propagation delay	100 mV overdrive					
	HYS[1:0] = 00					
	(no hysteresis)			15	18	ns
	100 mV overdrive					
	HYS[1:0] = 10					
	(with hysteresis)			25	30	ns
Hysteresis (± refers to rising and falling threshold shifts, respectively)	HYS[1:0] = 00	Typical (25°C)	0	0	±5	mV
		Across all corners (–40ºC to +100ºC)	0		±5	mV
	HYS[1:0] = 01	Typical (25°C)	±3	± 16	±30	mV
		Across all corners (–40ºC to +100ºC)	0		±36	mV
	HYS[1:0] = 10	Typical (25°C)	±19	± 31	±48	mV
		Across all corners (–40ºC to +100ºC)	±12		±54	mV
	HYS[1:0] = 11	Typical (25°C)	±80	± 105	±190	mV
		Across all corners (–40ºC to +100ºC)	±80		±194	mV
Comparator current requirements (per comparator)	VCC33A = 3.3 V (operational mode); COMP_EN = 1					
	VCC33A			150	165	µA
	VCC33AP			140	165	µA
	VCC15A			1	3	µA

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-47 on page 2-90.

***Table 2-100* • SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp1	SPI_x_CLK minimum period				
	SPI_x_CLK = PCLK/2	20	NA	20	ns
	SPI_x_CLK = PCLK/4	40	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [1]	4.7	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [1]	3.4	3.4	3.4	ns

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

User I/O Naming Conventions

The naming convention used for each FPGA user I/O is Gmn/IOuxwByVz, where:

Gmn is only used for I/Os that also have CCC access—i.e., global pins. Refer to the "Global I/O Naming Conventions" section on page 5-6.

u = I/O pair number in bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.

x = P (positive) or N (negative) or S (single-ended) or R (regular, single-ended).

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential Pairs (D), adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number starting at 0 from northwest I/O bank and incrementing clockwise.

V = Reference voltage

z = VREF mini bank number.

The FPGA user I/O pin functions as an input, output, tristate or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are disabled by Libero SoC software and include a weak pull-up resistor. During power-up, the used I/O pins are tristated with no pull-up or pull-down resistors until I/O enable (there is a delay after voltage stabilizes, and different I/O banks power up sequentially to avoid a surge of ICCI).

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Some of these pins are also multiplexed with integrated peripherals in the MSS (Ethernet MAC and external memory controller).

All unused MSS I/Os are tristated by default (with output buffer disabled). However, you can configure it as weak pull-up or pull-down by using Libero SoC I/O attributor window. The Schmitt trigger is disabled. Essentially, I/Os have the reset values as defined in Table 19-25 IOMUX_n_CR, in the *SmartFusion Microcontroller Subsystem User's Guide*.

By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to "Specifying I/O States During Programming" on page 1-3. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration. For more information, see the SmartFusion FPGA User I/Os section in the *SmartFusion FPGA Fabric User's Guide*.

TQ144	
Pin Number	**A2F060 Function**
73	VCC33A
74	PTEM
75	PTBASE
76	SPI_0_DO/GPIO_16
77	SPI_0_DI/GPIO_17
78	SPI_0_CLK/GPIO_18
79	SPI_0_SS/GPIO_19
80	UART_0_RXD/GPIO_21
81	UART_0_TXD/GPIO_20
82	UART_1_RXD/GPIO_29
83	UART_1_TXD/GPIO_28
84	VCC
85	VCCMSSIOB2
86	GND
87	I2C_1_SDA/GPIO_30
88	I2C_1_SCL/GPIO_31
89	I2C_0_SDA/GPIO_22
90	I2C_0_SCL/GPIO_23
91	GNDENVM
92	VCCENVM
93	JTAGSEL
94	TCK
95	TDI
96	TMS
97	TDO
98	TRSTB
99	VJTAG
100	VDDBAT
101	VCCLPXTAL
102	LPXOUT
103	LPXIN
104	GNDLPXTAL
105	GNDMAINXTAL
106	MAINXOUT
107	MAINXIN
108	VCCMAINXTAL

Pin Number	PQ208	
	A2F200	A2F500
125	TMS	TMS
126	TDO	TDO
127	TRSTB	TRSTB
128	VJTAG	VJTAG
129	VDDBAT	VDDBAT
130	VCCLPXTAL	VCCLPXTAL
131	LPXOUT	LPXOUT
132	LPXIN	LPXIN
133	GNDLPXTAL	GNDLPXTAL
134	GNDMAINXTAL	GNDMAINXTAL
135	MAINXOUT	MAINXOUT
136	MAINXIN	MAINXIN
137	VCCMAINXTAL	VCCMAINXTAL
138	GND	GND
139	VCC	VCC
140	VPP	VPP
141	VCCFPGAIOB1	VCCFPGAIOB1
142	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
143	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
144	GDC0/IO29NSB1V0	GDC0/IO38NSB1V0
145	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
146	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
147	VCCFPGAIOB1	VCCFPGAIOB1
148	GND	GND
149	VCC	VCC
150	IO25NDB1V0	IO30NDB1V0
151	GCC2/IO25PDB1V0	GBC2/IO30PDB1V0
152	IO23NDB1V0	IO28NDB1V0
153	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
154	GBC2/IO21PSB1V0	GBB2/IO27NDB1V0
155	GBA2/IO20PSB1V0	GBA2/IO27PDB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
156	GNDQ	GNDQ
157	GNDQ	GNDQ
158	VCCFPGAIOB0	VCCFPGAIOB0
159	GBA1/IO19PDB0V0	GBA1/IO23PDB0V0
160	GBA0/IO19NDB0V0	GBA0/IO23NDB0V0
161	VCCFPGAIOB0	VCCFPGAIOB0
162	GND	GND
163	VCC	VCC
164	EMC_AB[25]/IO16PDB0V0	IO21PDB0V0
165	EMC_AB[24]/IO16NDB0V0	IO21NDB0V0
166	EMC_AB[23]/IO15PDB0V0	IO20PDB0V0
167	EMC_AB[22]/IO15NDB0V0	IO20NDB0V0
168	EMC_AB[21]/IO14PDB0V0	IO19PDB0V0
169	EMC_AB[20]/IO14NDB0V0	IO19NDB0V0
170	EMC_AB[19]/IO13PDB0V0	IO18PDB0V0
171	EMC_AB[18]/IO13NDB0V0	IO18NDB0V0
172	EMC_AB[17]/IO12PDB0V0	IO17PDB0V0
173	EMC_AB[16]/IO12NDB0V0	IO17NDB0V0
174	VCCFPGAIOB0	VCCFPGAIOB0
175	GND	GND
176	VCC	VCC
177	EMC_AB[15]/IO11PDB0V0	IO14PDB0V0
178	EMC_AB[14]/IO11NDB0V0	IO14NDB0V0
179	EMC_AB[13]/IO10PDB0V0	IO13PDB0V0
180	EMC_AB[12]/IO10NDB0V0	IO13NDB0V0
181	EMC_AB[11]/IO09PDB0V0	IO12PDB0V0
182	EMC_AB[10]/IO09NDB0V0	IO12NDB0V0
183	EMC_AB[9]/IO08PDB0V0	IO11PDB0V0
184	EMC_AB[8]/IO08NDB0V0	IO11NDB0V0
185	EMC_AB[7]/IO07PDB0V0	IO10PDB0V0
186	EMC_AB[6]/IO07NDB0V0	IO10NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
K12	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
K13	GND	GND	GND
K14	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
K15	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
K16	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
L1	GND	GND	GND
L2	GPIO_2/IO31RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
L3	GPIO_3/IO30RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
L4	GPIO_4/IO29RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
L5	GPIO_9/IO24RSB4V0	MAC_CLK	MAC_CLK
L6	GND	GND	GND
L7	VCC	VCC	VCC
L8	GND	GND	GND
L9	VCC	VCC	VCC
L10	GND	GND	GND
L11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
L12	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
L13	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
L14	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
L15	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
L16	GND	GND	GND
M1	GPIO_5/IO28RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
M2	GPIO_6/IO27RSB4V0	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
M3	GPIO_7/IO26RSB4V0	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
M4	GND	GND	GND
M5	NC	ADC3	ADC3
M6	NC	GND15ADC0	GND15ADC0
M7	GND33ADC0	GND33ADC1	GND33ADC1
M8	GND33ADC0	GND33ADC1	GND33ADC1
M9	ADC7	ADC4	ADC4
M10	GNDTM0	GNDTM1	GNDTM1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
Y15	NC	VCC15ADC2
Y16	VCCMAINXTAL	VCCMAINXTAL
Y17	SDD1	SDD1
Y18	PTEM	PTEM
Y19	VCC33A	VCC33A
Y20	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
Y21	VCCMSSIOB2	VCCMSSIOB2
Y22	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (continued)	Corrected the Start-up time unit from "ms" to "µs" in Table 2-99 • Voltage Regulator (SAR 39395).	2-87
	Added the "References" section for "SmartFusion Development Tools" (SAR 43460).	3-1
	Updated the "References" section for Programming (SAR 43304). Added the "Application Notes on IAP Programming Technique" section (SAR 43458).	4-9
	A note was added to the "Supply Pins" table, referring to the *SmartFusion cSoC Board Design Guidelines* application note for details on VCCPLLx capacitor recommendations (SAR 42183).	5-1
	In the "Supply Pins" section, the VPP capacitor value section has been modified to: "For proper programming, 0.01µF, and 0.1µF to 1µF capacitors, (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible." (SAR 43569).	5-1
	In the "User-Defined Supply Pins" section, added description 'These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices.' for GPIO_x (SAR 28595).	5-5
	Updated the MAINXIN and MAINXOUT pin descriptions in the "Special Function Pins" section to read "If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating." (SAR 42807).	5-8
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 9 (September 2012)	The number of signal conditioning blocks (SCBs) for A2F500 in the "SmartFusion cSoC Family Product Table" was corrected to 4. Previously it had incorrectly been listed as 2 (SAR 39536).	II
	The "Product Ordering Codes" section was revised to clarify that only one eNVM size for each device is currently available (SAR 40333).	VI
	Information pertaining to analog I/Os was added to the "Specifying I/O States During Programming" section on page 1-3 (SAR 34836).	1-3
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34757).	2-27
	Maximum values for VIL and VIH were corrected in LVPECL Table 2-66 • Minimum and Maximum DC Input and Output Levels (SAR 37695).	2-43
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 29270).	2-59
	The temperature range for accuracy in Table 2-83 • Electrical Characteristics of the RC Oscillator was changed from "0°C to 85°C" to "–40°C to 100°C" (SAR 33670). The units for jitter were changed from ps to ps RMS (SAR 34270).	2-61
	In Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator, the output jitter for the 10 MHz crystal was corrected from 50 ps RMS to 1 ns RS (SAR 32939). Values for the startup time of VILXTAL were added (SAR 25248).	2-62
	In Table 2-85 • Electrical Characteristics of the Low Power Oscillator, output jitter was changed from 50 ps RMS to 30 ps RMS (SAR 32939). A value for ISTBXTAL standby current was added (SAR 25249). Startup time for a test load of 30 pF was added (SAR 27436).	2-62

Revision	Changes	Page
Revision 9 (continued)	The following note was added to Table 2-86 • SmartFusion CCC/PLL Specification in regard to delay increments in programmable delay blocks (SAR 34816): "When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information."	2-63
	Figure 2-36 • FIFO Read and Figure 2-37 • FIFO Write have been added (SAR 34851).	2-72
	Information regarding the MSS resetting itself after IAP of the FPGA fabric was added to the "Reprogramming the FPGA Fabric Using the Cortex-M3" section (SAR 37970).	4-8
	Instructions for unused VCC33ADCx pins were revised in "Supply Pins" (SAR 41137).	5-1
	Libero IDE was changed to Libero SoC throughout the document (SAR 40264).	N/A
Revision 8 (March 2012)	In the "Analog Front-End (AFE)" section, the resolution for the first-order sigma delta DAC was corrected from 12-bit to "8-bit, 16-bit, or 24-bit." The same correction was made in the "SmartFusion cSoC Family Product Table" (SAR 36541).	I, II
	The "SmartFusion cSoC Family Product Table" was revised to break out the features by package as well as device. The table now indicates that only one SPI is available for the PQ208 package in A2F200 and A2F500, and in the TQ144 package for A2F060 (SAR 33477). The EMC address bus size has been corrected to 26 bits (SAR 35664).	II
	The "SmartFusion cSoC Device Status" table was revised to change the CS288 package for A2F200 and A2F500 from preliminary to production status (SAR 37811).	III
	TQ144 package information for A2F060 was added to the "Package I/Os: MSS + FPGA I/Os" table, "SmartFusion cSoC Device Status" table, "Product Ordering Codes", and "Temperature Grade Offerings" table (SAR 36246).	III, VI
	Table 1 • SmartFusion cSoC Package Sizes Dimensions is new (SAR 31178).	III
	The Halogen-Free Packaging code (H) was removed from the "Product Ordering Codes" table (SAR 34017).	VI
	The "Specifying I/O States During Programming" section is new (SAR 34836).	1-3
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—P_{CLOCK}" section, was corrected to the "Device Architecture" chapter in the *SmartFusion FPGA Fabric User's Guide* (SAR 34742).	2-15
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34891).	2-30, 2-24
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34799): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-32
	In the SRAM "Timing Characteristics" tables, reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34874).	2-69
	The note for Table 2-93 • Current Monitor Performance Specification was modified to include the statement that the restriction on the TM pad being no greater than 10 mV above the CM pad.is applicable only if current monitor is used (SAR 26373).	2-78
	The unit "FR" in Table 2-96 • ABPS Performance Specifications and Table 2-98 • Analog Sigma-Delta DAC, used to designate full-scale error, was changed to "FS" and clarified with a table note (SAR 35342).	2-82, 2-85

Revision	Changes	Page
Revision 3 (continued)	Two notes were added to the "Supply Pins" table (SAR 27109): 1. *The following supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* 2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	5-1
	The descriptions for the "VCC33N", "NCAP", and "PCAP" pins were revised to include information on what to do if analog SCB features and SDDs are not used (SAR 26744).	5-2, 5-9, 5-9
	Information was added to the "User Pins" table regarding tristating of used and unused GPIO pins. The IO portion of the table was revised to state that unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor (SAR 26890). Information was added regarding behavior of used I/O pins during power-up.	5-6
	The type for "EMC_RW_N" was changed from In/out to Out (SAR 25113).	5-12
	A note was added to the "Analog Front-End (AFE)" table stating that unused analog inputs should be grounded (SAR 26744).	5-14
	The "TQ144" section is new, with pin tables for A2F200 and A2F500 (SAR 27044).	5-18
	The "FG256" pin table was replaced and now includes "Handling When Unused" information (SAR 27709).	5-42
Revision 2 (May 2010)	Embedded nonvolatile flash memory (eNVM) was changed from "64 to 512 Kbytes" to "128 to 512 Kbytes" in the "Microcontroller Subsystem (MSS)" section and "SmartFusion cSoC Family Product Table" (SAR 26005).	I, II
	The main oscillator range of values was changed to "32 KHz to 20 MHz" in the "Microcontroller Subsystem (MSS)" section and the "SmartFusion cSoC Family Product Table" (SAR 24906).	I, II
	The value for t_{PD} was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the "Analog Front-End (AFE)" section (SAR 26005).	I
	The number of PLLs for A2F200 was changed from 2 to 1 in the "SmartFusion cSoC Family Product Table" (SAR 25093).	II
	Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the "Package I/Os: MSS + FPGA I/Os" table. The Max. column was removed from the table (SAR 26005).	III
	The Speed Grade section of the "Product Ordering Codes" table was revised (SAR 25257).	VI
Revision 1 (March 2010)	The "Product Ordering Codes" table was revised to add "blank" as an option for lead-free packaging and application (junction temperature range).	VI
	Table 2-3 • Recommended Operating Conditions[5,6] was revised. Ta (ambient temperature) was replaced with T_J (junction temperature).	2-3
	PDC5 was deleted from Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs.	2-13
	The formulas in the footnotes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised.	2-27
	The values for input biased current were revised in Table 2-93 • Current Monitor Performance Specification.	2-78
Revision 0 (March 2010)	The "Analog Front-End (AFE)" section was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps.	I

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion cSoC Device Status" table on page III, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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