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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

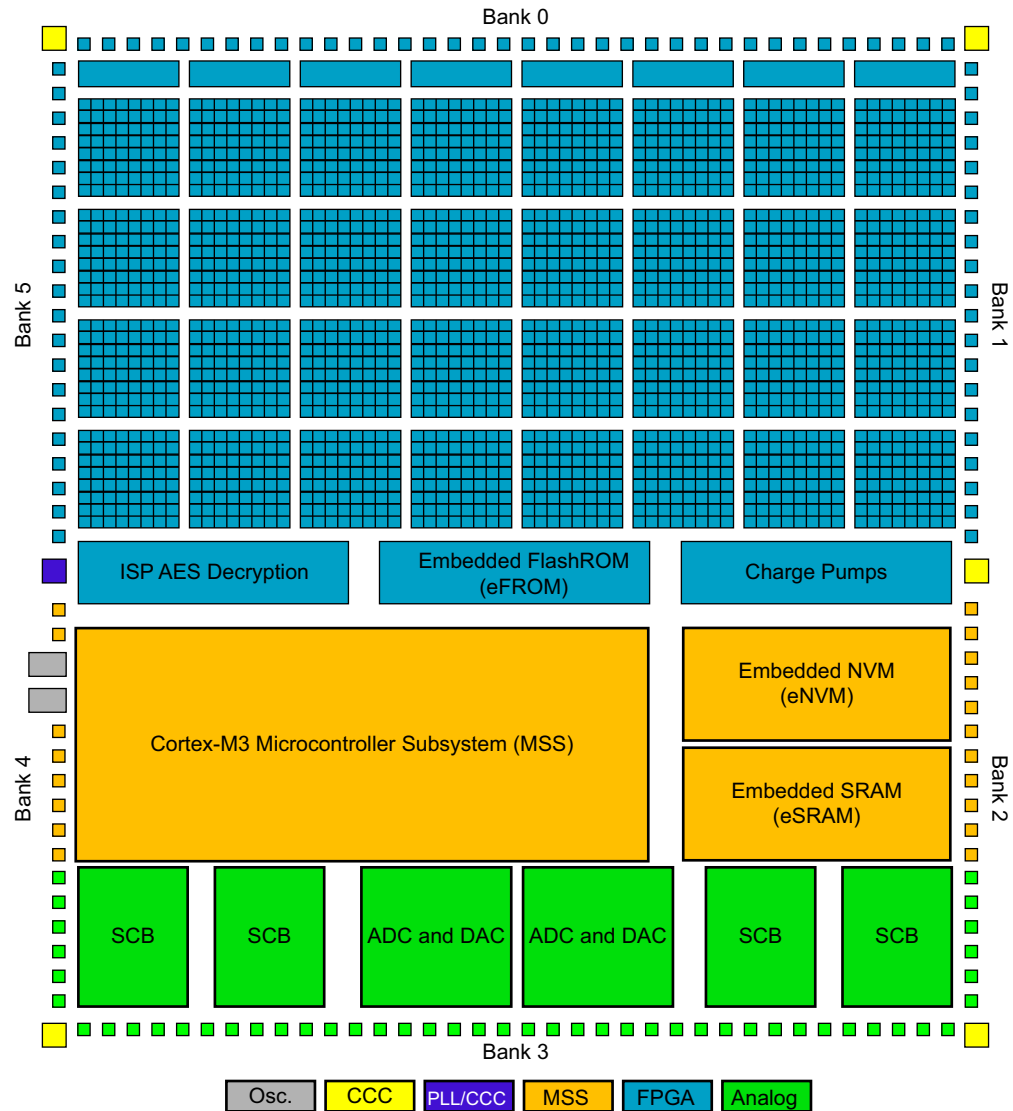
What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	Ethernet, I ² C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1pqq208i

SmartFusion cSoC System Architecture



Note: Architecture for A2F200

Table 2-30 • I/O Short Currents I_{OSH}/I_{OSL}
 Applicable to FPGA I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: * $T_J = 85^\circ\text{C}$.

Table 2-31 • I/O Short Currents I_{OSH}/I_{OSL}
 Applicable to MSS I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	54	51
2.5 V LVCMOS	8 mA	37	32
1.8 V LVCMOS	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Note: * $T_J = 85^\circ\text{C}$

Timing Characteristics

Table 2-38 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxxIOBx = 3.0 V

Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	7.20	0.04	0.97	0.39	7.34	6.18	2.52	2.46	9.39	8.23	ns
	–1	0.50	6.00	0.03	0.81	0.32	6.11	5.15	2.10	2.05	7.83	6.86	ns
8 mA	Std.	0.60	4.64	0.04	0.97	0.39	4.73	3.84	2.85	3.02	6.79	5.90	ns
	–1	0.50	3.87	0.03	0.81	0.32	3.94	3.20	2.37	2.52	5.65	4.91	ns
12 mA	Std.	0.60	3.37	0.04	0.97	0.39	3.43	2.67	3.07	3.39	5.49	4.73	ns
	–1	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
16 mA	Std.	0.60	3.18	0.04	0.97	0.39	3.24	2.43	3.11	3.48	5.30	4.49	ns
	–1	0.50	2.65	0.03	0.81	0.32	2.70	2.03	2.59	2.90	4.42	3.74	ns
24 mA	Std.	0.60	2.93	0.04	0.97	0.39	2.99	2.03	3.17	3.83	5.05	4.09	ns
	–1	0.50	2.45	0.03	0.81	0.32	2.49	1.69	2.64	3.19	4.21	3.41	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-39 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxxIOBx = 3.0 V

Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	9.75	0.04	0.97	0.39	9.93	8.22	2.52	2.31	11.99	10.28	ns
	–1	0.50	8.12	0.03	0.81	0.32	8.27	6.85	2.10	1.93	9.99	8.57	ns
8 mA	Std.	0.60	6.96	0.04	0.97	0.39	7.09	5.85	2.84	2.87	9.15	7.91	ns
	–1	0.50	5.80	0.03	0.81	0.32	5.91	4.88	2.37	2.39	7.62	6.59	ns
12 mA	Std.	0.60	5.35	0.04	0.97	0.39	5.45	4.58	3.06	3.23	7.51	6.64	ns
	–1	0.50	4.46	0.03	0.81	0.32	4.54	3.82	2.55	2.69	6.26	5.53	ns
16 mA	Std.	0.60	5.01	0.04	0.97	0.39	5.10	4.30	3.11	3.32	7.16	6.36	ns
	–1	0.50	4.17	0.03	0.81	0.32	4.25	3.58	2.59	2.77	5.97	5.30	ns
24 mA	Std.	0.60	4.67	0.04	0.97	0.39	4.75	4.28	3.16	3.66	6.81	6.34	ns
	–1	0.50	3.89	0.03	0.81	0.32	3.96	3.57	2.64	3.05	5.68	5.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-40 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxxIOBx = 3.0 V

Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.31	0.09	0.94	1.30	0.22	2.35	1.86	2.20	2.45	ns
	–1	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

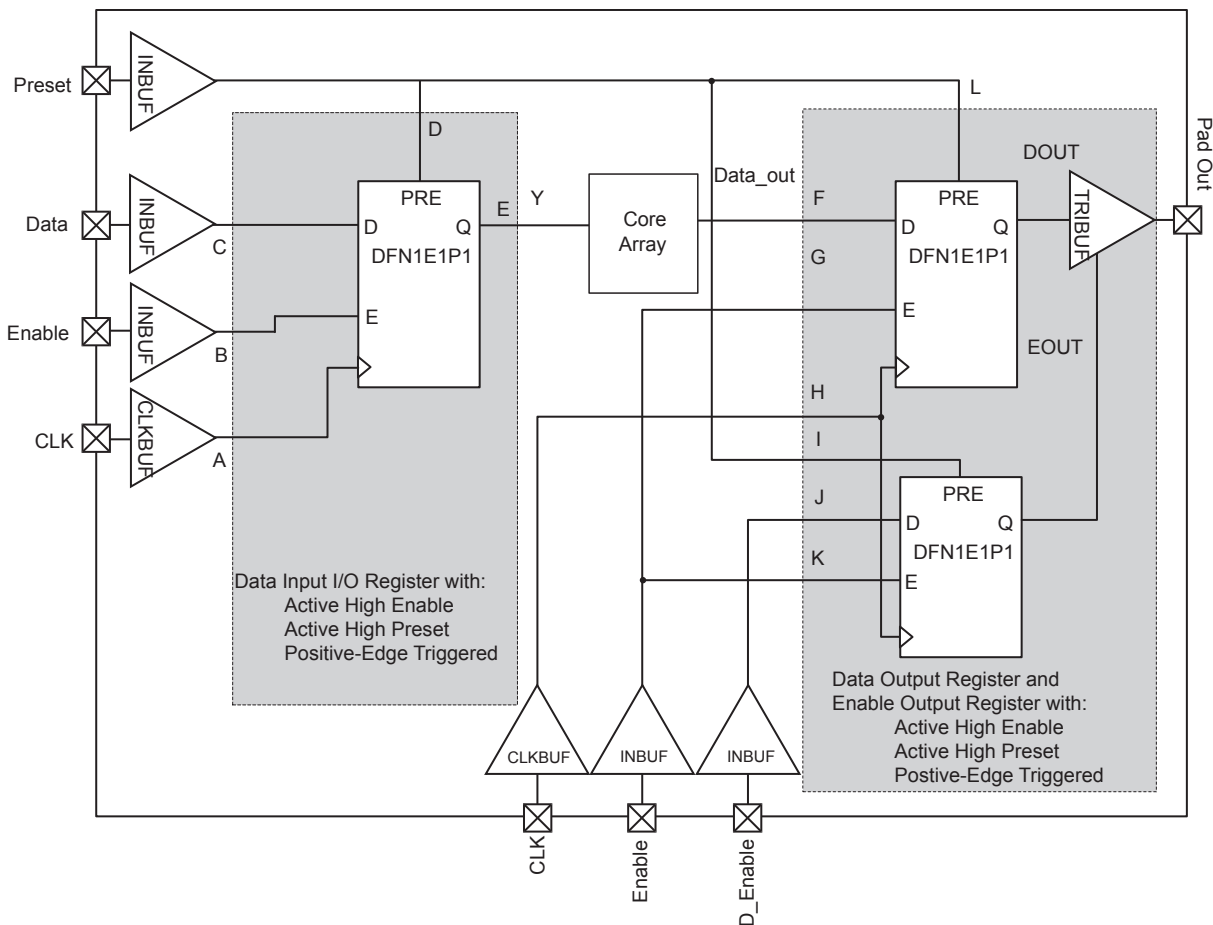


Figure 2-14 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-70 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* See [Figure 2-15 on page 2-46](#) for more information.

Output Register

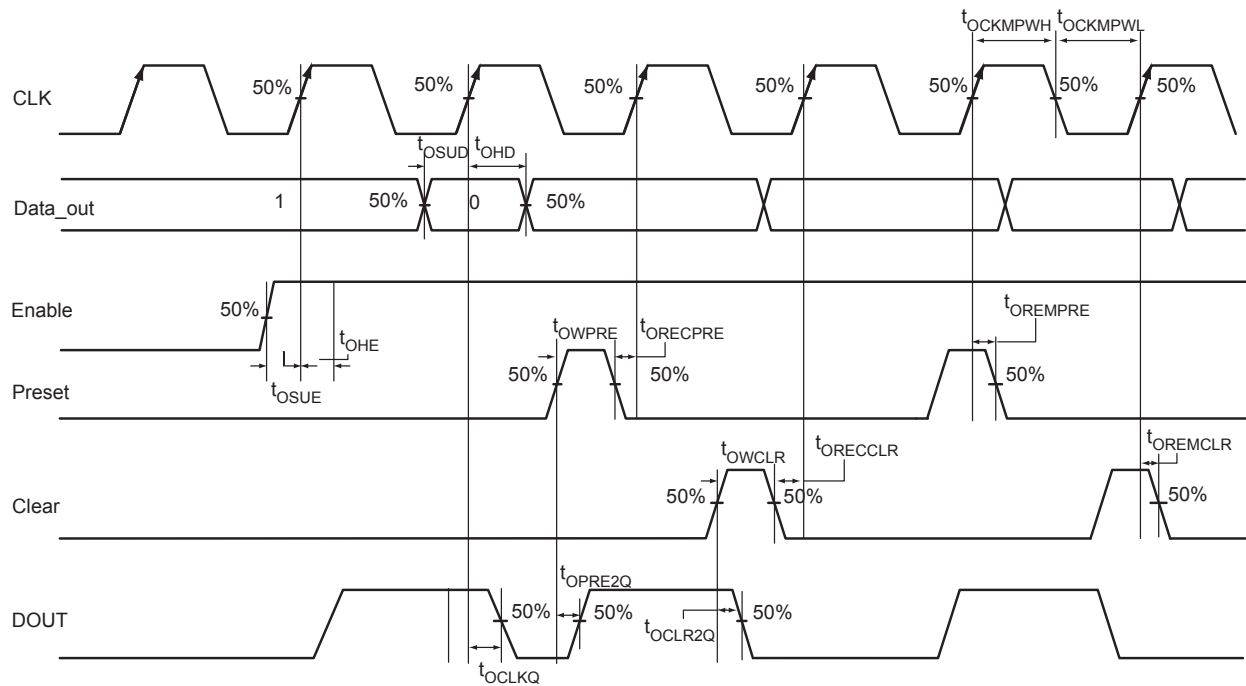


Figure 2-17 • Output Register Timing Diagram

Timing Characteristics

Table 2-72 • Output Data Register Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.72	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.38	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.98	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.98	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.41	0.49	ns
AND2	$Y = A \cdot B$	t_{PD}	0.48	0.57	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.48	0.57	ns
OR2	$Y = A + B$	t_{PD}	0.49	0.59	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.49	0.59	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.75	0.90	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.71	0.85	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.89	1.07	ns
MUX2	$Y = A \text{ IS } + B \text{ S}$	t_{PD}	0.51	0.62	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [IGLOO/e](#), [Fusion](#), [ProASIC3/E](#), and [SmartFusion Macro Library Guide](#).

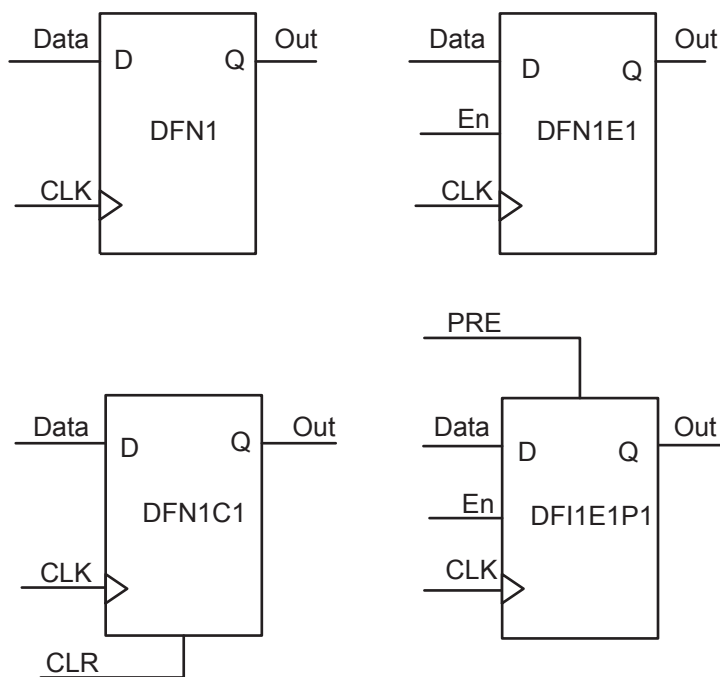


Figure 2-25 • Sample of Sequential Cells

Global Resource Characteristics

A2F200 Clock Tree Topology

Clock delays are device-specific. [Figure 2-27](#) is an example of a global tree used for clock routing. The global tree presented in [Figure 2-27](#) is driven by a CCC located on the west side of the A2F200 device. It is used to drive all D-flip-flops in the device.

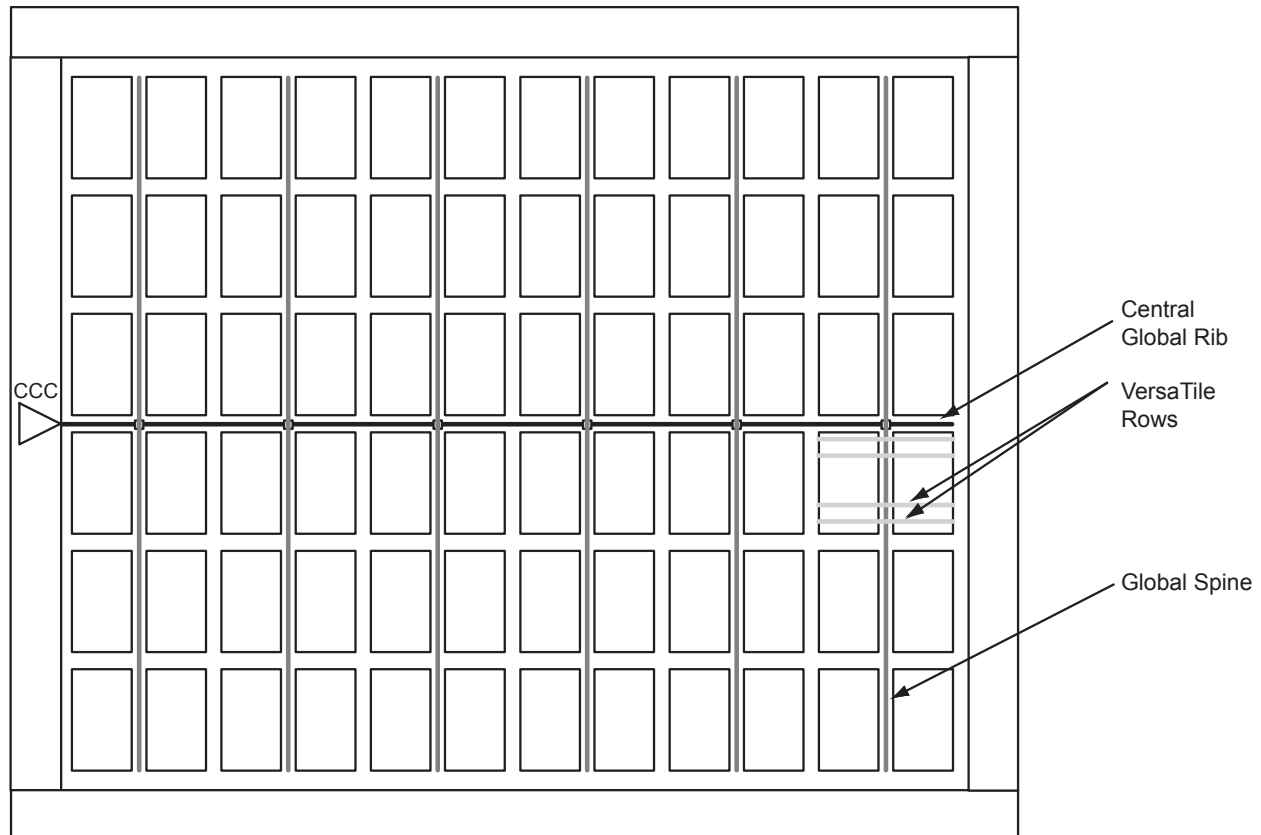


Figure 2-27 • Example of Global Tree Use in an A2F200 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the ["Clock Conditioning Circuits" section on page 2-63](#). [Table 2-80](#) through [Table 2-82 on page 2-61](#) present minimum and maximum global clock delays for the SmartFusion cSoCs. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Waveforms

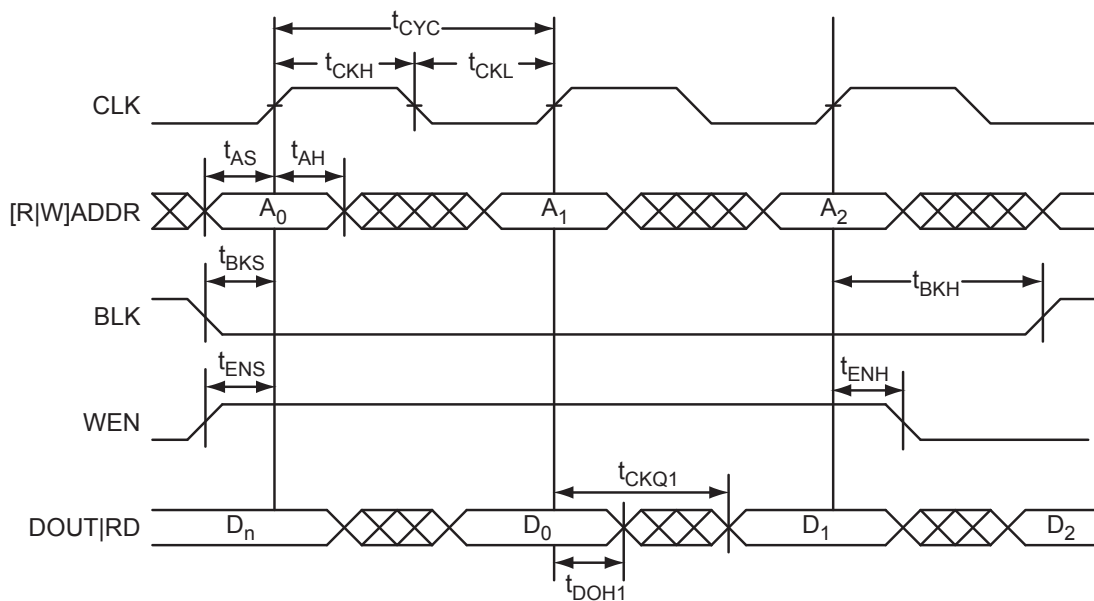


Figure 2-30 • RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18.

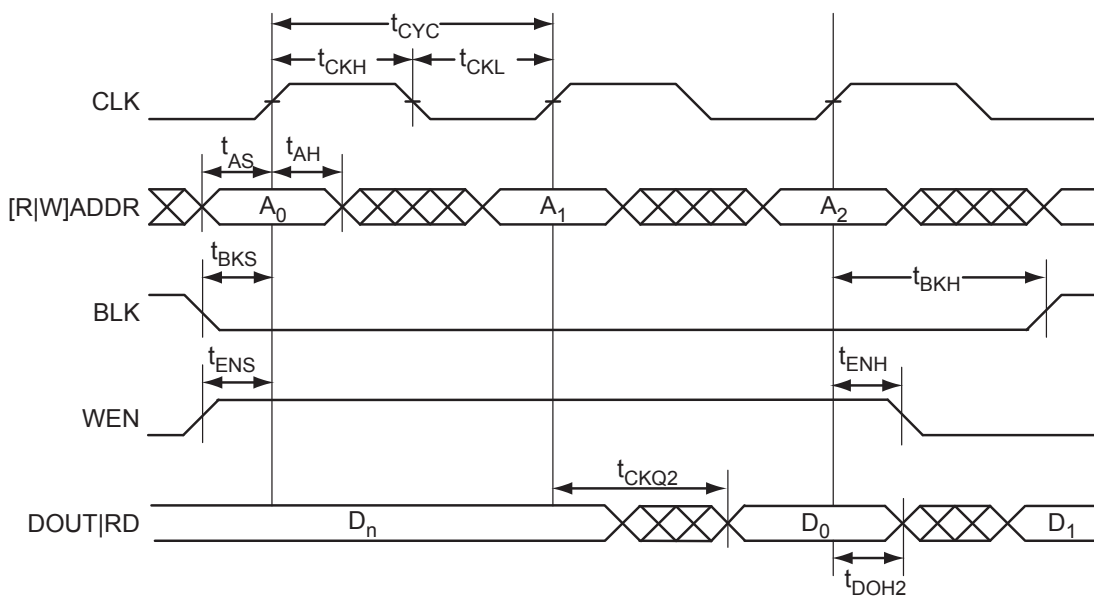


Figure 2-31 • RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18.

Embedded Nonvolatile Memory Block (eNVM)

Electrical Characteristics

Table 2-90 describes the eNVM maximum performance.

Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: $T_J = 85^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	A2F060		A2F200		A2F500		Units
		–1	Std.	–1	Std.	–1	Std.	
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 5 cycles (5:1:1:1*)	50	50	50	50	50	50	MHz
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 6 cycles (6:1:1:1*)	100	80	100	80	100	80	MHz

Note: *6:1:1:1 indicates 6 cycles for the first access and 1 each for the next three accesses. 5:1:1:1 indicates 5 cycles for the first access and 1 each for the next three accesses.

Note: *Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%.

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-91 describes the eFROM maximum performance

Table 2-91 • FlashROM Access Time, Worst Commercial Case Conditions: $T_J = 85^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{CK2Q}	Clock to out per configuration*	28.68	32.98	ns
F_{max}	Maximum Clock frequency	15.00	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-19 for more details.

Timing Characteristics

Table 2-92 • JTAG 1532

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.67	0.77	ns
t_{DIHD}	Test Data Input Hold Time	1.33	1.53	ns
t_{TMSSU}	Test Mode Select Setup Time	0.67	0.77	ns
t_{TMDHD}	Test Mode Select Hold Time	1.33	1.53	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	9.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Temperature Monitor

Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion cSoC and the sensing diode are at the same temperature.

Table 2-94 • Temperature Monitor Performance Specifications

Specification	Test Conditions	Min.	Typical	Max.	Units
Input diode temperature range		–55		150	°C
		233.2		378.15	K
Temperature sensitivity			2.5		mV/K
Intercept	Extrapolated to 0K		0		V
Input referred temperature offset error	At 25°C (298.15K)		±1	1.5	°C
Gain error	Slope of BFSL vs. 2.5 mV/K		±1	2.5	% nom.
Overall accuracy	Peak error from ideal transfer function		±2	±3	°C
Input referred noise	At 25°C (298.15K) – no output averaging		4		°C rms
Output current	Idle mode		100		μA
	Final measurement phases		10		μA
Analog settling time	Measured to 0.1% of final value, (with ADC load)				
	From TM_STB (High)	5			μs
	From ADC_START (High)	5		105	μs
AT parasitic capacitance				500	pF
Power supply rejection ratio	DC (0–10 KHz)	1.2	0.7		°C/V
Input referred temperature sensitivity error	Variation due to device temperature (–40°C to +100°C). External temperature sensor held constant.		0.005	0.008	°C/°C
Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREFx)	VCC33A		200		μA
	VCC33AP		150		μA
	VCC15A		50		μA

Note: All results are based on averaging over 64 samples.

Analog-to-Digital Converter (ADC)

Unless otherwise noted, ADC direct input performance is specified at 25°C with nominal power supply voltages, with the output measured using the external voltage reference with the internal ADC in 12-bit mode and 500 KHz sampling frequency, after trimming and digital compensation.

Table 2-95 • ADC Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)			2.56		V
Gain error			±0.4	±0.7	%
	–40°C to +100°C		±0.4	±0.7	%
Input referred offset voltage			±1	±2	mV
	–40°C to +100°C		±1	±2	
Integral non-linearity (INL)	RMS deviation from BFSL				
	12-bit mode		1.71		LSB
	10-bit mode		0.60	1.00	LSB
	8-bit mode		0.2	0.33	LSB
Differential non-linearity (DNL)	12-bit mode		2.4		LSB
	10-bit mode		0.80	0.94	LSB
	8-bit mode		0.2	0.23	LSB
Signal to noise ratio		62	64		dB
Effective number of bits (ENOB) $\text{ENOB} = \frac{\text{SINAD} - 1.76 \text{ dB}}{6.02 \text{ dB/bit}}$ EQ 10	–1 dBFS input				
	12-bit mode 10 KHz	9.9	10		Bits
	12-bit mode 100 KHz	9.9	10		Bits
	10-bit mode 10 KHz	9.5	9.6		Bits
	10-bit mode 100 KHz	9.5	9.6		Bits
	8-bit mode 10 KHz	7.8	7.9		Bits
	8-bit mode 100 KHz	7.8	7.9		Bits
Full power bandwidth	At –3 dB; –1 dBFS input	300			KHz
Analog settling time	To 0.1% of final value (with 1 Kohm source impedance and with ADC load)		2		µs
Input capacitance	Switched capacitance (ADC sample capacitor)		12	15	pF
	Cs: Static capacitance (Figure 2-44 on page 2-86)				
	CM[n] input		5	7	pF
	TM[n] input		5	7	pF
	ADC[n] input		5	7	pF
Input resistance	Rin: Series resistance (Figure 2-44)		2		KΩ
	Rsh: Shunt resistance, exclusive of switched capacitance effects (Figure 2-44)	10			MΩ

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

User-Defined Supply Pins

Name	Type	Polarity/ Bus Size	Description
VAREF0	Input	1	Analog reference voltage for first ADC. The SmartFusion cSoC can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 μF and 22 μF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the SmartFusion Programmable Analog User's Guide for more information. The SoC Products Group recommends customers use 10 μF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, the VAREFOUT pin must be connected to the appropriate ADC VAREF_x input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1 and VAREF2 together, if ADC0, ADC1, and ADC2 all are used.
VAREF1	Input	1	Analog reference voltage for second ADC See "VAREF0" above for more information.
VAREF2	Input	1	Analog reference voltage for third ADC See "VAREF0" above for more.
VAREFOUT	Out	1	Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREF_x input—either the VAREF0 or VAREF1 pin—on the PCB.

Table 5-1 • Recommended Tie-Off Values for the TCK and TRST Pins

VJTAG	Tie-Off Resistance^{1, 2}
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Notes:

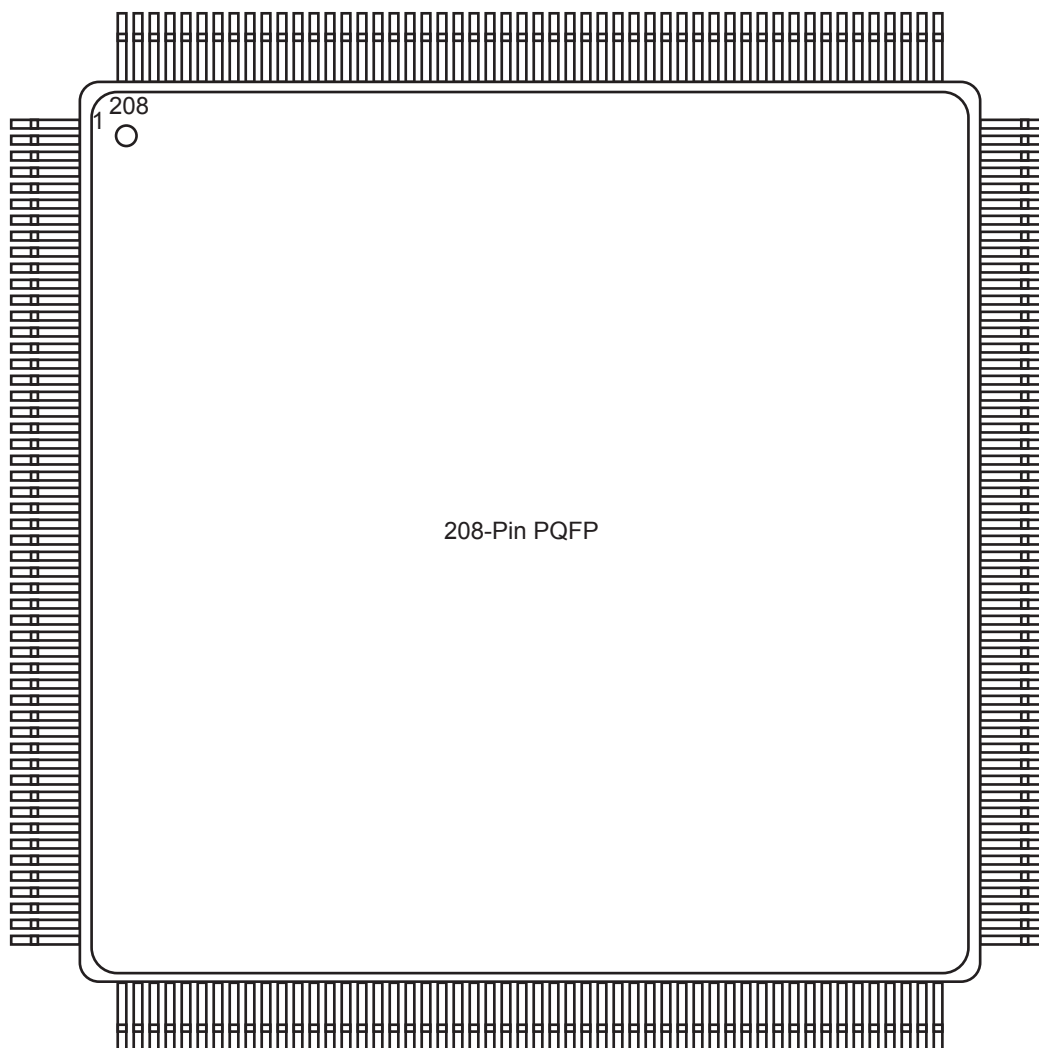
1. The TCK pin can be pulled up/down.
2. The TRST pin can only be pulled down.
1. Equivalent parallel resistance if more than one device is on JTAG chain.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
F12	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
F13	GND	GND	GND
F14	GCB1/IO19PPB0V0	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
F15	GNDQ	GNDQ	GNDQ
F16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
F17	GCB0/IO19NPB0V0	IO24NDB1V0	IO33NDB1V0
F19	IO23NDB1V0	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
F21	GCA2/IO21PDB1V0	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
G1	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G3	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	NC	GFB1/IO65PDB5V0	GFB1/IO82PDB5V0
G6	EMC_DB[10]/IO43NDB5V0	EMC_DB[10]/IO69NDB5V0	EMC_DB[10]/IO86NDB5V0
G9	NC	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
G13	GCA0/IO20NPB0V0	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
G16	NC	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
G17	IO22NPB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
G19	GCC2/IO23PDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
G21	GND	GND	GND
H1	EMC_DB[9]/IO40PPB5V0	EMC_DB[9]/GEC1/IO63PPB5V0	EMC_DB[9]/GEC1/IO80PPB5V0
H3	GND	GND	GND
H5	NC	GFB0/IO65NDB5V0	GFB0/IO82NDB5V0
H6	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H8	GND	GND	GND
H9	VCC	VCC	VCC
H10	GND	GND	GND
H11	VCC	VCC	VCC
H12	GND	GND	GND
H13	VCC	VCC	VCC
H14	GND	GND	GND
H16	NC	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
H17	NC	GDC2/IO32PPB1V0	GDC2/IO41PPB1V0

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

PQ208



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

Pin Number	PQ208	
	A2F200	A2F500
63	TM1	TM1
64	CM1	CM1
65	ABPS3	ABPS3
66	ABPS2	ABPS2
67	ADC0	ADC0
68	ADC1	ADC1
69	ADC2	ADC2
70	ADC3	ADC3
71	VAREF0	VAREF0
72	GND33ADC0	GND33ADC0
73	VCC33ADC0	VCC33ADC0
74	GND33ADC0	GND33ADC0
75	VCC15ADC0	VCC15ADC0
76	GND15ADC0	GND15ADC0
77	GND15ADC1	GND15ADC1
78	VCC15ADC1	VCC15ADC1
79	GND33ADC1	GND33ADC1
80	VCC33ADC1	VCC33ADC1
81	GND33ADC1	GND33ADC1
82	VAREF1	VAREF1
83	ADC7	ADC7
84	ADC6	ADC6
85	ADC5	ADC5
86	ADC4	ADC4
87	ABPS6	ABPS6
88	ABPS7	ABPS7
89	CM3	CM3
90	TM3	TM3
91	GNDTM1	GNDTM1
92	TM2	TM2
93	CM2	CM2

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
H13	TDO	TDO	TDO
H14	TDI	TDI	TDI
H15	JTAGSEL	JTAGSEL	JTAGSEL
H16	GND	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC	GNDRCOSC
J5	NC	GNDQ	GNDQ
J6	GND	GND	GND
J7	VCC	VCC	VCC
J8	GND	GND	GND
J9	VCC	VCC	VCC
J10	GND	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND	GND
K8	VCC	VCC	VCC
K9	GND	GND	GND
K10	VCC	VCC	VCC
K11	GND	GND	GND

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
P10	TM0	TM3	TM3
P11	GNDA	GNDA	GNDA
P12	VCCMAINXTAL	VCCMAINXTAL	VCCMAINXTAL
P13	GNDLPXTAL	GNDLPXTAL	GNDLPXTAL
P14	VDDBAT	VDDBAT	VDDBAT
P15	PTM	PTM	PTM
P16	PTBASE	PTBASE	PTBASE
R1	PCAP	PCAP	PCAP
R2	SDD0	SDD0	SDD0
R3	ADC0	ABPS0	ABPS0
R4	ADC3	TM0	TM0
R5	NC	ABPS2	ABPS2
R6	NC	ADC1	ADC1
R7	NC	VCC33ADC0	VCC33ADC0
R8	VCC15ADC0	VCC15ADC1	VCC15ADC1
R9	ADC10	ADC7	ADC7
R10	ABPS1	ABPS7	ABPS7
R11	NC	ABPS4	ABPS4
R12	MAINXIN	MAINXIN	MAINXIN
R13	MAINXOUT	MAINXOUT	MAINXOUT
R14	LPXIN	LPXIN	LPXIN
R15	LPXOUT	LPXOUT	LPXOUT
R16	VCC33A	VCC33A	VCC33A
T1	NCAP	NCAP	NCAP
T2	ADC1	ABPS1	ABPS1
T3	ADC2	CM0	CM0
T4	NC	GNDTM0	GNDTM0
T5	NC	ADC0	ADC0
T6	NC	VAREF0	VAREF0
T7	NC	GND33ADC0	GND33ADC0
T8	GND15ADC0	GND15ADC1	GND15ADC1

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.