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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, SPI, UART/USART |
| Speed | 80MHz |
| Primary Attributes | ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 288-TFBGA, CSPBGA |
| Supplier Device Package | 288-CSP (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-csg288 |

# 1 – SmartFusion Family Overview

## Introduction

The SmartFusion® family of cSoCs builds on the technology first introduced with the Fusion mixed signal FPGAs. SmartFusion cSoCs are made possible by integrating FPGA technology with programmable high-performance analog and hardened ARM Cortex-M3 microcontroller blocks on a flash semiconductor process. The SmartFusion cSoC takes its name from the fact that these three discrete technologies are integrated on a single chip, enabling the lowest cost of ownership and smallest footprint solution to you.

## General Description

### Microcontroller Subsystem (MSS)

The MSS is composed of a 100 MHz Cortex-M3 processor and integrated peripherals, which are interconnected via a multi-layer AHB bus matrix (ABM). This matrix allows the Cortex-M3 processor, FPGA fabric master, Ethernet media access controller (MAC), when available, and peripheral DMA (PDMA) controller to act as masters to the integrated peripherals, FPGA fabric, embedded nonvolatile memory (eNVM), embedded synchronous RAM (eSRAM), external memory controller (EMC), and analog compute engine (ACE) blocks.

SmartFusion cSoCs of different densities offer various sets of integrated peripherals. Available peripherals include SPI, $I^2C$, and UART serial ports, embedded FlashROM (EFROM), 10/100 Ethernet MAC, timers, phase-locked loops (PLLs), oscillators, real-time counters (RTC), and peripheral DMA controller (PDMA).

### Programmable Analog

#### *Analog Front-End (AFE)*

SmartFusion cSoCs offer an enhanced analog front-end compared to Fusion devices. The successive approximation register analog-to-digital converters (SAR ADC) are similar to those found on Fusion devices. SmartFusion cSoC also adds first order sigma-delta digital-to-analog converters (SDD DAC).

SmartFusion cSoCs can handle multiple analog signals simultaneously with its signal conditioning blocks (SCBs). SCBs are made of a combination of active bipolar prescalers (ABPS), comparators, current monitors and temperature monitors. ABPS modules allow larger bipolar voltages to be fed to the ADC. Current monitors take the voltage across an external sense resistor and convert it to a voltage suitable for the ADC input range. Similarly, the temperature monitor reads the current through an external PN-junction (diode or transistor) and converts it internally for the ADC. The SCB also includes comparators to monitor fast signal thresholds without using the ADC. The output of the comparators can be fed to the analog compute engine or the ADC.

#### *Analog Compute Engine (ACE)*

The mixed signal blocks found in SmartFusion cSoCs are controlled and connected to the rest of the system via a dedicated processor called the analog compute engine (ACE). The role of the ACE is to offload control of the analog blocks from the Cortex-M3, thus offering faster throughput or better power consumption compared to a system where the main processor is in charge of monitoring the analog resources. The ACE is built to handle sampling, sequencing, and post-processing of the ADCs, DACs, and SCBs.

## ProASIC3 FPGA Fabric

The SmartFusion cSoC family, based on the proven, low power, firm-error immune ProASIC®3 flash FPGA architecture, benefits from the advantages only flash-based devices offer:

### Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based SmartFusion cSoCs are Instant On and do not need to be loaded from an external boot PROM at each power-up. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system programming (ISP) to support future design iterations and critical field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry standard AES algorithm with MAC data authentication on the device.

### Low Power

Flash-based SmartFusion cSoCs exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With SmartFusion cSoCs, there is no power-on current and no high current transition, both of which are common with SRAM-based FPGAs.

SmartFusion cSoCs also have low dynamic power consumption and support very low power time-keeping mode, offering further power savings.

### Security

As the nonvolatile, flash-based SmartFusion cSoC family requires no boot PROM, there is no vulnerable external bitstream. SmartFusion cSoCs incorporate FlashLock®, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only a device with nonvolatile flash programming can offer.

SmartFusion cSoCs utilize a 128-bit flash-based key lock and a separate AES key to provide security for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the AES-128 block cipher encryption standard (FIPS Publication 192).

SmartFusion cSoCs with AES-based security are designed to provide protection for remote field updates over public networks, such as the Internet, and help to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the SmartFusion cSoC family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. SmartFusion cSoCs, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry standard security measures, making remote ISP feasible. A SmartFusion cSoC provides the highest security available for programmable logic designs.

### Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based SmartFusion cSoCs do not require system configuration components such as electrically erasable programmable read-only memories (EEPROMs) or microcontrollers to load device configuration data during power-up. This reduces bill-of-materials costs and PCB area, and increases system security and reliability.

### Instant On

Flash-based SmartFusion cSoCs are Instant On. Instant On SmartFusion cSoCs greatly simplify total system design and reduce total system cost by eliminating the need for complex programmable logic devices (CPLDs). SmartFusion Instant On clocking (PLLs) replace off-chip clocking resources. In addition, glitches and brownouts in system power will not corrupt the SmartFusion flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored.

# 2 – SmartFusion DC and Switching Characteristics

## General Specifications

### Operating Conditions

Stresses beyond the operating conditions listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-3 on page 2-3 is not implied.

***Table 2-1 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLLx | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCFPGAIOBx | DC FPGA I/O buffer supply voltage | –0.3 to 3.75 | V |
| VCCMSSIOBx | DC MSS I/O buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3 V to 3.6 V<br>(when I/O hot insertion mode is enabled)<br>–0.3 V to (VCCxxxxIOBx + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| VCC33A | Analog clean 3.3 V supply to the analog circuitry | –0.3 to 3.75 | V |
| VCC33ADCx | Analog 3.3 V supply to ADC | –0.3 to 3.75 | V |
| VCC33AP | Analog clean 3.3 V supply to the charge pump | –0.3 to 3.75 | V |
| VCC33SDDx | Analog 3.3 V supply to the sigma-delta DAC | –0.3 to 3.75 | V |
| VAREFx | Voltage reference for ADC | 1.0 to 3.75 | V |
| VCCRCOSC | Analog supply to the integrated RC oscillator | –0.3 to 3.75 | V |
| VDDBAT | External battery supply | –0.3 to 3.75 | V |
| VCCMAINXTAL | Analog supply to the main crystal oscillator | –0.3 to 3.75 | V |
| VCCLPXTAL | Analog supply to the low power 32 kHz crystal oscillator | –0.3 to 3.75 | V |
| VCCENVM | Embedded nonvolatile memory supply | –0.3 to 1.65 | V |
| VCCESRAM | Embedded SRAM supply | –0.3 to 1.65 | V |
| VCC15A | Analog 1.5 V supply to the analog circuitry | –0.3 to 1.65 | V |
| VCC15ADCx | Analog 1.5 V supply to the ADC | –0.3 to 1.65 | V |
| $T_{STG}$[1] | Storage temperature | –65 to +150 | °C |
| $T_J$[1] | Junction temperature | 125 | °C |

*Notes:*

1. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-4. For recommended operating conditions, refer to Table 2-3 on page 2-3.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-5 on page 2-4.*

**Table 2-28 • I/O Output Buffer Maximum Resistances[1]**
**Applicable to MSS I/O Banks**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ ($\Omega$)[2] | $R_{PULL\text{-}UP}$ ($\Omega$)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 8mA | 50 | 150 |
| 2.5 V LVCMOS | 8 mA | 50 | 100 |
| 1.8 V LVCMOS | 4 mA | 100 | 112 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

**Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCxxxxIOBx | $R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$) | | $R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$) | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |

*Notes:*

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

**Table 2-52 • 1.8 V LVCMOS High Slew**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCxxxxIOBx = 1.7 V**
**Applicable to MSS I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.22 | 2.77 | 0.09 | 1.09 | 1.64 | 0.22 | 2.82 | 2.72 | 2.21 | 2.25 | ns |
| | –1 | 0.18 | 2.31 | 0.07 | 0.91 | 1.37 | 0.18 | 2.35 | 2.27 | 1.84 | 1.87 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

# DDR Module Specifications

## Input DDR Module

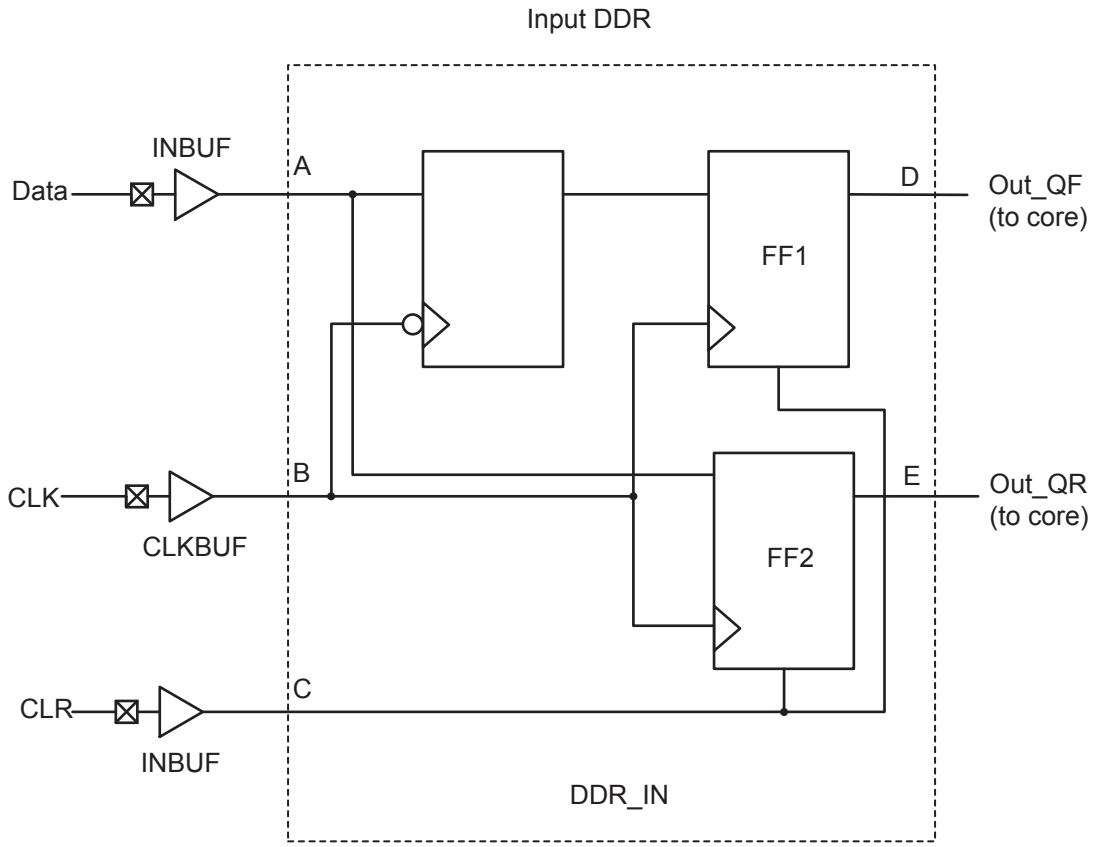



***Figure 2-19 •*** **Input DDR Timing Model**

***Table 2-74 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

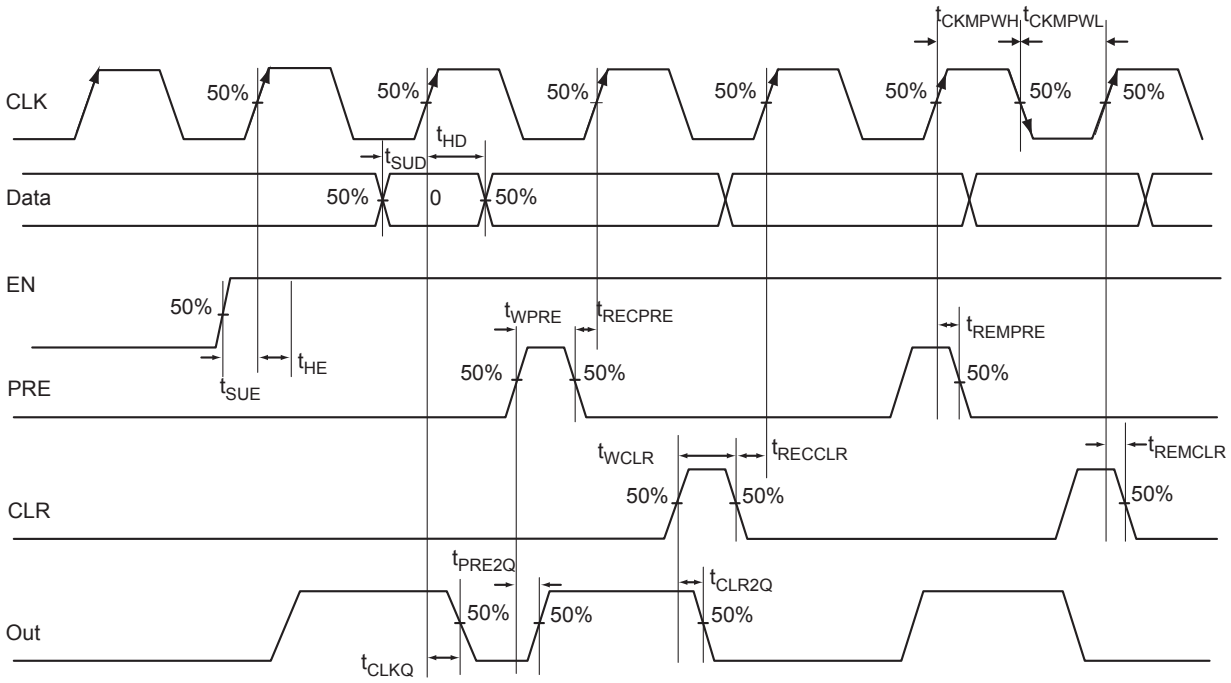



***Figure 2-26 •*** **Timing Model and Waveforms**

## Timing Characteristics

***Table 2-79 •*** **Register Delays**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.56 | 0.67 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.44 | 0.52 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.46 | 0.55 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.41 | 0.49 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.41 | 0.49 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.23 | 0.27 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.23 | 0.27 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.22 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.22 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.32 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.36 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

**Table 2-82 • A2F060 Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VCC = 1.425 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.75 | 0.96 | 0.90 | 1.15 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.72 | 0.98 | 0.86 | 1.17 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 1.00 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.26 | | 0.31 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

# RC Oscillator

The table below describes the electrical characteristics of the RC oscillator.

## RC Oscillator Characteristics

**Table 2-83 • Electrical Characteristics of the RC Oscillator**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| FRC | Operating frequency | | | 100 | | MHz |
| | Accuracy | Temperature: –40°C to 100°C<br>Voltage: 3.3 V ± 5% | | 1 | | % |
| | Output jitter | Period jitter (at 5 K cycles) | | 100 | | ps RMS |
| | | Cycle-to-cycle jitter (at 5 K cycles) | | 100 | | ps RMS |
| | | Period jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | | 150 | | ps RMS |
| | | Cycle-to-cycle jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | | 150 | | ps RMS |
| | Output duty cycle | | | 50 | | % |
| IDYNRC | Operating current | 3.3 V domain | | 1 | | mA |
| | | 1.5 V domain | | 2 | | mA |

***Table 2-96* • ABPS Performance Specifications (continued)**

| Specification | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Input referred offset voltage | | | | | |
| | GDEC[1:0] = 11 | –0.31 | –0.07 | 0.31 | % FS* |
| | –40ºC to +100ºC | –1.00 | | 1.47 | % FS* |
| | GDEC[1:0] = 10 | –0.34 | –0.07 | 0.34 | % FS* |
| | –40ºC to +100ºC | –0.90 | | 1.37 | % FS* |
| | GDEC[1:0] = 01 | –0.61 | –0.07 | 0.35 | % FS* |
| | –40ºC to +100ºC | –1.05 | | 1.35 | % FS* |
| | GDEC[1:0] = 00 | –0.39 | –0.07 | 0.35 | % FS* |
| | –40ºC to +100ºC | –1.06 | | 1.38 | % FS* |
| SINAD | | 53 | 56 | | dB |
| Non-linearity | RMS deviation from BFSL | | | 0.5 | % FS* |
| Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 11* | GDEC[1:0] = 11 (±2.56 range), –1 dBFS input | | | | |
| | 12-bit mode 10 KHz | 8.6 | 9.1 | | Bits |
| | 12-bit mode 100 KHz | 8.6 | 9.1 | | Bits |
| | 10-bit mode 10 KHz | 8.5 | 8.9 | | Bits |
| | 10-bit mode 100 KHz | 8.5 | 8.9 | | Bits |
| | 8-bit mode 10 KHz | 7.7 | 7.8 | | Bits |
| | 8-bit mode 100 KHz | 7.7 | 7.8 | | Bits |
| Large-signal bandwidth | –1 dBFS input | | 1 | | MHz |
| Analog settling time | To 0.1% of final value (with ADC load) | | | 10 | µs |
| Input resistance | | | 1 | | MΩ |
| Power supply rejection ratio | DC (0–1 KHz) | 38 | 40 | | dB |
| ABPS power supply current requirements (not including ADC or VAREFx) | ABPS_EN = 1 (operational mode) | | | | |
| | VCC33A | | 123 | 134 | µA |
| | VCC33AP | | 89 | 94 | µA |
| | VCC15A | | 1 | | µA |

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

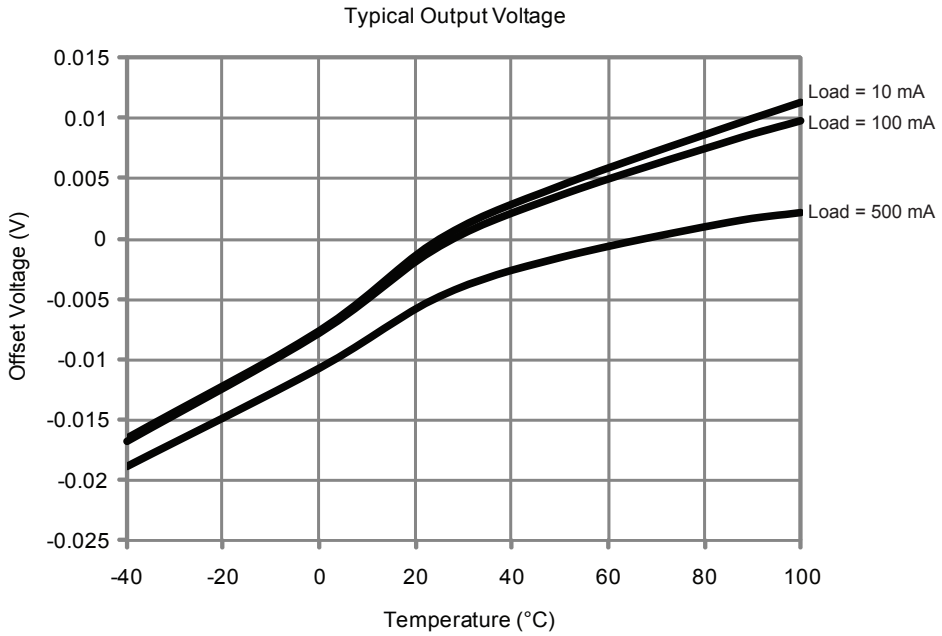



***Figure 2-45 •*** **Typical Output Voltage**

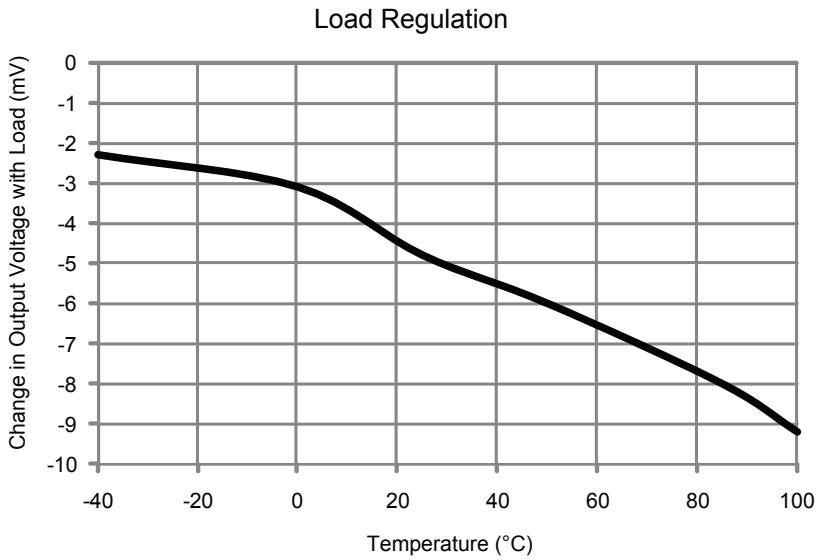



***Figure 2-46 •*** **Load Regulation**

**Table 2-100 • SPI Characteristics**
**Commercial Case Conditions: $T_J$ = 85ºC, VDD = 1.425 V, –1 Speed Grade (continued)**

| Symbol | Description and Condition | A2F060 | A2F200 | A2F500 | Unit |
|---|---|---|---|---|---|
| sp6 | Data from master (SPI_x_DO) setup time [2] | 1 | 1 | 1 | pclk cycles |
| sp7 | Data from master (SPI_x_DO) hold time [2] | 1 | 1 | 1 | pclk cycles |
| sp8 | SPI_x_DI setup time [2] | 1 | 1 | 1 | pclk cycles |
| sp9 | SPI_x_DI hold time [2] | 1 | 1 | 1 | pclk cycles |

*Notes:*

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

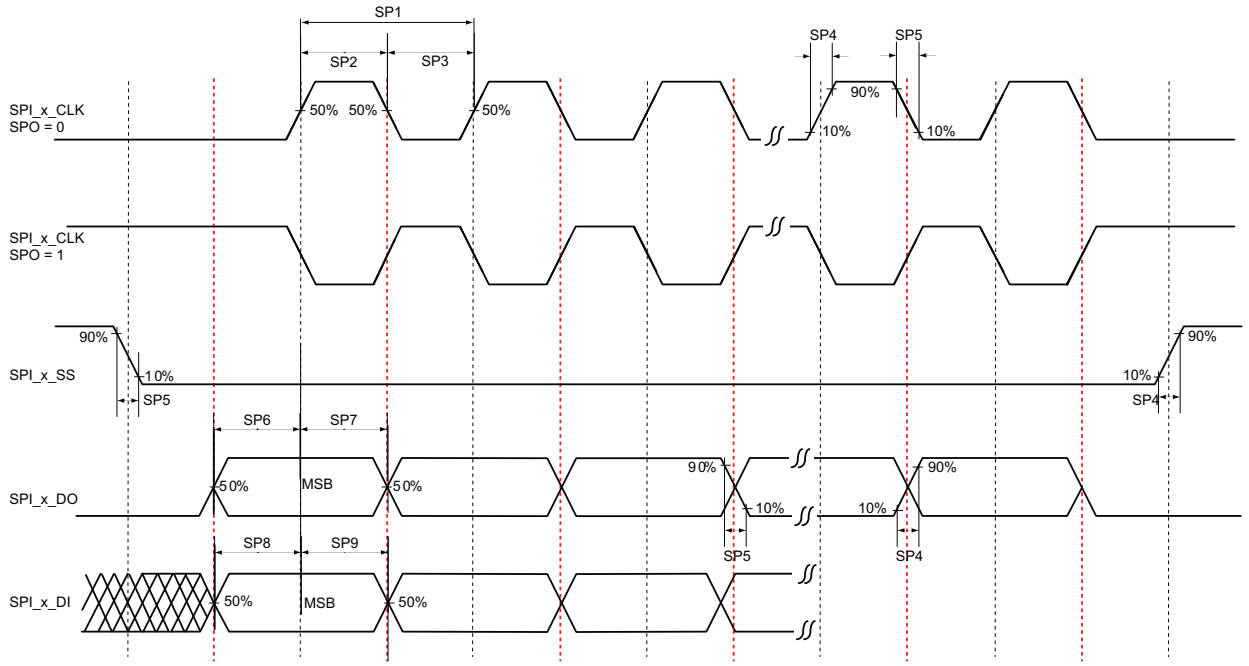



**Figure 2-47 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

# Inter-Integrated Circuit ($I^2C$) Characteristics

This section describes the DC and switching of the $I^2C$ interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 2-48 on page 2-92.

***Table 2-101* • $I^2C$ Characteristics**
**Commercial Case Conditions: $T_J$ = 85ºC, $V_{DD}$ = 1.425 V, –1 Speed Grade**

| Parameter | Definition | Condition | Value | Unit |
|---|---|---|---|---|
| $V_{IL}$ | Minimum input low voltage | – | See Table 2-36 on page 2-30 | – |
| | Maximum input low voltage | – | See Table 2-36 | – |
| $V_{IH}$ | Minimum input high voltage | – | See Table 2-36 | – |
| | Maximum input high voltage | – | See Table 2-36 | – |
| $V_{OL}$ | Maximum output voltage low | $I_{OL}$ = 8 mA | See Table 2-36 | – |
| $I_{IL}$ | Input current high | – | See Table 2-36 | – |
| $I_{IH}$ | Input current low | – | See Table 2-36 | – |
| $V_{hyst}$ | Hysteresis of Schmitt trigger inputs | – | See Table 2-33 on page 2-29 | V |
| $T_{FALL}$ | Fall time [2] | VIHmin to VILMax, $C_{load}$ = 400 pF | 15.0 | ns |
| | | VIHmin to VILMax, $C_{load}$ = 100 pF | 4.0 | ns |
| $T_{RISE}$ | Rise time [2] | VILMax to VIHmin, $C_{load}$ = 400pF | 19.5 | ns |
| | | VILMax to VIHmin, $C_{load}$ = 100pF | 5.2 | ns |
| Cin | Pin capacitance | VIN = 0, f = 1.0 MHz | 8.0 | pF |
| $R_{pull-up}$ | Output buffer maximum pull-down Resistance [1] | – | 50 | Ω |
| $R_{pull-down}$ | Output buffer maximum pull-up Resistance [1] | – | 150 | Ω |
| $D_{max}$ | Maximum data rate | Fast mode | 400 | Kbps |
| $t_{LOW}$ | Low period of I2C_x_SCL [3] | – | 1 | pclk cycles |
| $t_{HIGH}$ | High period of I2C_x_SCL [3] | – | 1 | pclk cycles |
| $t_{HD;STA}$ | START hold time [3] | – | 1 | pclk cycles |
| $t_{SU;STA}$ | START setup time [3] | – | 1 | pclk cycles |
| $t_{HD;DAT}$ | DATA hold time [3] | – | 1 | pclk cycles |
| $t_{SU;DAT}$ | DATA setup time [3] | – | 1 | pclk cycles |

*Notes:*

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
3. *For allowable Pclk configurations, refer to the Inter-Integrated Circuit ($I^2C$) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide.*

## User I/O Naming Conventions

The naming convention used for each FPGA user I/O is Gmn/IOuxwByVz, where:

**Gmn** is only used for I/Os that also have CCC access—i.e., global pins. Refer to the "Global I/O Naming Conventions" section on page 5-6.

**u** = I/O pair number in bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.

**x** = P (positive) or N (negative) or S (single-ended) or R (regular, single-ended).

**w** = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential Pairs (D), adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

**B** = Bank

**y** = Bank number starting at 0 from northwest I/O bank and incrementing clockwise.

**V** = Reference voltage

**z** = VREF mini bank number.

The FPGA user I/O pin functions as an input, output, tristate or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are disabled by Libero SoC software and include a weak pull-up resistor. During power-up, the used I/O pins are tristated with no pull-up or pull-down resistors until I/O enable (there is a delay after voltage stabilizes, and different I/O banks power up sequentially to avoid a surge of ICCI).

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Some of these pins are also multiplexed with integrated peripherals in the MSS (Ethernet MAC and external memory controller).

All unused MSS I/Os are tristated by default (with output buffer disabled). However, you can configure it as weak pull-up or pull-down by using Libero SoC I/O attributor window. The Schmitt trigger is disabled. Essentially, I/Os have the reset values as defined in Table 19-25 IOMUX_n_CR, in the *SmartFusion Microcontroller Subsystem User's Guide*.

By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to "Specifying I/O States During Programming" on page 1-3. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration. For more information, see the SmartFusion FPGA User I/Os section in the *SmartFusion FPGA Fabric User's Guide*.

# Special Function Pins

| Name | Type | Polarity/Bus Size | Description |
|---|---|---|---|
| NC | | | No connect<br>This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device. |
| DC | | | Do not connect.<br>This pin should not be connected to any signals on the PCB. These pins should be left unconnected. |
| LPXIN | In | 1 | Low power 32 KHz crystal oscillator.<br>Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*. |
| LPXOUT | In | 1 | Low power 32 KHz crystal oscillator.<br>Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*. |
| MAINXIN | In | 1 | Main crystal oscillator circuit.<br>Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value.<br>If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating.<br>For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*. |
| MAINXOUT | Out | 1 | Main crystal oscillator circuit.<br>Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value.<br>If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating.<br>For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*. |

| Pin Number | PQ208 | |
|---|---|---|
| | A2F200 | A2F500 |
| 32 | VCCRCOSC | VCCRCOSC |
| 33 | MSS_RESET_N | MSS_RESET_N |
| 34 | VCCESRAM | VCCESRAM |
| 35 | MAC_MDC/IO48RSB4V0 | MAC_MDC/IO57RSB4V0 |
| 36 | MAC_MDIO/IO49RSB4V0 | MAC_MDIO/IO58RSB4V0 |
| 37 | MAC_TXEN/IO52RSB4V0 | MAC_TXEN/IO61RSB4V0 |
| 38 | MAC_CRSDV/IO51RSB4V0 | MAC_CRSDV/IO60RSB4V0 |
| 39 | MAC_RXER/IO50RSB4V0 | MAC_RXER/IO59RSB4V0 |
| 40 | GND | GND |
| 41 | VCCMSSIOB4 | VCCMSSIOB4 |
| 42 | VCC | VCC |
| 43 | MAC_TXD[0]/IO56RSB4V0 | MAC_TXD[0]/IO65RSB4V0 |
| 44 | MAC_TXD[1]/IO55RSB4V0 | MAC_TXD[1]/IO64RSB4V0 |
| 45 | MAC_RXD[0]/IO54RSB4V0 | MAC_RXD[0]/IO63RSB4V0 |
| 46 | MAC_RXD[1]/IO53RSB4V0 | MAC_RXD[1]/IO62RSB4V0 |
| 47 | MAC_CLK | MAC_CLK |
| 48 | GNDSDD0 | GNDSDD0 |
| 49 | VCC33SDD0 | VCC33SDD0 |
| 50 | VCC15A | VCC15A |
| 51 | PCAP | PCAP |
| 52 | NCAP | NCAP |
| 53 | VCC33AP | VCC33AP |
| 54 | VCC33N | VCC33N |
| 55 | SDD0 | SDD0 |
| 56 | GNDA | GNDA |
| 57 | GNDAQ | GNDAQ |
| 58 | ABPS0 | ABPS0 |
| 59 | ABPS1 | ABPS1 |
| 60 | CM0 | CM0 |
| 61 | TM0 | TM0 |
| 62 | GNDTM0 | GNDTM0 |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin Number | PQ208 | |
|---|---|---|
| | A2F200 | A2F500 |
| 63 | TM1 | TM1 |
| 64 | CM1 | CM1 |
| 65 | ABPS3 | ABPS3 |
| 66 | ABPS2 | ABPS2 |
| 67 | ADC0 | ADC0 |
| 68 | ADC1 | ADC1 |
| 69 | ADC2 | ADC2 |
| 70 | ADC3 | ADC3 |
| 71 | VAREF0 | VAREF0 |
| 72 | GND33ADC0 | GND33ADC0 |
| 73 | VCC33ADC0 | VCC33ADC0 |
| 74 | GND33ADC0 | GND33ADC0 |
| 75 | VCC15ADC0 | VCC15ADC0 |
| 76 | GND15ADC0 | GND15ADC0 |
| 77 | GND15ADC1 | GND15ADC1 |
| 78 | VCC15ADC1 | VCC15ADC1 |
| 79 | GND33ADC1 | GND33ADC1 |
| 80 | VCC33ADC1 | VCC33ADC1 |
| 81 | GND33ADC1 | GND33ADC1 |
| 82 | VAREF1 | VAREF1 |
| 83 | ADC7 | ADC7 |
| 84 | ADC6 | ADC6 |
| 85 | ADC5 | ADC5 |
| 86 | ADC4 | ADC4 |
| 87 | ABPS6 | ABPS6 |
| 88 | ABPS7 | ABPS7 |
| 89 | CM3 | CM3 |
| 90 | TM3 | TM3 |
| 91 | GNDTM1 | GNDTM1 |
| 92 | TM2 | TM2 |
| 93 | CM2 | CM2 |

*Notes:*

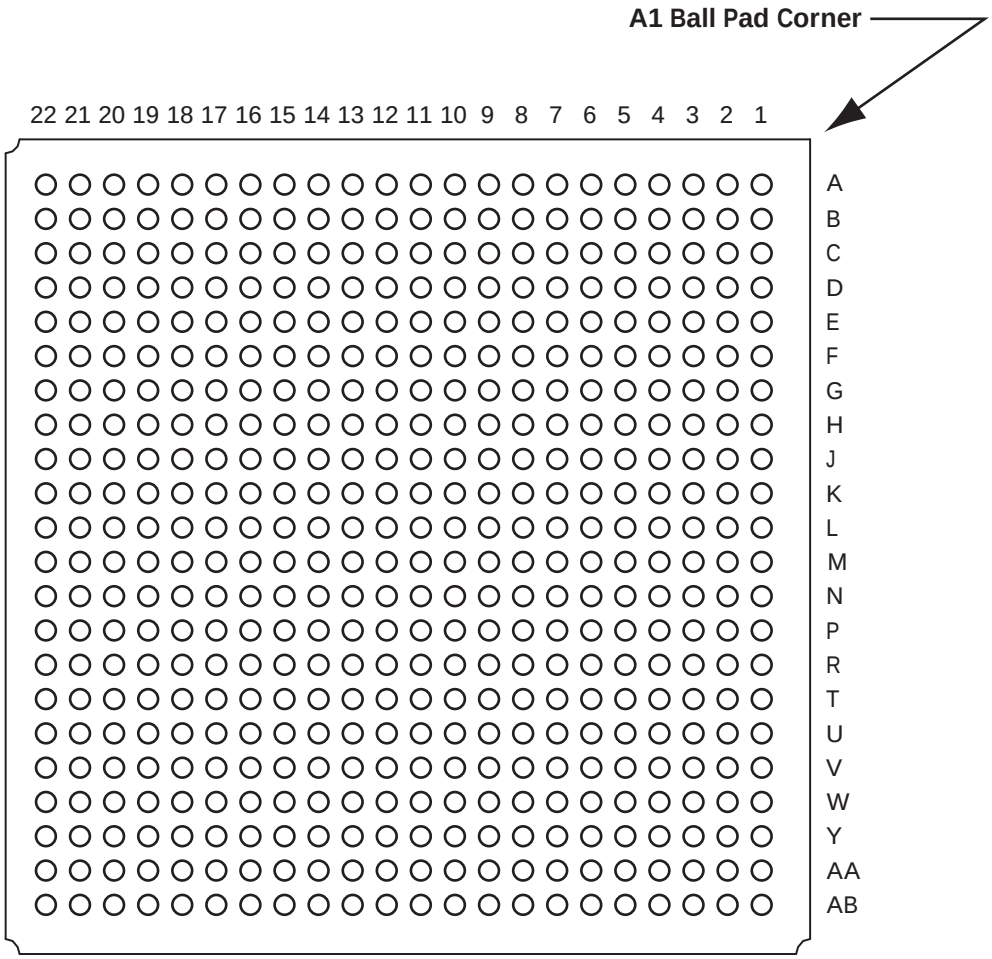
1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| F14 | IO21NDB1V0 | GCB0/IO27NDB1V0 | GCB0/IO34NDB1V0 |
| F15 | GND | GND | GND |
| F16 | VCCENVM | VCCENVM | VCCENVM |
| G1 | EMC_DB[8]/IO40NDB5V0 | EMC_DB[8]/GEC0/IO63NDB5V0 | EMC_DB[8]/GEC0/IO80NDB5V0 |
| G2 | EMC_DB[7]/IO39PDB5V0 | EMC_DB[7]/GEB1/IO62PDB5V0 | EMC_DB[7]/GEB1/IO79PDB5V0 |
| G3 | EMC_DB[6]/IO39NDB5V0 | EMC_DB[6]/GEB0/IO62NDB5V0 | EMC_DB[6]/GEB0/IO79NDB5V0 |
| G4 | GFC2/IO41PDB5V0 | GFC2/IO67PDB5V0 | GFC2/IO84PDB5V0 |
| G5 | IO41NDB5V0 | IO67NDB5V0 | IO84NDB5V0 |
| G6 | GND | GND | GND |
| G7 | VCC | VCC | VCC |
| G8 | GND | GND | GND |
| G9 | VCC | VCC | VCC |
| G10 | GND | GND | GND |
| G11 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| G12 | VPP | VPP | VPP |
| G13 | TRSTB | TRSTB | TRSTB |
| G14 | TMS | TMS | TMS |
| G15 | TCK | TCK | TCK |
| G16 | GNDENVM | GNDENVM | GNDENVM |
| H1 | GND | GND | GND |
| H2 | EMC_DB[5]/IO38PPB5V0 | EMC_DB[5]/GEA1/IO61PPB5V0 | EMC_DB[5]/GEA1/IO78PPB5V0 |
| H3 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| H4 | EMC_DB[1]/IO36PDB5V0 | EMC_DB[1]/GEB2/IO59PDB5V0 | EMC_DB[1]/GEB2/IO76PDB5V0 |
| H5 | EMC_DB[0]/IO36NDB5V0 | EMC_DB[0]/GEA2/IO59NDB5V0 | EMC_DB[0]/GEA2/IO76NDB5V0 |
| H6 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| H7 | GND | GND | GND |
| H8 | VCC | VCC | VCC |
| H9 | GND | GND | GND |
| H10 | VCC | VCC | VCC |
| H11 | GND | GND | GND |
| H12 | VJTAG | VJTAG | VJTAG |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

# FG484




### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| M21 | VPP | VPP |
| M22 | IO32NDB1V0 | IO41NDB1V0 |
| N1 | GND | GND |
| N2 | NC | IO70PDB5V0 |
| N3 | NC | IO70NDB5V0 |
| N4 | VCCRCOSC | VCCRCOSC |
| N5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| N6 | NC | IO68NDB5V0 |
| N7 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| N8 | GND | GND |
| N9 | VCC | VCC |
| N10 | GND | GND |
| N11 | VCC | VCC |
| N12 | GND | GND |
| N13 | VCC | VCC |
| N14 | GND | GND |
| N15 | VCC | VCC |
| N16 | NC | GND |
| N17 | NC | NC |
| N18 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| N19 | VCCENVM | VCCENVM |
| N20 | GNDENVM | GNDENVM |
| N21 | NC | NC |
| N22 | GND | GND |
| P1 | NC | IO69NDB5V0 |
| P2 | NC | IO69PDB5V0 |
| P3 | GNDRCOSC | GNDRCOSC |
| P4 | GND | GND |
| P5 | NC | NC |
| P6 | NC | NC |
| P7 | GND | GND |
| P8 | VCC | VCC |
| P9 | GND | GND |
| P10 | VCC | VCC |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| T1 | GND | GND |
| T2 | VCCMSSIOB4 | VCCMSSIOB4 |
| T3 | GPIO_8/IO39RSB4V0 | GPIO_8/IO48RSB4V0 |
| T4 | GPIO_11/IO57RSB4V0 | GPIO_11/IO66RSB4V0 |
| T5 | GND | GND |
| T6 | MAC_CLK | MAC_CLK |
| T7 | VCCMSSIOB4 | VCCMSSIOB4 |
| T8 | VCC33SDD0 | VCC33SDD0 |
| T9 | VCC15A | VCC15A |
| T10 | GNDAQ | GNDAQ |
| T11 | GND33ADC0 | GND33ADC0 |
| T12 | ADC7 | ADC7 |
| T13 | NC | TM4 |
| T14 | NC | VAREF2 |
| T15 | VAREFOUT | VAREFOUT |
| T16 | VCCMSSIOB2 | VCCMSSIOB2 |
| T17 | SPI_1_DO/GPIO_24 | SPI_1_DO/GPIO_24 |
| T18 | GND | GND |
| T19 | NC | NC |
| T20 | NC | NC |
| T21 | VCCMSSIOB2 | VCCMSSIOB2 |
| T22 | GND | GND |
| U1 | GND | GND |
| U2 | GPIO_5/IO42RSB4V0 | GPIO_5/IO51RSB4V0 |
| U3 | GPIO_10/IO58RSB4V0 | GPIO_10/IO67RSB4V0 |
| U4 | VCCMSSIOB4 | VCCMSSIOB4 |
| U5 | MAC_RXD[1]/IO53RSB4V0 | MAC_RXD[1]/IO62RSB4V0 |
| U6 | NC | NC |
| U7 | VCC33AP | VCC33AP |
| U8 | VCC33N | VCC33N |
| U9 | CM1 | CM1 |
| U10 | VAREF0 | VAREF0 |
| U11 | GND33ADC1 | GND33ADC1 |
| U12 | ADC4 | ADC4 |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*