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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-fg256i

Package I/Os: MSS + FPGA I/Os

Device	A2F060 ¹			A2F200 ²				A2F500 ²			
Package	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Inputs	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Inputs	4	4	4	16	16	16	16	16	16	16	20
Total Analog Inputs	15	15	15	24	24	24	24	24	24	24	32
Analog Outputs	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os ^{3,4}	21 ⁵	28 ⁵	26 ⁵	22	31	25	41	22	31	25	41
FPGA I/Os	33 ⁶	68	66	66	78	66	94	66 ⁶	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:

1. There are no LVTTTL capable direct inputs available on A2F060 devices.
2. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.
3. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.
4. 9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.
5. 10/100 Ethernet MAC is not available on A2F060.
6. EMC is not available on the A2F500 PQ208 and A2F060 TQ144 package.

Table 1 • SmartFusion cSoC Package Sizes Dimensions

Package	TQ144	PQ208	CS288	FG256	FG484
Length × Width (mm\mm)	20 × 20	28 × 28	11 × 11	17 × 17	23 × 23
Nominal Area (mm ²)	400	784	121	289	529
Pitch (mm)	0.5	0.5	0.5	1.0	1.0
Height (mm)	1.40	3.40	1.05	1.60	2.23

SmartFusion cSoC Device Status

Device	Status
A2F060	Preliminary: CS288, FG256, TQ144
A2F200	Production: CS288, FG256, FG484, PQ208
A2F500	Production: CS288, FG256, FG484, PQ208

Datasheet Categories	6-14
Microsemi SoC Products Group Safety Critical, Life Support, and High-Reliability Applications Policy	6-14

Table 2-3 • Recommended Operating Conditions^{5,6}

Symbol	Parameter ¹		Commercial	Industrial	Units
T _J	Junction temperature		0 to +85	−40 to +100	°C
VCC ²	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.425 to 3.6	1.425 to 3.6	V
VPP	Programming voltage	Programming mode ³	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLLx	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCFPGAIOBx/ VCCMSSIOBx ⁵	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A ⁶	Analog clean 3.3 V supply to the analog circuitry		3.15 to 3.45	3.15 to 3.45	V
VCC33ADCx ⁶	Analog 3.3 V supply to ADC		3.15 to 3.45	3.15 to 3.45	V
VCC33AP ⁶	Analog clean 3.3 V supply to the charge pump		3.15 to 3.45	3.15 to 3.45	V
VCC33SDDx ⁶	Analog 3.3 V supply to sigma-delta DAC		3.15 to 3.45	3.15 to 3.45	V
VAREFx	Voltage reference for ADC		2.527 to 3.3	2.527 to 3.3	V
VCCRCOSC	Analog supply to the integrated RC oscillator		3.15 to 3.45	3.15 to 3.45	V
VDDBAT	External battery supply		2.7 to 3.63	2.7 to 3.63	V
VCCMAINXTAL ⁶	Analog supply to the main crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCLPXTAL ⁶	Analog supply to the low power 32 KHz crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCENVM	Embedded nonvolatile memory supply		1.425 to 1.575	1.425 to 1.575	V
VCCESRAM	Embedded SRAM supply		1.425 to 1.575	1.425 to 1.575	V
VCC15A ²	Analog 1.5 V supply to the analog circuitry		1.425 to 1.575	1.425 to 1.575	V
VCC15ADCx ²	Analog 1.5 V supply to the ADC		1.425 to 1.575	1.425 to 1.575	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.
3. The Programming temperature range supported is T_{ambient} = 0°C to 85°C.
4. VPP can be left floating during operation (not programming mode).
5. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-19 on page 2-23](#). VCCxxxIOBx should be at the same voltage within a given I/O bank.
6. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.

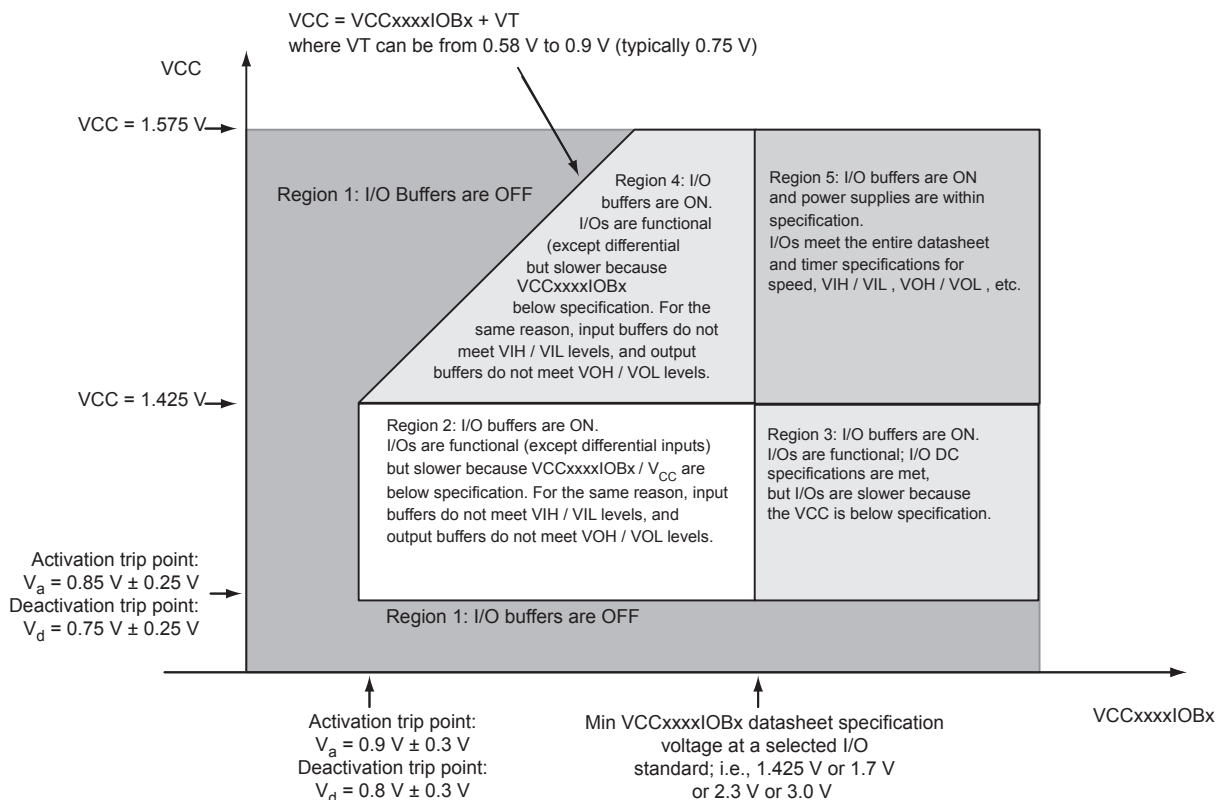


Figure 2-1 • I/O State as a Function of $VCC_{xxxxIOBx}$ and VCC Voltage Levels

Calculating Power Dissipation

Quiescent Supply Current

Table 2-8 • Power Supplies Configuration

Modes and Power Supplies	VCCxxxIOBx VCCFPGAIOBx VCCMSSIOBx	VCC33A / VCC33ADCx VCC33AP / VCC33SDDx VCCMAINXTAL / VCCLPXTAL	VCC / VCC15A / VCC15ADCx VCCPLLx, VCCENVM, VCCESRAM	VDDBAT	VCCRCOSC	VJTAG	VPP	eNVM (reset/off)	LPXTAL (enable/disable)	MAINXTAL (enable/disable)
Time Keeping mode	0 V	0 V	0 V	3.3 V	0 V	0 V	0 V	Off	Enable	Disable
Standby mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	Reset	Enable	Disable
SoC mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	On	Enable	Enable

Note: *On means proper voltage is applied. Refer to [Table 2-3 on page 2-3](#) for recommended operating conditions.

Table 2-9 • Quiescent Supply Current Characteristics

Parameter	Modes	A2F060		A2F200		A2F500	
		1.5 V Domain	3.3 V Domain	1.5 V Domain	3.3 V Domain	1.5 V Domain	3.3 V Domain
IDC1	SoC mode	3 mA	2 mA	7 mA	4 mA	16.5 mA	4 mA
IDC2	Standby mode	3 mA	2 mA	7 mA	4 mA	16.5 mA	4 mA
IDC3	Time Keeping mode	N/A	10 μ A	N/A	10 μ A	N/A	10 μ A

Power per I/O Pin

Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

	VCCFPGAIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (μ W/MHz)
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	17.55
2.5 V LVCMOS	2.5	–	5.97
1.8 V LVCMOS	1.8	–	2.88
1.5 V LVCMOS (JESD8-11)	1.5	–	2.33
3.3 V PCI	3.3	–	19.21
3.3 V PCI-X	3.3	–	19.21
Differential			
LVDS	2.5	2.26	0.82
LVPECL	3.3	5.72	1.16

Microcontroller Subsystem Dynamic Contribution— P_{MSS}

SoC Mode

$$P_{MSS} = P_{AC22}$$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots 0.78125\%) / 8$.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 2-17 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-18 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	Toggle rate of the logic driving the output buffer
β_2	FPGA fabric SRAM enable rate for read operations	12.5%
β_3	FPGA fabric SRAM enable rate for write operations	12.5%
β_4	eNVM enable rate for read operations	< 5%

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-35 • Minimum and Maximum DC Input and Output Levels
Applicable to FPGA I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	15	15
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	15	15
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-36 • Minimum and Maximum DC Input and Output Levels
Applicable to MSS I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

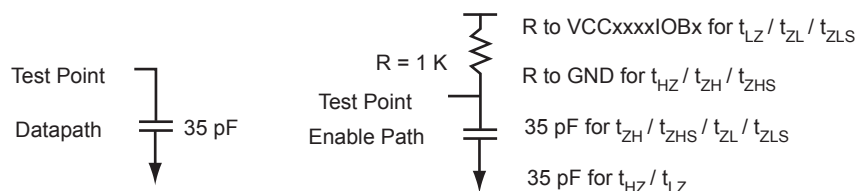


Figure 2-6 • AC Loading

Table 2-37 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	CLOAD (pF)
0	3.3	1.4	—	35

Note: *Measuring point = V_{trip} . See Table 2-22 on page 2-24 for a complete table of trip points.

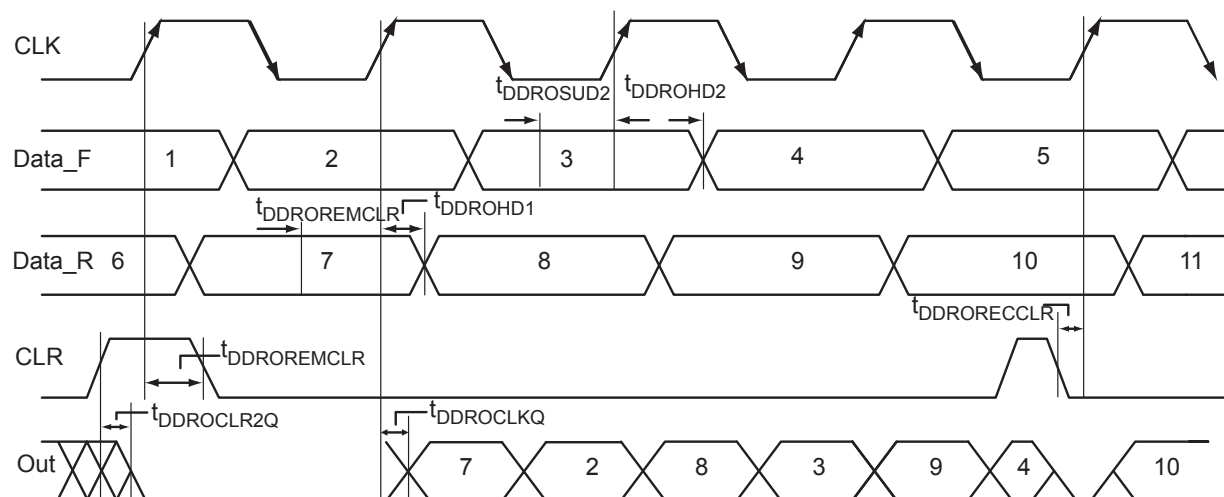


Figure 2-22 • Output DDR Timing Diagram

Timing Characteristics

Table 2-77 • Output DDR Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.71	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.38	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.38	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.81	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{\text{DDROECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	0.36	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [IGLOO/e](#), [Fusion](#), [ProASIC3/E](#), and [SmartFusion Macro Library Guide](#).

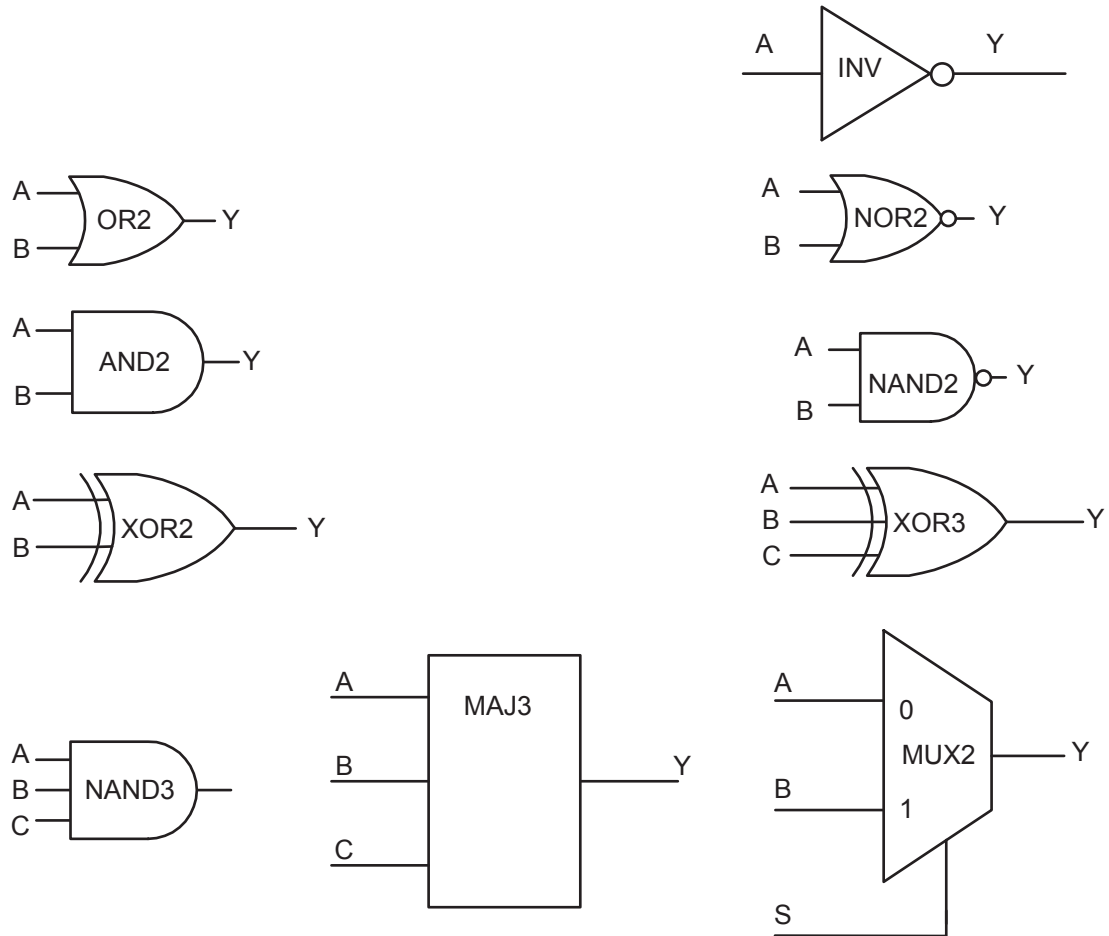


Figure 2-23 • Sample of Combinatorial Cells

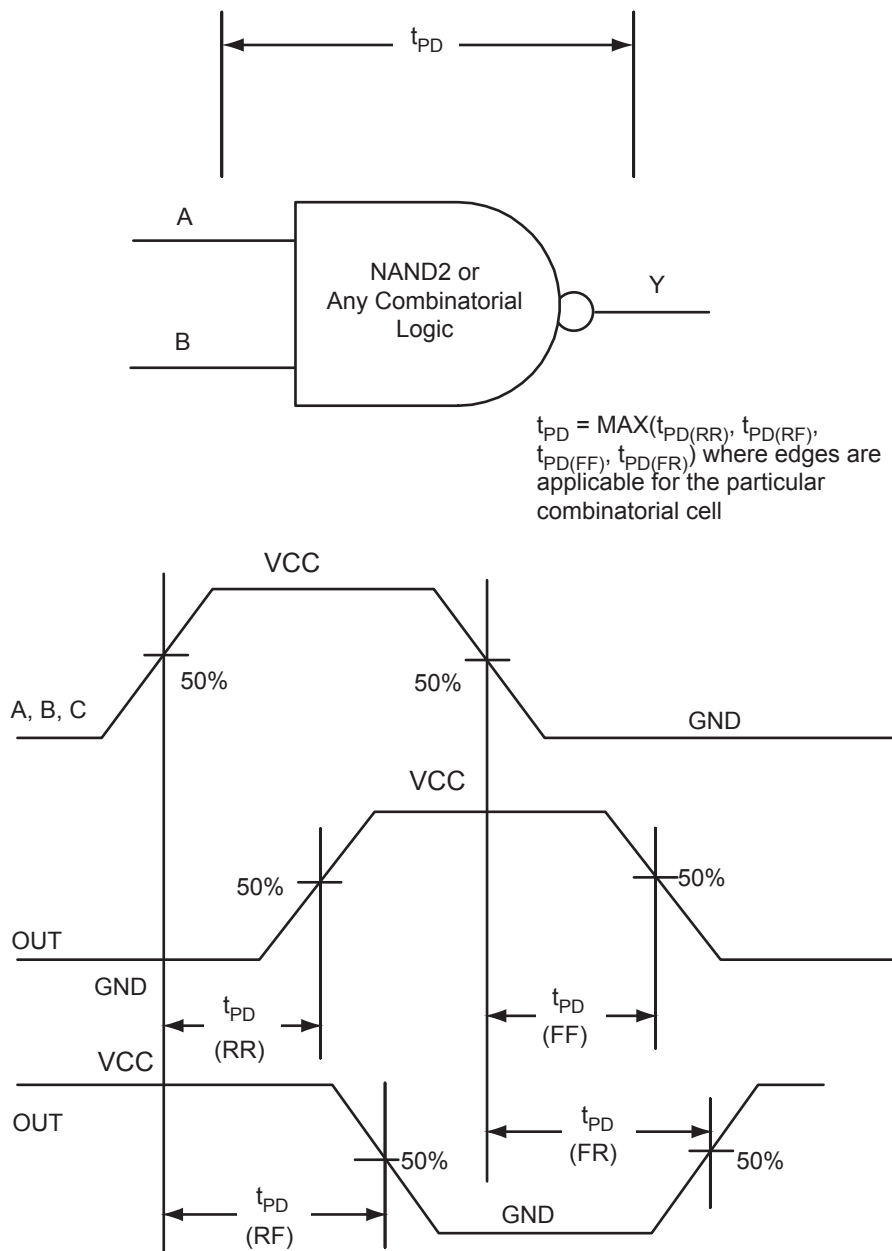


Figure 2-24 • Timing Model and Waveforms

Main and Lower Power Crystal Oscillator

The tables below describes the electrical characteristics of the main and low power crystal oscillator.

Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency	Using external crystal	0.032		20	MHz
		Using ceramic resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output duty cycle			50		%
	Output jitter	With 10 MHz crystal		1		ns RMS
IDYNXTAL	Operating current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby current of crystal oscillator			10		μA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	RC [Tested at 3.24Mhz]		300	550	μs
		0.032–0.2 [Tested at 32KHz]		500	3,000	μs
		0.2–2.0 [Tested at 2MHz]		8	12	μs
		2.0–20.0 [Tested at 20MHz]		160	180	μs

Table 2-85 • Electrical Characteristics of the Low Power Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency			32		KHz
	Output duty cycle			50		%
	Output jitter			30		ns RMS
IDYNXTAL	Operating current	32 KHz		10		μA
ISTBXTAL	Standby current of crystal oscillator			2		μA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	Test load used: 20 pF		2.5		s
		Test load used: 30 pF		3.7	13	s

Name	Type	Description
VCCFPGAIOB5	Supply	Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCLPXTAL	Supply	Analog supply to the low power 32 KHz crystal oscillator. Always power this pin. ¹
VCCMAINXTAL	Supply	Analog supply to the main crystal oscillator circuit. Always power this pin. ¹
VCCMSSIOB2	Supply	Supply voltage to the microcontroller subsystem I/O bank 2 (east MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCMSSIOB4	Supply	Supply voltage to the microcontroller subsystem I/O bank 4 (west MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCPLLx	Supply	Analog 1.5 V supply to the PLL. Always power this pin.
VCCRCOSC	Supply	Analog supply to the integrated RC oscillator circuit. Always power this pin. ¹
VCOMPLAx	Supply	Analog ground for the PLL
VDDBAT	Supply	External battery connection to the low power 32 KHz crystal oscillator (along with VCCLPXTAL), RTC, and battery switchover circuit. Can be pulled down if unused.

Notes:

1. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.
2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.
3. For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, [SmartFusion cSoC Board Design Guidelines](#), the "PLL Power Supply Decoupling Scheme" section.

TQ144	
Pin Number	A2F060 Function
73	VCC33A
74	PTEM
75	PTBASE
76	SPI_0_DO/GPIO_16
77	SPI_0_DI/GPIO_17
78	SPI_0_CLK/GPIO_18
79	SPI_0_SS/GPIO_19
80	UART_0_RXD/GPIO_21
81	UART_0_TXD/GPIO_20
82	UART_1_RXD/GPIO_29
83	UART_1_TXD/GPIO_28
84	VCC
85	VCCMSSIOB2
86	GND
87	I2C_1_SDA/GPIO_30
88	I2C_1_SCL/GPIO_31
89	I2C_0_SDA/GPIO_22
90	I2C_0_SCL/GPIO_23
91	GNDENV
92	VCCENV
93	JTAGSEL
94	TCK
95	TDI
96	TMS
97	TDO
98	TRSTB
99	VJTAG
100	VDDBAT
101	VCCLPXTAL
102	LPXOUT
103	LPXIN
104	GNDLPXTAL
105	GNDMAINXTAL
106	MAINXOUT
107	MAINXIN
108	VCCMAINXTAL

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
H19	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
H21	NC	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J3	EMC_DB[8]/IO40NPB5V0	EMC_DB[8]/GEC0/IO63NPB5V0	EMC_DB[8]/GEC0/IO80NPB5V0
J5	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
J6	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
J8	VCC	VCC	VCC
J9	GND	GND	GND
J10	VCC	VCC	VCC
J11	GND	GND	GND
J12	VCC	VCC	VCC
J13	GND	GND	GND
J14	VCC	VCC	VCC
J15	VPP	VPP	VPP
J16	NC	IO32NPB1V0	IO41NPB1V0
J17	NC	GNDQ	GNDQ
J19	VCCMAINXTAL	VCCMAINXTAL	VCCMAINXTAL
J21	NC	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
K1	GND	GND	GND
K3	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
K5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K6	EMC_DB[3]/IO37PPB5V0	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
K8	GND	GND	GND
K9	VCC	VCC	VCC
K10	GND	GND	GND
K11	VCC	VCC	VCC
K12	GND	GND	GND
K13	VCC	VCC	VCC
K14	GND	GND	GND
K16	LPXOUT	LPXOUT	LPXOUT

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

Notes:

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2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
U5	VCC33SDD0	VCC33SDD0	VCC33SDD0
U6	VCC15A	VCC15A	VCC15A
U7	NC	ABPS3	ABPS3
U8	NC	ADC2	ADC2
U9	NC	VCC33ADC0	VCC33ADC0
U10	GND15ADC0	GND15ADC1	GND15ADC1
U11	VCC33ADC0	VCC33ADC1	VCC33ADC1
U12	ADC10	ADC7	ADC7
U13	ABPS0	ABPS6	ABPS6
U14	GNDTM0	GNDTM1	GNDTM1
U15	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
U16	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
U17	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
U19	GND	GND	GND
U21	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
V1	NC	MAC_CLK	MAC_CLK
V3	GNDSD0	GNDSD0	GNDSD0
V19	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
V21	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
W1	PCAP	PCAP	PCAP
W3	NCAP	NCAP	NCAP
W4	ADC2	CM0	CM0
W5	ADC3	TM0	TM0
W6	ADC4	TM1	TM1
W7	NC	ADC0	ADC0
W8	NC	ADC3	ADC3
W9	NC	GND33ADC0	GND33ADC0
W10	VCC15ADC0	VCC15ADC1	VCC15ADC1
W11	GND33ADC0	GND33ADC1	GND33ADC1
W12	ADC8	ADC5	ADC5
W13	CM0	CM3	CM3

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Pin Number	PQ208	
	A2F200	A2F500
187	VCCFPGAIOB0	VCCFPGAIOB0
188	GND	GND
189	VCC	VCC
190	EMC_AB[5]/IO06PDB0V0	IO08PDB0V0
191	EMC_AB[4]/IO06NDB0V0	IO08NDB0V0
192	EMC_AB[3]/IO05PDB0V0	GAC1/IO07PDB0V0
193	EMC_AB[2]/IO05NDB0V0	GAC0/IO07NDB0V0
194	EMC_AB[1]/IO04PDB0V0	IO04PDB0V0
195	EMC_AB[0]/IO04NDB0V0	IO04NDB0V0
196	EMC_OEN1_N/IO03PDB0V0	IO03PDB0V0
197	EMC_OEN0_N/IO03NDB0V0	IO03NDB0V0
198	EMC_BYTEN[1]/GAC1/IO02PDB0V0	GAA1/IO02PDB0V0
199	EMC_BYTEN[0]/GAC0/IO02NDB0V0	GAA0/IO02NDB0V0
200	VCCFPGAIOB0	VCCFPGAIOB0
201	GND	GND
202	VCC	VCC
203	EMC_CS1_N/GAB1/IO01PDB0V0	IO01PDB0V0
204	EMC_CS0_N/GAB0/IO01NDB0V0	IO01NDB0V0
205	EMC_RW_N/GAA1/IO00PDB0V0	IO00PDB0V0
206	EMC_CLK/GAA0/IO00NDB0V0	IO00NDB0V0
207	VCCFPGAIOB0	VCCFPGAIOB0
208	GNDQ	GNDQ

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Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
H13	TDO	TDO	TDO
H14	TDI	TDI	TDI
H15	JTAGSEL	JTAGSEL	JTAGSEL
H16	GND	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC	GNDRCOSC
J5	NC	GNDQ	GNDQ
J6	GND	GND	GND
J7	VCC	VCC	VCC
J8	GND	GND	GND
J9	VCC	VCC	VCC
J10	GND	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND	GND
K8	VCC	VCC	VCC
K9	GND	GND	GND
K10	VCC	VCC	VCC
K11	GND	GND	GND

Notes:

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2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
AA13	NC	ADC10
AA14	NC	ADC9
AA15	NC	GND15ADC2
AA16	MAINXIN	MAINXIN
AA17	MAINXOUT	MAINXOUT
AA18	LPXIN	LPXIN
AA19	LPXOUT	LPXOUT
AA20	NC	NC
AA21	NC	NC
AA22	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
AB1	GND	GND
AB2	GPIO_13/IO36RSB4V0	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO35RSB4V0	GPIO_14/IO44RSB4V0
AB4	GND	GND
AB5	PCAP	PCAP
AB6	NCAP	NCAP
AB7	ABPS3	ABPS3
AB8	ADC3	ADC3
AB9	GND15ADC0	GND15ADC0
AB10	VCC33ADC1	VCC33ADC1
AB11	VAREF1	VAREF1
AB12	TM2	TM2
AB13	CM2	CM2
AB14	ABPS4	ABPS4
AB15	GNDQA	GNDQA
AB16	GNDMAINXTAL	GNDMAINXTAL
AB17	GNDLPXTAL	GNDLPXTAL
AB18	VCCLPXTAL	VCCLPXTAL
AB19	VDDBAT	VDDBAT
AB20	PTBASE	PTBASE
AB21	NC	NC
AB22	GND	GND
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND

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Pin Number	FG484	
	A2F200 Function	A2F500 Function
T1	GND	GND
T2	VCCMSSIOB4	VCCMSSIOB4
T3	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO57RSB4V0	GPIO_11/IO66RSB4V0
T5	GND	GND
T6	MAC_CLK	MAC_CLK
T7	VCCMSSIOB4	VCCMSSIOB4
T8	VCC33SDD0	VCC33SDD0
T9	VCC15A	VCC15A
T10	GND	GND
T11	GND33ADC0	GND33ADC0
T12	ADC7	ADC7
T13	NC	TM4
T14	NC	VAREF2
T15	VAREFOUT	VAREFOUT
T16	VCCMSSIOB2	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
T18	GND	GND
T19	NC	NC
T20	NC	NC
T21	VCCMSSIOB2	VCCMSSIOB2
T22	GND	GND
U1	GND	GND
U2	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO58RSB4V0	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4	VCCMSSIOB4
U5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
U6	NC	NC
U7	VCC33AP	VCC33AP
U8	VCC33N	VCC33N
U9	CM1	CM1
U10	VAREF0	VAREF0
U11	GND33ADC1	GND33ADC1
U12	ADC4	ADC4

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