



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-fg484">https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-fg484</a>









### 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

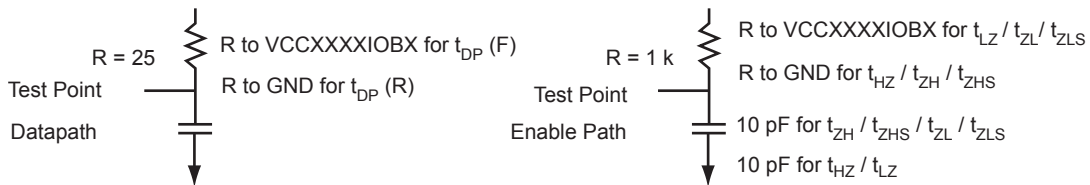
**Table 2-59 • Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
Per PCI specification	Per PCI curves										15	15

**Notes:**

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in Figure 2-10.



**Figure 2-10 • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in Table 2-60.

**Table 2-60 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V <sub>REF</sub> (typ.) (V)	C <sub>LOAD</sub> (pF)
0	3.3	0.285 * VCCxxxIOBx for t <sub>DP(R)</sub> 0.615 * VCCxxxIOBx for t <sub>DP(F)</sub>	–	10

\* Measuring point = V<sub>trip</sub>. See Table 2-22 on page 2-24 for a complete table of trip points.

### Timing Characteristics

**Table 2-61 • 3.3 V PCI**

Worst Commercial-Case Conditions: T<sub>J</sub> = 85°C, Worst-Case VCC = 1.425 V,  
Worst-Case VCCxxxIOBx = 3.0 V  
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.60	2.54	0.04	0.82	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

**Table 2-62 • 3.3 V PCI-X**

Worst Commercial-Case Conditions: T<sub>J</sub> = 85°C, Worst-Case VCC = 1.425 V,  
Worst-Case VCCxxxIOBx = 3.0 V  
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.60	2.54	0.04	0.77	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

## VersaTile Characteristics

### VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e*, *Fusion*, *ProASIC3/E*, and *SmartFusion Macro Library Guide*.

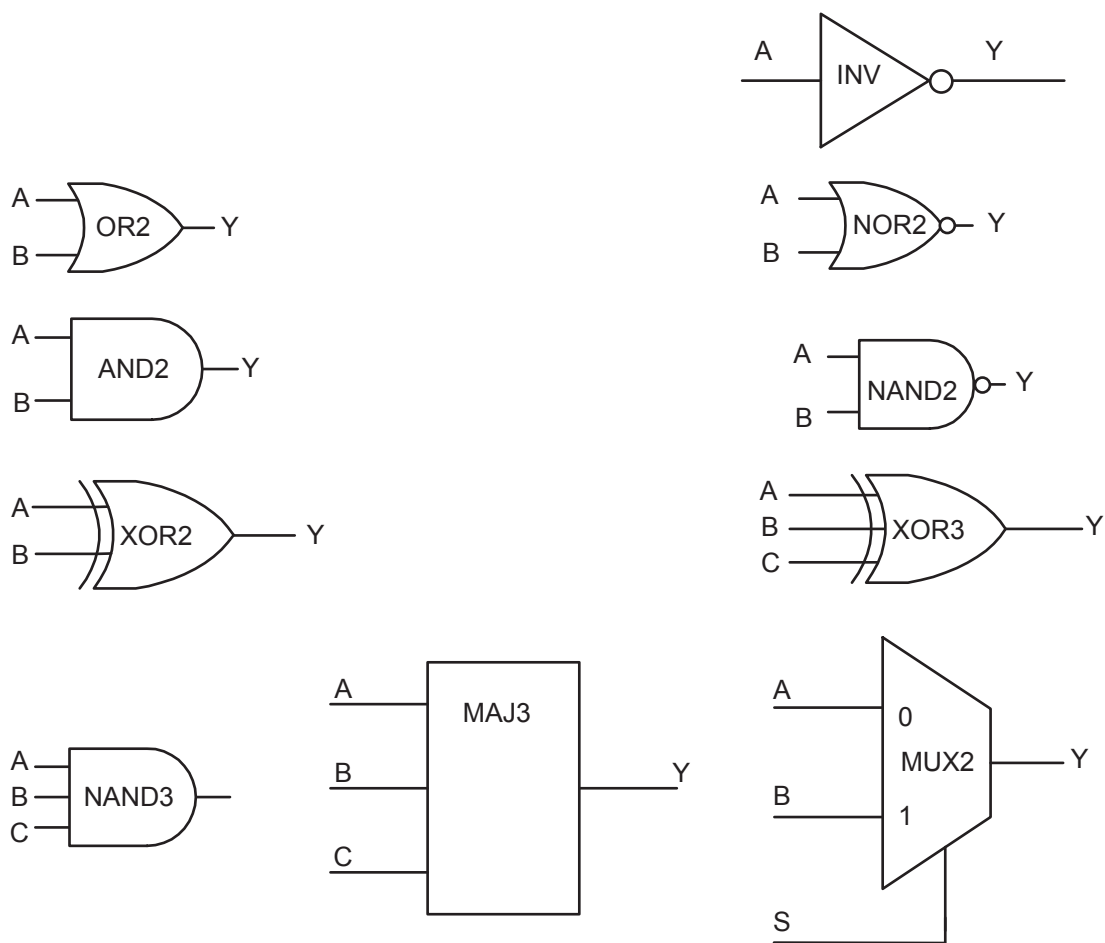
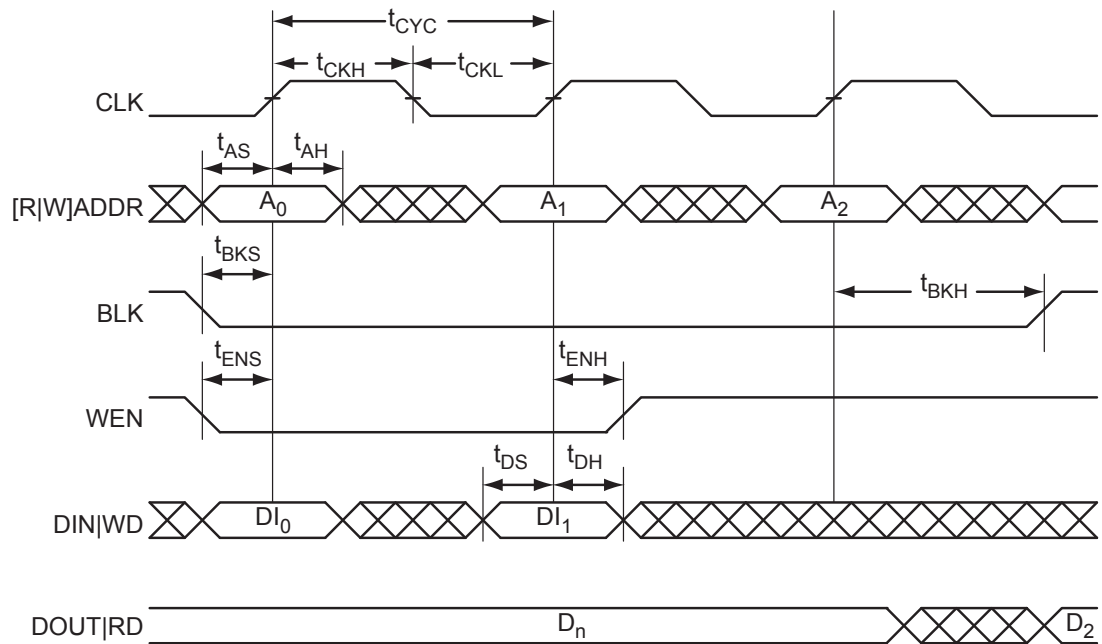
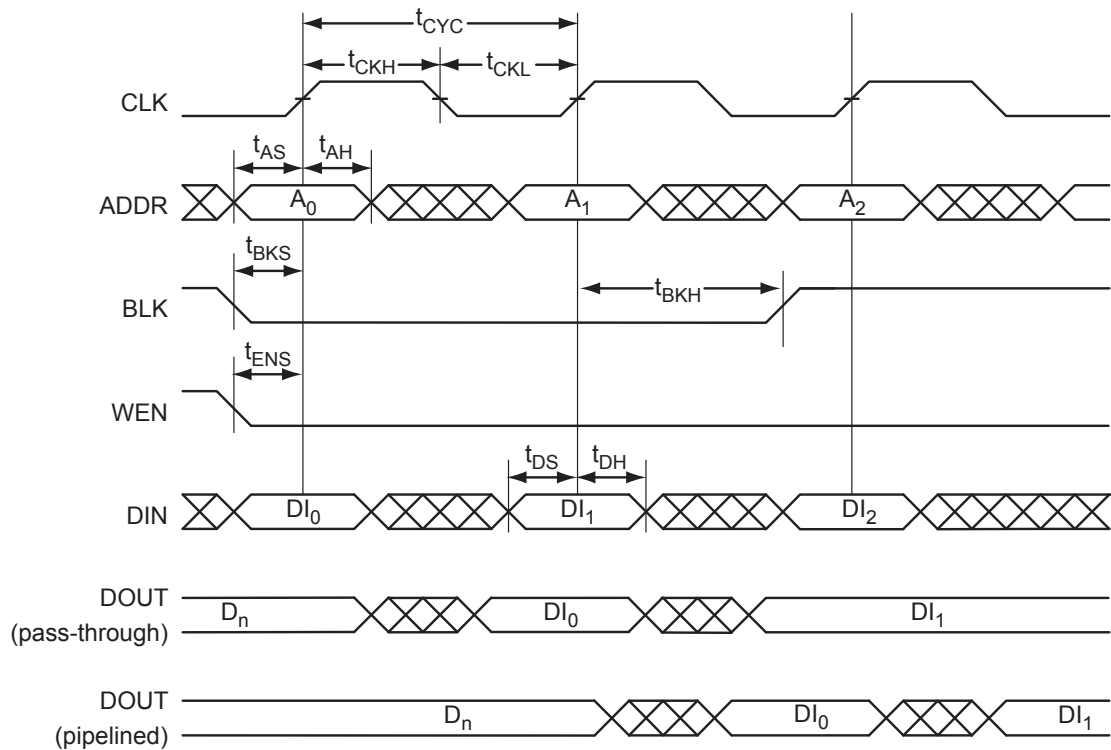


Figure 2-23 • Sample of Combinatorial Cells



**Figure 2-32 • RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.**



**Figure 2-33 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

## Timing Characteristics

**Table 2-89 • FIFO**
**Worst Commercial-Case Conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	-1	Std.	Units
$t_{ENS}$	REN, WEN Setup Time	1.40	1.68	ns
$t_{ENH}$	REN, WEN Hold Time	0.02	0.02	ns
$t_{BKS}$	BLK Setup Time	0.19	0.19	ns
$t_{BKH}$	BLK Hold Time	0.00	0.00	ns
$t_{DS}$	Input Data (WD) Setup Time	0.19	0.22	ns
$t_{DH}$	Input Data (WD) Hold Time	0.00	0.00	ns
$t_{CKQ1}$	Clock High to New Data Valid on RD (flow-through)	2.39	2.87	ns
$t_{CKQ2}$	Clock High to New Data Valid on RD (pipelined)	0.91	1.09	ns
$t_{RCKEF}$	RCLK High to Empty Flag Valid	1.74	2.09	ns
$t_{WCKFF}$	WCLK High to Full Flag Valid	1.66	1.99	ns
$t_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	6.29	7.54	ns
$t_{RSTFG}$	RESET Low to Empty/Full Flag Valid	1.72	2.06	ns
$t_{RSTAF}$	RESET Low to Almost Empty/Full Flag Valid	6.22	7.47	ns
$t_{RSTBQ}$	RESET Low to Data Out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to Data Out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET Recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.22	0.22	ns
$t_{CYC}$	Clock Cycle Time	3.28	3.28	ns
$F_{MAX}$	Maximum Frequency for FIFO	305	305	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on [page 2-9](#) for derating values.

**Table 5-1 • Recommended Tie-Off Values for the TCK and TRST Pins**

<b>VJTAG</b>	<b>Tie-Off Resistance<sup>1, 2</sup></b>
VJTAG at 3.3 V	200 $\Omega$ to 1 k $\Omega$
VJTAG at 2.5 V	200 $\Omega$ to 1 k $\Omega$
VJTAG at 1.8 V	500 $\Omega$ to 1 k $\Omega$
VJTAG at 1.5 V	500 $\Omega$ to 1 k $\Omega$

**Notes:**

1. The TCK pin can be pulled up/down.
2. The TRST pin can only be pulled down.
1. Equivalent parallel resistance if more than one device is on JTAG chain.

**Table 5-2 • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

**Notes:**

1. *ABPSx\_IN*: Input to active bipolar prescaler channel *x*.
2. *CMx\_H/L*: Current monitor channel *x*, high/low side.
3. *TMx\_IO*: Temperature monitor channel *x*.
4. *CMPx\_P/N*: Comparator channel *x*, positive/negative input.
5. *LVTTTLx\_IN*: LVTTTL I/O channel *x*.
6. *SDDMx\_OUT*: Output from sigma-delta DAC MUX channel *x*.
7. *SDDx\_OUT*: Direct output from sigma-delta DAC channel *x*.







Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
B16	GNDQ	GNDQ	GNDQ
C1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	VCCPLL0	VCCPLL	VCCPLL0
C3	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
C4	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C5	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
C6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
C7	GND	GND	GND
C8	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C9	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
C10	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C11	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C12	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C13	GND	GND	GND
C14	GCC0/IO18NPB0V0	GBA2/IO20PPB1V0	GBA2/IO27PPB1V0
C15	GCB0/IO19NDB0V0	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
C16	GCB1/IO19PDB0V0	IO23NDB1V0	IO28NDB1V0
D1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D2	VCOMPLA0	VCOMPLA	VCOMPLA0
D3	GND	GND	GND
D4	GNDQ	GNDQ	GNDQ
D5	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
D6	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
D7	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
D8	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
D9	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D10	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
D11	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
D12	GNDQ	GNDQ	GNDQ
D13	GCC1/IO18PPB0V0	GBB2/IO20NPB1V0	GBB2/IO27NPB1V0
D14	GCA0/IO20NDB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. \*: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF\_LVPECL/CLKBUF\_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
D15	GCA1/IO20PDB0V0	IO24NDB1V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E3	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ	GNDQ
E6	GND	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
E13	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND	GND
F8	VCC	VCC	VCC
F9	GND	GND	GND
F10	VCC	VCC	VCC
F11	GND	GND	GND
F12	IO22NDB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
F13	NC	GNDQ	GNDQ

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. \*: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF\_LVPECL/CLKBUF\_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
F14	IO21NDB1V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
F15	GND	GND	GND
F16	VCCENVM	VCCENVM	VCCENVM
G1	EMC_DB[8]/IO40NDB5V0	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
G2	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
G3	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
G4	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G6	GND	GND	GND
G7	VCC	VCC	VCC
G8	GND	GND	GND
G9	VCC	VCC	VCC
G10	GND	GND	GND
G11	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
G12	VPP	VPP	VPP
G13	TRSTB	TRSTB	TRSTB
G14	TMS	TMS	TMS
G15	TCK	TCK	TCK
G16	GNDENVM	GNDENVM	GNDENVM
H1	GND	GND	GND
H2	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
H3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H4	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
H5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
H6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H7	GND	GND	GND
H8	VCC	VCC	VCC
H9	GND	GND	GND
H10	VCC	VCC	VCC
H11	GND	GND	GND
H12	VJTAG	VJTAG	VJTAG

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. \*: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF\_LVPECL/CLKBUF\_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
H13	TDO	TDO	TDO
H14	TDI	TDI	TDI
H15	JTAGSEL	JTAGSEL	JTAGSEL
H16	GND	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC	GNDRCOSC
J5	NC	GNDQ	GNDQ
J6	GND	GND	GND
J7	VCC	VCC	VCC
J8	GND	GND	GND
J9	VCC	VCC	VCC
J10	GND	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND	GND
K8	VCC	VCC	VCC
K9	GND	GND	GND
K10	VCC	VCC	VCC
K11	GND	GND	GND

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. \*: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF\_LVPECL/CLKBUF\_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
AA13	NC	ADC10
AA14	NC	ADC9
AA15	NC	GND15ADC2
AA16	MAINXIN	MAINXIN
AA17	MAINXOUT	MAINXOUT
AA18	LPXIN	LPXIN
AA19	LPXOUT	LPXOUT
AA20	NC	NC
AA21	NC	NC
AA22	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
AB1	GND	GND
AB2	GPIO_13/IO36RSB4V0	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO35RSB4V0	GPIO_14/IO44RSB4V0
AB4	GND	GND
AB5	PCAP	PCAP
AB6	NCAP	NCAP
AB7	ABPS3	ABPS3
AB8	ADC3	ADC3
AB9	GND15ADC0	GND15ADC0
AB10	VCC33ADC1	VCC33ADC1
AB11	VAREF1	VAREF1
AB12	TM2	TM2
AB13	CM2	CM2
AB14	ABPS4	ABPS4
AB15	GNDAQ	GNDAQ
AB16	GNDMAINXTAL	GNDMAINXTAL
AB17	GNDLPXTAL	GNDLPXTAL
AB18	VCCLPXTAL	VCCLPXTAL
AB19	VDDBAT	VDDBAT
AB20	PTBASE	PTBASE
AB21	NC	NC
AB22	GND	GND
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. \*: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF\_LVPECL/CLKBUF\_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
L9	VCC	VCC
L10	GND	GND
L11	VCC	VCC
L12	GND	GND
L13	VCC	VCC
L14	GND	GND
L15	VCC	VCC
L16	GND	GND
L17	GNDQ	GNDQ
L18	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
L19	VCCFPGAIOB1	VCCFPGAIOB1
L20	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
L21	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
L22	GDC2/IO32PDB1V0	GDC2/IO41PDB1V0
M1	NC	IO71PDB5V0
M2	NC	IO71NDB5V0
M3	VCCFPGAIOB5	VCCFPGAIOB5
M4	NC	IO72NPB5V0
M5	GNDQ	GNDQ
M6	NC	IO68PDB5V0
M7	GND	GND
M8	VCC	VCC
M9	GND	GND
M10	VCC	VCC
M11	GND	GND
M12	VCC	VCC
M13	GND	GND
M14	VCC	VCC
M15	GND	GND
M16	VCCFPGAIOB1	VCCFPGAIOB1
M17	NC	NC
M18	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
M19	VJTAG	VJTAG
M20	GND	GND

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. \*: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF\_LVPECL/CLKBUF\_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
M21	VPP	VPP
M22	IO32NDB1V0	IO41NDB1V0
N1	GND	GND
N2	NC	IO70PDB5V0
N3	NC	IO70NDB5V0
N4	VCCRCOSC	VCCRCOSC
N5	VCCFPGAIOB5	VCCFPGAIOB5
N6	NC	IO68NDB5V0
N7	VCCFPGAIOB5	VCCFPGAIOB5
N8	GND	GND
N9	VCC	VCC
N10	GND	GND
N11	VCC	VCC
N12	GND	GND
N13	VCC	VCC
N14	GND	GND
N15	VCC	VCC
N16	NC	GND
N17	NC	NC
N18	VCCFPGAIOB1	VCCFPGAIOB1
N19	VCCENVM	VCCENVM
N20	GNDEVVM	GNDEVVM
N21	NC	NC
N22	GND	GND
P1	NC	IO69NDB5V0
P2	NC	IO69PDB5V0
P3	GNDRCOSC	GNDRCOSC
P4	GND	GND
P5	NC	NC
P6	NC	NC
P7	GND	GND
P8	VCC	VCC
P9	GND	GND
P10	VCC	VCC

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. \*: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF\_LVPECL/CLKBUF\_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the *SmartFusion Microcontroller Subsystem User's Guide* for more details.





