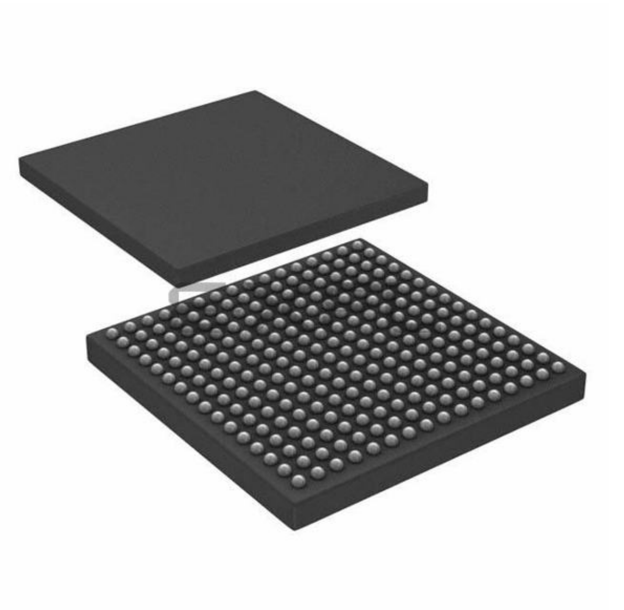

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-fgg256

Package I/Os: MSS + FPGA I/Os

Device	A2F060[1]			A2F200[2]				A2F500[2]			
Package	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Inputs	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Inputs	4	4	4	16	16	16	16	16	16	16	20
Total Analog Inputs	15	15	15	24	24	24	24	24	24	24	32
Analog Outputs	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[3,4]	21[5]	28[5]	26[5]	22	31	25	41	22	31	25	41
FPGA I/Os	33[6]	68	66	66	78	66	94	66[6]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:

1. *There are no LVTTL capable direct inputs available on A2F060 devices.*
2. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
3. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
4. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
5. *10/100 Ethernet MAC is not available on A2F060.*
6. *EMC is not available on the A2F500 PQ208 and A2F060 TQ144 package.*

Table 1 • SmartFusion cSoC Package Sizes Dimensions

Package	TQ144	PQ208	CS288	FG256	FG484
Length × Width (mm\mm)	20 × 20	28 × 28	11 × 11	17 × 17	23 × 23
Nominal Area (mm^2)	400	784	121	289	529
Pitch (mm)	0.5	0.5	0.5	1.0	1.0
Height (mm)	1.40	3.40	1.05	1.60	2.23

SmartFusion cSoC Device Status

Device	Status
A2F060	Preliminary: CS288, FG256, TQ144
A2F200	Production: CS288, FG256, FG484, PQ208
A2F500	Production: CS288, FG256, FG484, PQ208

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the A2F200-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 19.00°C/W (taken from Table 2-6 on page 2-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an A2F200-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W

θ_{JC} = 8.28°C/W

Table 2-24 • **Summary of I/O Timing Characteristics—Software Default Settings**
–1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard)
Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
2.5 V LVCMOS	12 mA	High	35	–	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
1.8 V LVCMOS	12 mA	High	35	–	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
1.5 V LVCMOS	12 mA	High	35	–	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
3.3 V PCI	Per PCI spec	High	10	25[1]	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25[1]	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns
LVDS	24 mA	High	–	–	0.50	1.53	0.03	1.55	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.50	1.46	0.03	1.46	–	–	–	–	–	–	–	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-25 • **Summary of I/O Timing Characteristics—Software Default Settings**
–1 Speed Grade, Worst Commercial-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard)
Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns
2.5 V LVCMOS	8 mA	High	10	–	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns
1.8 V LVCMOS	4 mA	High	10	–	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns
1.5 V LVCMOS	2 mA	High	10	–	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-39 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Timing Characteristics

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	7.20	0.04	0.97	0.39	7.34	6.18	2.52	2.46	9.39	8.23	ns
	–1	0.50	6.00	0.03	0.81	0.32	6.11	5.15	2.10	2.05	7.83	6.86	ns
8 mA	Std.	0.60	4.64	0.04	0.97	0.39	4.73	3.84	2.85	3.02	6.79	5.90	ns
	–1	0.50	3.87	0.03	0.81	0.32	3.94	3.20	2.37	2.52	5.65	4.91	ns
12 mA	Std.	0.60	3.37	0.04	0.97	0.39	3.43	2.67	3.07	3.39	5.49	4.73	ns
	–1	0.50	2.81	0.03	0.81	0.32	2.86	2.23	2.55	2.82	4.58	3.94	ns
16 mA	Std.	0.60	3.18	0.04	0.97	0.39	3.24	2.43	3.11	3.48	5.30	4.49	ns
	–1	0.50	2.65	0.03	0.81	0.32	2.70	2.03	2.59	2.90	4.42	3.74	ns
24 mA	Std.	0.60	2.93	0.04	0.97	0.39	2.99	2.03	3.17	3.83	5.05	4.09	ns
	–1	0.50	2.45	0.03	0.81	0.32	2.49	1.69	2.64	3.19	4.21	3.41	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	9.75	0.04	0.97	0.39	9.93	8.22	2.52	2.31	11.99	10.28	ns
	–1	0.50	8.12	0.03	0.81	0.32	8.27	6.85	2.10	1.93	9.99	8.57	ns
8 mA	Std.	0.60	6.96	0.04	0.97	0.39	7.09	5.85	2.84	2.87	9.15	7.91	ns
	–1	0.50	5.80	0.03	0.81	0.32	5.91	4.88	2.37	2.39	7.62	6.59	ns
12 mA	Std.	0.60	5.35	0.04	0.97	0.39	5.45	4.58	3.06	3.23	7.51	6.64	ns
	–1	0.50	4.46	0.03	0.81	0.32	4.54	3.82	2.55	2.69	6.26	5.53	ns
16 mA	Std.	0.60	5.01	0.04	0.97	0.39	5.10	4.30	3.11	3.32	7.16	6.36	ns
	–1	0.50	4.17	0.03	0.81	0.32	4.25	3.58	2.59	2.77	5.97	5.30	ns
24 mA	Std.	0.60	4.67	0.04	0.97	0.39	4.75	4.28	3.16	3.66	6.81	6.34	ns
	–1	0.50	3.89	0.03	0.81	0.32	3.96	3.57	2.64	3.05	5.68	5.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-40 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.31	0.09	0.94	1.30	0.22	2.35	1.86	2.20	2.45	ns
	–1	0.18	1.92	0.07	0.78	1.09	0.18	1.96	1.55	1.83	2.04	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Timing Characteristics

Table 2-50 **• 1.8 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.06	0.04	1.14	0.39	8.61	11.06	2.61	1.59	10.67	13.12	ns
	–1	0.50	9.22	0.03	0.95	0.32	7.17	9.22	2.18	1.33	8.89	10.93	ns
4 mA	Std.	0.60	6.46	0.04	1.14	0.39	5.53	6.46	3.04	2.66	7.59	8.51	ns
	–1	0.50	5.38	0.03	0.95	0.32	4.61	5.38	2.54	2.22	6.33	7.10	ns
6 mA	Std.	0.60	4.16	0.04	1.14	0.39	3.99	4.16	3.34	3.18	6.05	6.22	ns
	–1	0.50	3.47	0.03	0.95	0.32	3.32	3.47	2.78	2.65	5.04	5.18	ns
8 mA	Std.	0.60	3.69	0.04	1.14	0.39	3.76	3.67	3.40	3.31	5.81	5.73	ns
	–1	0.50	3.07	0.03	0.95	0.32	3.13	3.06	2.84	2.76	4.85	4.78	ns
12 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns
16 mA	Std.	0.60	3.38	0.04	1.14	0.39	3.44	2.86	3.50	3.82	5.50	4.91	ns
	–1	0.50	2.81	0.03	0.95	0.32	2.87	2.38	2.92	3.18	4.58	4.10	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-51 **• 1.8 V LVCMOS Low Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	14.24	0.04	1.14	0.39	13.47	14.24	2.62	1.54	15.53	16.30	ns
	–1	0.50	11.87	0.03	0.95	0.32	11.23	11.87	2.18	1.28	12.94	13.59	ns
4 mA	Std.	0.60	9.74	0.04	1.14	0.39	9.92	9.62	3.05	2.57	11.98	11.68	ns
	–1	0.50	8.11	0.03	0.95	0.32	8.26	8.02	2.54	2.14	9.98	9.74	ns
6 mA	Std.	0.60	7.67	0.04	1.14	0.39	7.81	7.24	3.34	3.08	9.87	9.30	ns
	–1	0.50	6.39	0.03	0.95	0.32	6.51	6.03	2.79	2.56	8.23	7.75	ns
8 mA	Std.	0.60	7.15	0.04	1.14	0.39	7.29	6.75	3.41	3.21	9.34	8.80	ns
	–1	0.50	5.96	0.03	0.95	0.32	6.07	5.62	2.84	2.68	7.79	7.34	ns
12 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns
16 mA	Std.	0.60	6.76	0.04	1.14	0.39	6.89	6.75	3.50	3.70	8.95	8.81	ns
	–1	0.50	5.64	0.03	0.95	0.32	5.74	5.62	2.92	3.08	7.46	7.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

***Table 2-52* • 1.8 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	Std.	0.22	2.77	0.09	1.09	1.64	0.22	2.82	2.72	2.21	2.25	ns
	–1	0.18	2.31	0.07	0.91	1.37	0.18	2.35	2.27	1.84	1.87	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-69 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-14 on page 2-44 for more information.*

Timing Waveforms

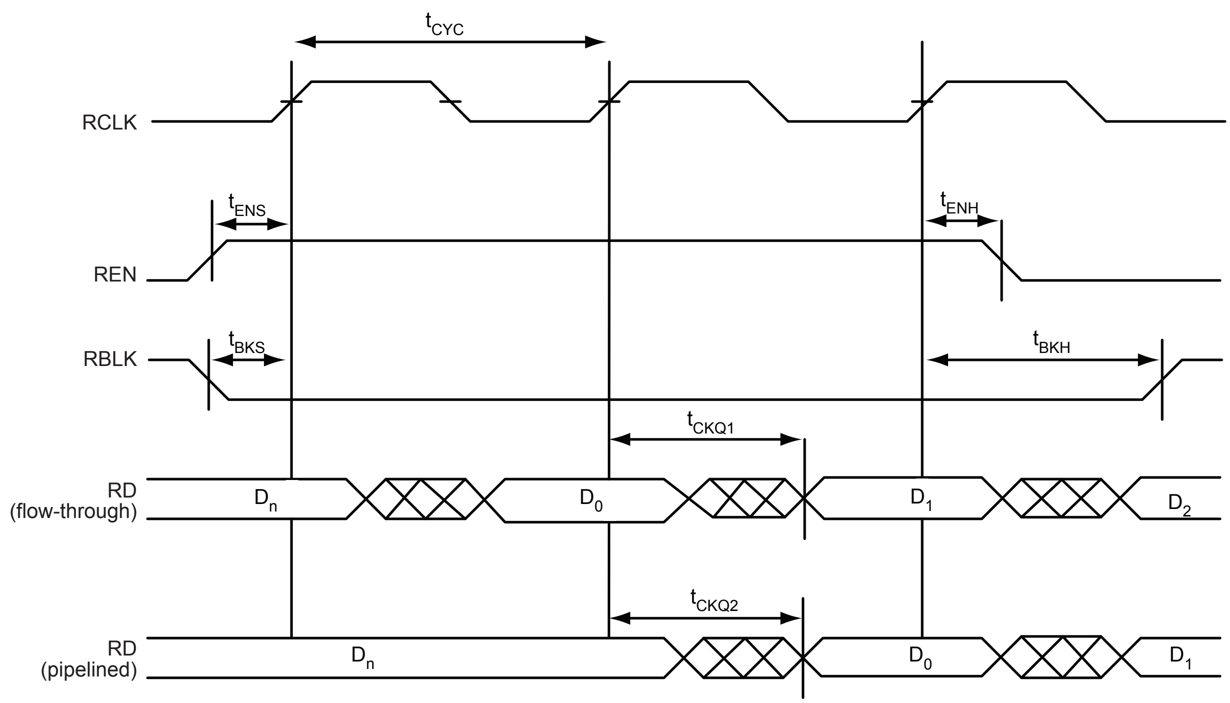

***Figure 2-36* • FIFO Read**

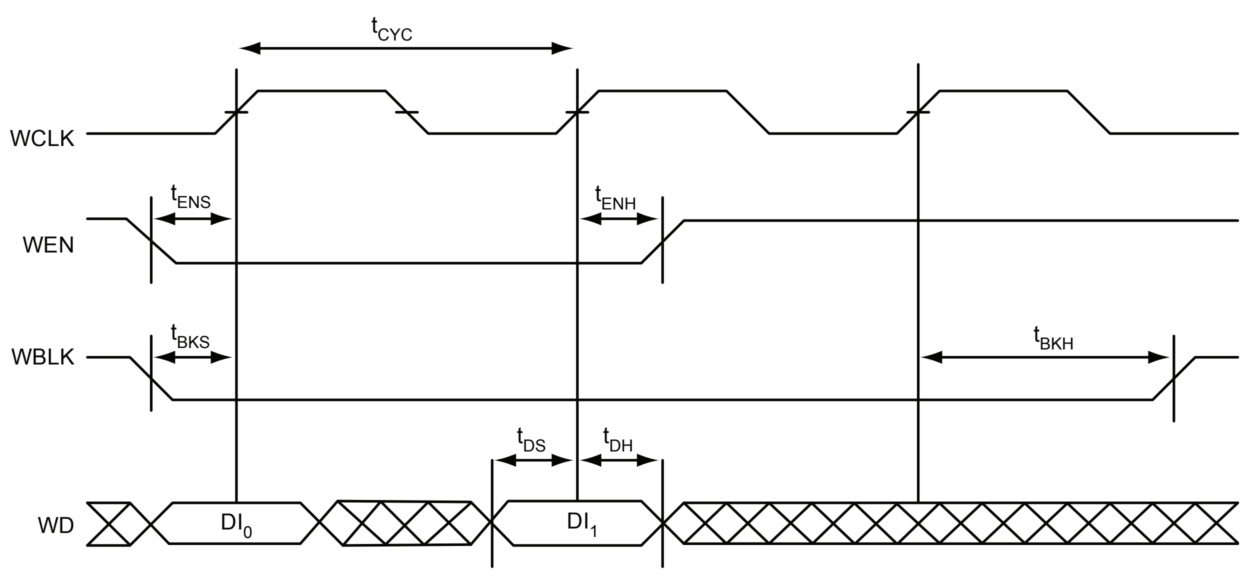

***Figure 2-37* • FIFO Write**

***Table 2-95* • ADC Specifications (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

***Table 2-96* • ABPS Performance Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

4 – SmartFusion Programming

SmartFusion cSoCs have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
   a. A2F060 and A2F500: The FPGA fabric, eNVM, and eFROM
   b. A2F200: Only the FPGA fabric and the eNVM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. Table 4-1 describes the JTAG programming hardware that will program a SmartFusion cSoC and Table 4-2 defines the JTAG pins that provide the interface for the programming hardware.

Table 4-1 **• Supported JTAG Programming Hardware**

Dongle	Source	JTAG	SWD[1]	SWV[2]	Program FPGA	Program eFROM	Program eNVM
FlashPro3/4	SoC Products Group	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes

Notes:

1. *SWD = ARM Serial Wire Debug*
2. *SWV = ARM Serial Wire Viewer*
3. *Planned support*

Table 4-2 **• JTAG Pin Descriptions**

Pin Name	Description
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

Analog Front-End (AFE)

Name	Type	Description	Associated With	
			ADC/SDD	SCB
ABPS0	In	SCB 0 / active bipolar prescaler input 1. See the Active Bipolar Prescaler (ABPS) section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ABPS1	In	SCB 0 / active bipolar prescaler Input 2	ADC0	SCB0
ABPS2	In	SCB 1 / active bipolar prescaler Input 1	ADC0	SCB1
ABPS3	In	SCB 1 / active bipolar prescaler Input 2	ADC0	SCB1
ABPS4	In	SCB 2 / active bipolar prescaler Input 1	ADC1	SCB2
ABPS5	In	SCB 2 / active bipolar prescaler Input 2	ADC1	SCB2
ABPS6	In	SCB 3 / active bipolar prescaler Input 1	ADC1	SCB3
ABPS7	In	SCB 3 / active bipolar prescaler input 2	ADC1	SCB3
ABPS8	In	SCB 4 / active bipolar prescaler input 1	ADC2	SCB4
ABPS9	In	SCB 4 / active bipolar prescaler input 2	ADC2	SCB4
ADC0	In	ADC 0 direct input 0 / FPGA Input. See the "Sigma-Delta Digital-to-Analog Converter (DAC)" section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ADC1	In	ADC 0 direct input 1 / FPGA input	ADC0	SCB0
ADC2	In	ADC 0 direct input 2 / FPGA input	ADC0	SCB1
ADC3	In	ADC 0 direct input 3 / FPGA input	ADC0	SCB1
ADC4	In	ADC 1 direct input 0 / FPGA input	ADC1	SCB2
ADC5	In	ADC 1 direct input 1 / FPGA input	ADC1	SCB2
ADC6	In	ADC 1 direct input 2 / FPGA input	ADC1	SCB3
ADC7	In	ADC 1 direct input 3 / FPGA input	ADC1	SCB3
ADC8	In	ADC 2 direct input 0 / FPGA input	ADC2	SCB4
ADC9	In	ADC 2 direct input 1 / FPGA input	ADC2	SCB4
ADC10	In	ADC 2 direct input 2 / FPGA input	ADC2	N/A
ADC11	In	ADC 2 direct input 3 / FPGA input	ADC2	N/A
CM0	In	SCB 0 / high side of current monitor / comparator Positive input. See the Current Monitor section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
CM1	In	SCB 1 / high side of current monitor / comparator. Positive input.	ADC0	SCB1
CM2	In	SCB 2 / high side of current monitor / comparator. Positive input.	ADC1	SCB2
CM3	In	SCB 3 / high side of current monitor / comparator. Positive input.	ADC1	SCB3
CM4	In	SCB 4 / high side of current monitor / comparator. Positive input.	ADC2	SCB4

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Pin No.	CS288		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
A1	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A2	GNDQ	GNDQ	GNDQ
A3	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
A4	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
A5	GND	GND	GND
A6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
A7	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
A8	EMC_AB[0]/IO04NPB0V0	EMC_AB[0]/IO04NPB0V0	EMC_AB[0]/IO06NPB0V0
A9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A10	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
A11	EMC_AB[8]/IO08NPB0V0	EMC_AB[8]/IO08NPB0V0	EMC_AB[8]/IO13NPB0V0
A12	EMC_AB[14]/IO11NPB0V0	EMC_AB[14]/IO11NPB0V0	EMC_AB[14]/IO15NPB0V0
A13	GND	GND	GND
A14	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
A15	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
A17	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A18	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A19	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
A20	GNDQ	GNDQ	GNDQ
A21	GND	GND	GND
AA1	ADC1	ABPS1	ABPS1
AA2	GNDAQ	GNDAQ	GNDAQ
AA3	GNDA	GNDA	GNDA
AA4	VCC33N	VCC33N	VCC33N
AA5	SDD0	SDD0	SDD0
AA6	ADC0	ABPS0	ABPS0
AA7	NC	GNDTM0	GNDTM0
AA8	NC	ABPS2	ABPS2
AA9	NC	VAREF0	VAREF0
AA10	NC	GND15ADC0	GND15ADC0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
63	TM1	TM1
64	CM1	CM1
65	ABPS3	ABPS3
66	ABPS2	ABPS2
67	ADC0	ADC0
68	ADC1	ADC1
69	ADC2	ADC2
70	ADC3	ADC3
71	VAREF0	VAREF0
72	GND33ADC0	GND33ADC0
73	VCC33ADC0	VCC33ADC0
74	GND33ADC0	GND33ADC0
75	VCC15ADC0	VCC15ADC0
76	GND15ADC0	GND15ADC0
77	GND15ADC1	GND15ADC1
78	VCC15ADC1	VCC15ADC1
79	GND33ADC1	GND33ADC1
80	VCC33ADC1	VCC33ADC1
81	GND33ADC1	GND33ADC1
82	VAREF1	VAREF1
83	ADC7	ADC7
84	ADC6	ADC6
85	ADC5	ADC5
86	ADC4	ADC4
87	ABPS6	ABPS6
88	ABPS7	ABPS7
89	CM3	CM3
90	TM3	TM3
91	GNDTM1	GNDTM1
92	TM2	TM2
93	CM2	CM2

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
H13	TDO	TDO	TDO
H14	TDI	TDI	TDI
H15	JTAGSEL	JTAGSEL	JTAGSEL
H16	GND	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC	GNDRCOSC
J5	NC	GNDQ	GNDQ
J6	GND	GND	GND
J7	VCC	VCC	VCC
J8	GND	GND	GND
J9	VCC	VCC	VCC
J10	GND	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND	GND
K8	VCC	VCC	VCC
K9	GND	GND	GND
K10	VCC	VCC	VCC
K11	GND	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
M11	ADC6	TM2	TM2
M12	ADC5	CM2	CM2
M13	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
M14	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
M15	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
M16	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
N1	GPIO_8/IO25RSB4V0	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
N2	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
N3	VCC15A	VCC15A	VCC15A
N4	VCC33AP	VCC33AP	VCC33AP
N5	NC	ABPS3	ABPS3
N6	ADC4	TM1	TM1
N7	NC	GND33ADC0	GND33ADC0
N8	VCC33ADC0	VCC33ADC1	VCC33ADC1
N9	ADC8	ADC5	ADC5
N10	CM0	CM3	CM3
N11	GNDAQ	GNDAQ	GNDAQ
N12	VAREFOUT	VAREFOUT	VAREFOUT
N13	NC	GNDSDD1	GNDSDD1
N14	NC	VCC33SDD1	VCC33SDD1
N15	GND	GND	GND
N16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
P1	GNDSDD0	GNDSDD0	GNDSDD0
P2	VCC33SDD0	VCC33SDD0	VCC33SDD0
P3	VCC33N	VCC33N	VCC33N
P4	GNDA	GNDA	GNDA
P5	GNDAQ	GNDAQ	GNDAQ
P6	NC	CM1	CM1
P7	NC	ADC2	ADC2
P8	NC	VCC15ADC0	VCC15ADC0
P9	ADC9	ADC6	ADC6

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 0 (continued)	"SmartFusion Development Tools" section was replaced with new content.	3-1
	The pin description tables were revised by adding additional pins to reflect the pinout for A2F500.	5-1 through 5-16
	The descriptions for "GNDSDD1" and "VCC33SDD1" were revised.	5-1, 5-2
	The description for "VCC33A" was revised.	5-2
	The pin tables for the "FG256" and "FG484" were replaced with tables that compare pin functions across densities for each package.	5-42
Draft B (December 2009)	The "Digital I/Os" section was renamed to the "I/Os and Operating Voltage" section and information was added regarding digital and analog VCC.	I
	The "SmartFusion cSoC Family Product Table" and "Package I/Os: MSS + FPGA I/Os" section were revised.	II
	The terminology for the analog blocks was changed to "programmable analog," consisting of two blocks: the analog front-end and analog compute engine. This is reflected throughout the text and in the "SmartFusion cSoC Block Diagram".	IV
	The "Product Ordering Codes" table was revised to add G as an ordering code for eNVM size.	VI
	Timing tables were populated with information that has become available for speed grade –1.	N/A
	All occurrences of the VMV parameter were removed.	N/A
	The SDD[n] voltage parameter was removed from Table 2-2 • Analog Maximum Ratings.	2-2
	Table 36-4 • Flash Programming Limits – Retention, Storage and Operating Temperature was replaced with Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits.	2-4
	The "Thermal Characteristics" section was revised extensively.	2-7
	Table 2-8 • Power Supplies Configuration was revised significantly.	2-10
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs were updated.	2-12
	Figure 2-2 • Timing Model was updated.	2-19
	The temperature associated with the reliability for LVTTL/LVCMOS in Table 2-34 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was changed from 110º to 100º.	2-29
	The values in Table 2-78 • Combinatorial Cell Propagation Delays were updated.	2-57
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator is new. Table 2-84 • Electrical Characteristics of the Main Crystal Oscillator was revised.	2-62
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V and Table 2-91 • FlashROM Access Time, Worse Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V are new.	2-76
	The performance tables in the "Programmable Analog Specifications" section were revised, including new data available. Table 2-98 • Analog Sigma-Delta DAC is new.	2-78
	The "256-Pin FBGA" table for A2F200 is new.	4-15

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