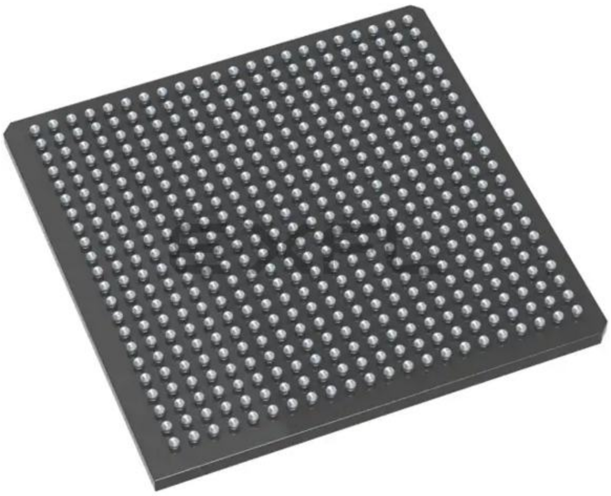

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-fgg484i

Package I/Os: MSS + FPGA I/Os

Device	A2F060[1]			A2F200[2]				A2F500[2]			
Package	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Inputs	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Inputs	4	4	4	16	16	16	16	16	16	16	20
Total Analog Inputs	15	15	15	24	24	24	24	24	24	24	32
Analog Outputs	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[3,4]	21[5]	28[5]	26[5]	22	31	25	41	22	31	25	41
FPGA I/Os	33[6]	68	66	66	78	66	94	66[6]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:

1. *There are no LVTTL capable direct inputs available on A2F060 devices.*
2. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
3. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
4. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
5. *10/100 Ethernet MAC is not available on A2F060.*
6. *EMC is not available on the A2F500 PQ208 and A2F060 TQ144 package.*

Table 1 • SmartFusion cSoC Package Sizes Dimensions

Package	TQ144	PQ208	CS288	FG256	FG484
Length × Width (mm\mm)	20 × 20	28 × 28	11 × 11	17 × 17	23 × 23
Nominal Area (mm^2)	400	784	121	289	529
Pitch (mm)	0.5	0.5	0.5	1.0	1.0
Height (mm)	1.40	3.40	1.05	1.60	2.23

SmartFusion cSoC Device Status

Device	Status
A2F060	Preliminary: CS288, FG256, TQ144
A2F200	Production: CS288, FG256, FG484, PQ208
A2F500	Production: CS288, FG256, FG484, PQ208

VCCxxxxIOBx Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to "Specifying I/O States During Programming" on page 1-3.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

Microcontroller Subsystem Dynamic Contribution—P_{MSS}

SoC Mode

$P_{MSS} = P_{AC22}$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

***Table 2-17* • Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

***Table 2-18* • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	Toggle rate of the logic driving the output buffer
β_2	FPGA fabric SRAM enable rate for read operations	12.5%
β_3	FPGA fabric SRAM enable rate for write operations	12.5%
β_4	eNVM enable rate for read operations	< 5%

Table 2-28 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to MSS I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	8mA	50	150
2.5 V LVCMOS	8 mA	50	100
1.8 V LVCMOS	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website.*
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-29 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCxxxxIOBx	$R_{(WEAK\ PULL-UP)}$[1] (Ω)		$R_{(WEAK\ PULL-DOWN)}$[2] (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL-UP-MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL-UP-MIN)}$
2. $R_{(WEAK\ PULL-DOWN-MAX)} = (VOLspec) / I_{(WEAK\ PULL-DOWN-MIN)}$

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

***Table 2-41* • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

***Table 2-42* • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

2.5 V LVCMOS	VIL		V_{IH}		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max., mA[1]	μA[2]	μA[2]
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

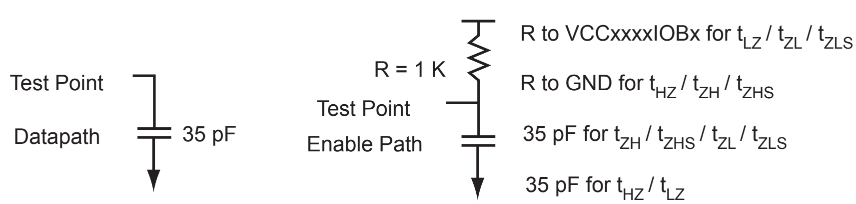

***Figure 2-7* • AC Loading**

***Table 2-43* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

* *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-44 • **2.5 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	8.10	0.04	1.23	0.39	7.37	8.10	2.54	2.17	9.43	10.15	ns
	–1	0.46	6.75	0.03	1.03	0.32	6.14	6.75	2.12	1.81	7.85	8.46	ns
8 mA	Std.	0.55	4.85	0.04	1.23	0.39	4.76	4.85	2.90	2.83	6.82	6.91	ns
	–1	0.46	4.04	0.03	1.03	0.32	3.97	4.04	2.42	2.36	5.68	5.76	ns
12 mA	Std.	0.60	3.28	0.04	1.23	0.39	3.46	3.23	3.15	3.24	5.52	5.29	ns
	–1	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
16 mA	Std.	0.60	3.09	0.04	1.23	0.39	3.27	2.88	3.20	3.35	5.33	4.94	ns
	–1	0.50	2.57	0.03	1.03	0.32	2.72	2.40	2.67	2.79	4.44	4.12	ns
24 mA	Std.	0.60	2.95	0.04	1.23	0.39	3.01	2.31	3.27	3.76	5.07	4.37	ns
	–1	0.50	2.46	0.03	1.03	0.32	2.51	1.93	2.73	3.13	4.22	3.64	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-45 • **2.5 V LVCMOS Low Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	10.50	0.04	1.23	0.39	10.69	10.50	2.54	2.07	12.75	12.56	ns
	–1	0.46	8.75	0.03	1.03	0.32	8.91	8.75	2.12	1.73	10.62	10.47	ns
8 mA	Std.	0.55	7.61	0.04	1.23	0.39	7.46	7.19	2.81	2.66	9.52	9.25	ns
	–1	0.46	6.34	0.03	1.03	0.32	6.22	5.99	2.34	2.22	7.93	7.71	ns
12 mA	Std.	0.60	5.92	0.04	1.23	0.39	5.79	5.45	3.04	3.06	7.85	7.51	ns
	–1	0.50	4.93	0.03	1.03	0.32	4.83	4.54	2.53	2.55	6.54	6.26	ns
16 mA	Std.	0.60	5.53	0.04	1.23	0.39	5.40	5.09	3.09	3.16	7.46	7.14	ns
	–1	0.50	4.61	0.03	1.03	0.32	4.50	4.24	2.58	2.64	6.22	5.95	ns
24 mA	Std.	0.60	5.18	0.04	1.23	0.39	5.28	5.14	3.27	3.64	7.34	7.20	ns
	–1	0.50	4.32	0.03	1.03	0.32	4.40	4.29	2.72	3.03	6.11	6.00	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-46 • **2.5 V LVCMOS High Slew**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.35	0.09	1.18	1.39	0.22	2.40	2.18	2.19	2.32	ns
	–1	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Output Register

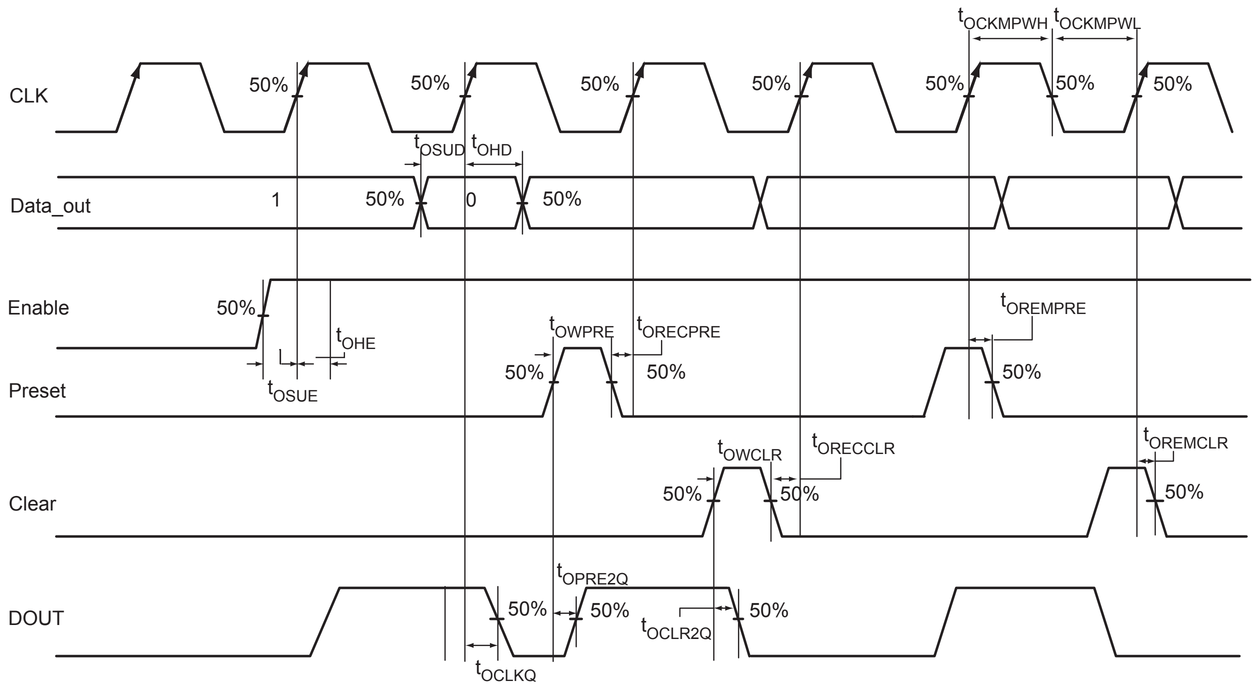

Figure 2-17 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-72 • **Output Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.72	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.38	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.98	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.98	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

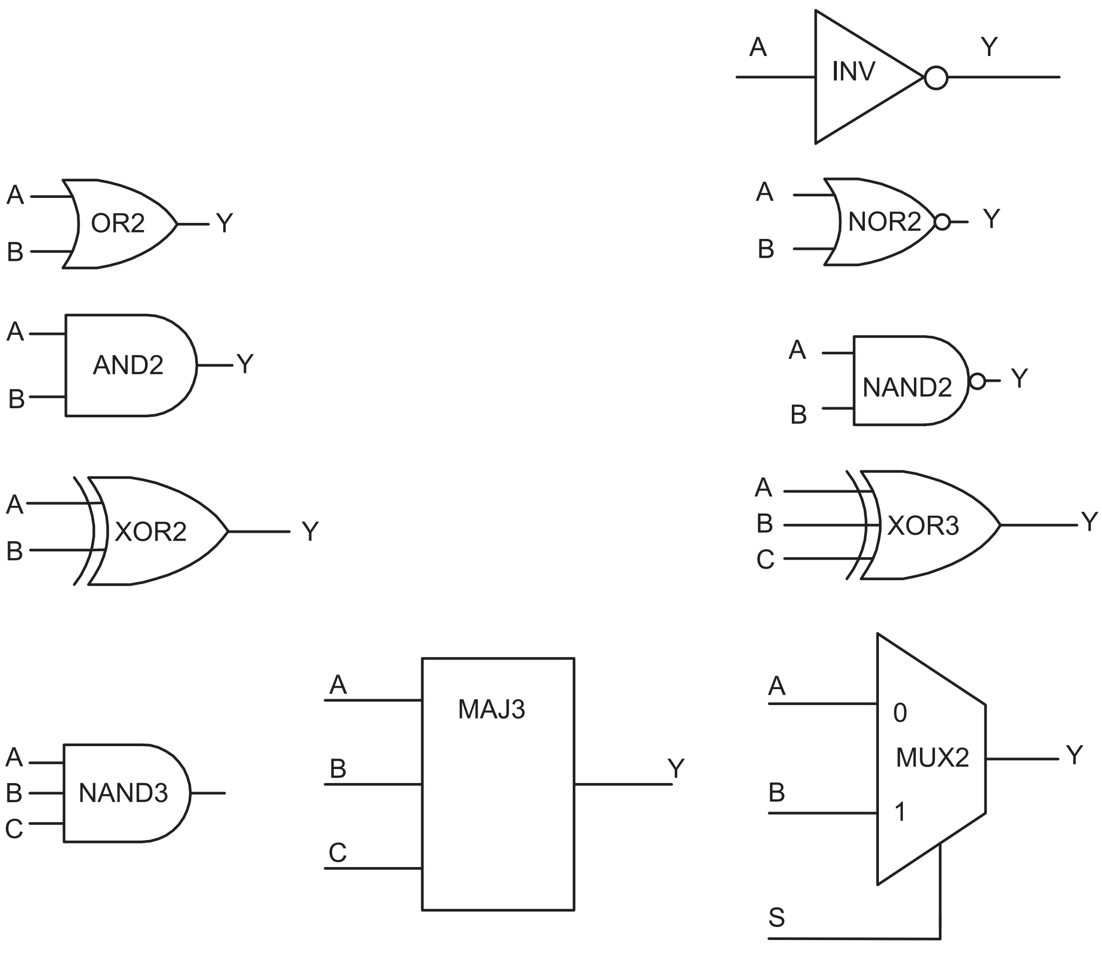

Figure 2-23 • **Sample of Combinatorial Cells**

***Table 2-88* • RAM512X18**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.22	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.19	2.63	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.91	1.09	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.38	0.43	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.44	0.50	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to data out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.22	ns
t_{CYC}	Clock cycle time	3.28	3.28	ns
F_{MAX}	Maximum clock frequency	305	305	MHz

Notes:

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

FIFO

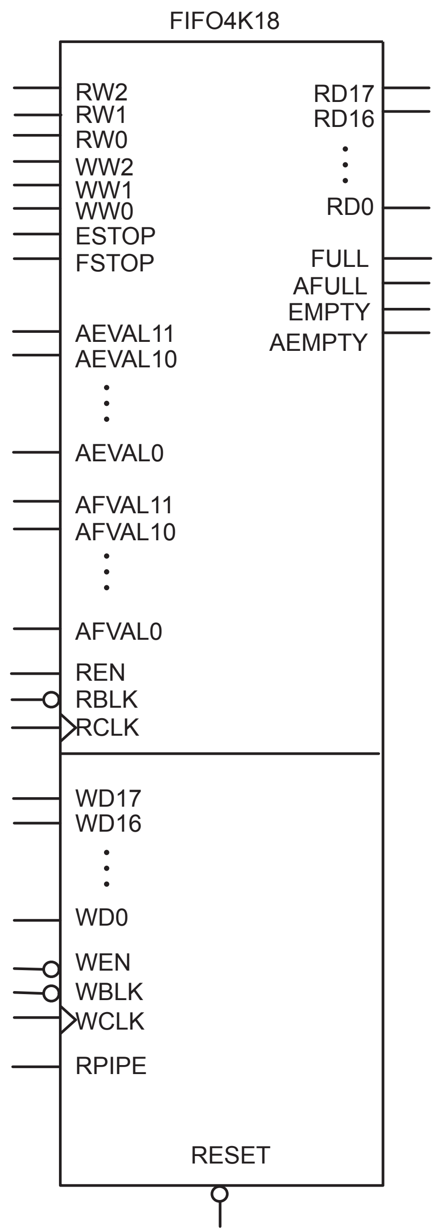

***Figure 2-35* • FIFO Model**

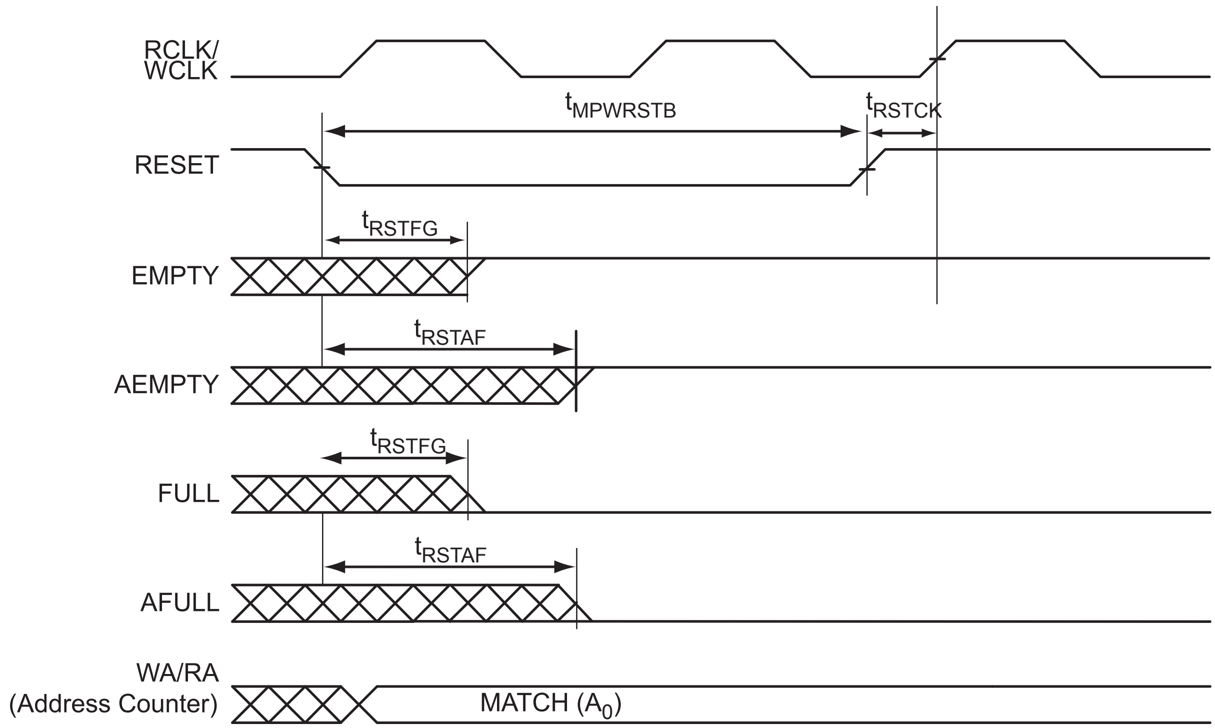

Figure 2-38 • **FIFO Reset**

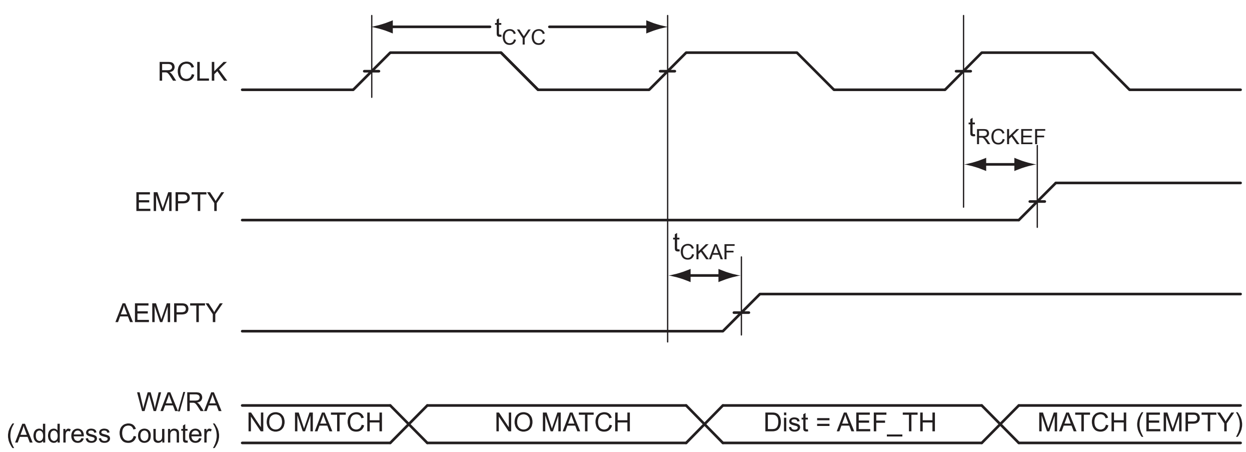

Figure 2-39 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

Embedded Nonvolatile Memory Block (eNVM)

Electrical Characteristics

Table 2-90 describes the eNVM maximum performance.

Table 2-90 **• eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V**

Parameter	Description	A2F060		A2F200		A2F500		Units
		–1	Std.	–1	Std.	–1	Std.	
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 5 cycles (5:1:1:1*)	50	50	50	50	50	50	MHz
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 6 cycles (6:1:1:1*)	100	80	100	80	100	80	MHz

Note: **6:1:1:1 indicates 6 cycles for the first access and 1 each for the next three accesses. 5:1:1:1 indicates 5 cycles for the first access and 1 each for the next three accesses.*

Note: **Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%.*

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-91 describes the eFROM maximum performance

Table 2-91 **• FlashROM Access Time, Worse Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V**

Parameter	Description	–1	Std.	Units
t_{CK2Q}	Clock to out per configuration*	28.68	32.98	ns
F_{max}	Maximum Clock frequency	15.00	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-19 for more details.

Timing Characteristics

Table 2-92 **• JTAG 1532**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.67	0.77	ns
t_{DIHD}	Test Data Input Hold Time	1.33	1.53	ns
t_{TMSSU}	Test Mode Select Setup Time	0.67	0.77	ns
t_{TMDHD}	Test Mode Select Hold Time	1.33	1.53	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	9.20	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-92 • JTAG 1532
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{RSTB2Q}	Reset to Q (data out)	26.67	30.67	ns
F_{TCKMAX}	TCK Maximum Frequency	19.00	21.85	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.27	0.31	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: *All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.*

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-96 • ABPS Performance Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%

Note: **FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quite analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GNDA	Ground	Quiet analog ground to the analog front-end
GNDAQ	Ground	Quiet analog ground to the analog I/O of SmartFusion cSoCs
GNDENVM	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GNDLPXTAL	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GNDMAINXTAL	Ground	Analog ground to the main crystal oscillator circuitry
GNDQ	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND.
GNDRCOSC	Ground	Analog ground to the integrated RC oscillator circuit
GNDSDD0	Ground	Analog ground to the first sigma-delta DAC
GNDSDD1	Ground	Common analog ground to the second and third sigma-delta DACs
GNDTM0	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM1	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM2	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GNDVAREF	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Global I/O Naming Conventions

Gmn (Gxxx) refers to Global I/Os. These Global I/Os are used to connect the input to global networks. Global networks have high fanout and low skew. The naming convention for Global I/Os is as follows:

G = Global

m = Global pin location associated with each CCC on the device:

- A (northwest corner)
- B (northeast corner)
- C (east middle)
- D (southeast corner)
- E (southwest corner)
- F (west middle)

n = Global input MUX and pin number of the associated Global location m—A0, A1, A2, B0, B1, B2, C0, C1, or C2.

Global (GL) I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities.

Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the clocking resources chapter of the *SmartFusion FPGA Fabric User's Guide* and the clock conditioning circuitry chapter of the *SmartFusion Microcontroller Subsystem User's Guide*.

All inputs other than GC/GF are direct inputs into the quadrant clocks. The inputs to the global network are multiplexed, and only one input can be used as a global input. For example, if GAA0 is used as a quadrant global input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs other than GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. For more details, refer to the Global Input Selections section of the SmartFusion Fabric User Guide.

User Pins

Name	Type	Polarity/Bus Size	Description
GPIO_x	In/out	32	Microcontroller Subsystem (MSS) General Purpose I/O (GPIO). The MSS GPIO pin functions as an input, output, tristate, or bidirectional buffer with configurable interrupt generation and Schmitt trigger support. Input and output signal levels are compatible with the I/O standard selected. Unused GPIO pins are tristated and do not include pull-up or pull-down resistors. During power-up, the used GPIO pins are tristated with no pull-up or pull-down resistors until Sys boot configures them. Some of these pins are also multiplexed with integrated peripherals in the MSS (SPI, I^2C, and UART). These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices. GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. This allows GPIO pins to be multiplexed as either I/Os for the FPGA fabric, the ARM® Cortex-M3 or for given integrated MSS peripherals. The MSS peripherals are not multiplexed with each other; they are multiplexed only with the GPIO block. For more information, see the General Purpose I/O Block (GPIO) section in the *SmartFusion Microcontroller Subsystem User's Guide*.
IO	In/out		FPGA user I/O

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
K12	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
K13	GND	GND	GND
K14	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
K15	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
K16	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
L1	GND	GND	GND
L2	GPIO_2/IO31RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
L3	GPIO_3/IO30RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
L4	GPIO_4/IO29RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
L5	GPIO_9/IO24RSB4V0	MAC_CLK	MAC_CLK
L6	GND	GND	GND
L7	VCC	VCC	VCC
L8	GND	GND	GND
L9	VCC	VCC	VCC
L10	GND	GND	GND
L11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
L12	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
L13	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
L14	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
L15	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
L16	GND	GND	GND
M1	GPIO_5/IO28RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
M2	GPIO_6/IO27RSB4V0	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
M3	GPIO_7/IO26RSB4V0	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
M4	GND	GND	GND
M5	NC	ADC3	ADC3
M6	NC	GND15ADC0	GND15ADC0
M7	GND33ADC0	GND33ADC1	GND33ADC1
M8	GND33ADC0	GND33ADC1	GND33ADC1
M9	ADC7	ADC4	ADC4
M10	GNDTM0	GNDTM1	GNDTM1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
P11	GND	GND
P12	VCC	VCC
P13	GND	GND
P14	VCC	VCC
P15	GND	GND
P16	VCCFPGAIOB1	VCCFPGAIOB1
P17	TDI	TDI
P18	TCK	TCK
P19	GND	GND
P20	TMS	TMS
P21	TDO	TDO
P22	TRSTB	TRSTB
R1	MSS_RESET_N	MSS_RESET_N
R2	VCCFPGAIOB5	VCCFPGAIOB5
R3	GPIO_1/IO46RSB4V0	GPIO_1/IO55RSB4V0
R4	NC	NC
R5	NC	NC
R6	NC	NC
R7	NC	NC
R8	GND	GND
R9	VCC	VCC
R10	GND	GND
R11	VCC	VCC
R12	GND	GND
R13	VCC	VCC
R14	GND	GND
R15	VCC	VCC
R16	JTAGSEL	JTAGSEL
R17	NC	NC
R18	NC	NC
R19	NC	NC
R20	NC	NC
R21	VCCFPGAIOB1	VCCFPGAIOB1
R22	NC	NC

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
T1	GND	GND
T2	VCCMSSIOB4	VCCMSSIOB4
T3	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO57RSB4V0	GPIO_11/IO66RSB4V0
T5	GND	GND
T6	MAC_CLK	MAC_CLK
T7	VCCMSSIOB4	VCCMSSIOB4
T8	VCC33SDD0	VCC33SDD0
T9	VCC15A	VCC15A
T10	GNDAQ	GNDAQ
T11	GND33ADC0	GND33ADC0
T12	ADC7	ADC7
T13	NC	TM4
T14	NC	VAREF2
T15	VAREFOUT	VAREFOUT
T16	VCCMSSIOB2	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
T18	GND	GND
T19	NC	NC
T20	NC	NC
T21	VCCMSSIOB2	VCCMSSIOB2
T22	GND	GND
U1	GND	GND
U2	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO58RSB4V0	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4	VCCMSSIOB4
U5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
U6	NC	NC
U7	VCC33AP	VCC33AP
U8	VCC33N	VCC33N
U9	CM1	CM1
U10	VAREF0	VAREF0
U11	GND33ADC1	GND33ADC1
U12	ADC4	ADC4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
W3	GND	GND
W4	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
W5	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
W6	NC	SDD2
W7	GNDA	GNDA
W8	TM0	TM0
W9	ABPS2	ABPS2
W10	GND33ADC0	GND33ADC0
W11	VCC15ADC1	VCC15ADC1
W12	ABPS6	ABPS6
W13	NC	CM4
W14	NC	ABPS9
W15	NC	VCC33ADC2
W16	GNDA	GNDA
W17	PU_N	PU_N
W18	GNDSDD1	GNDSDD1
W19	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
W20	GND	GND
W21	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
W22	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
Y1	GPIO_3/IO44RSB4V0	GPIO_3/IO53RSB4V0
Y2	VCCMSSIOB4	VCCMSSIOB4
Y3	GPIO_15/IO34RSB4V0	GPIO_15/IO43RSB4V0
Y4	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
Y5	VCCMSSIOB4	VCCMSSIOB4
Y6	GNDSDD0	GNDSDD0
Y7	CM0	CM0
Y8	GNDTM0	GNDTM0
Y9	ADC0	ADC0
Y10	VCC15ADC0	VCC15ADC0
Y11	ABPS7	ABPS7
Y12	TM3	TM3
Y13	NC	ABPS8
Y14	NC	GND33ADC2

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*