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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-pq208i

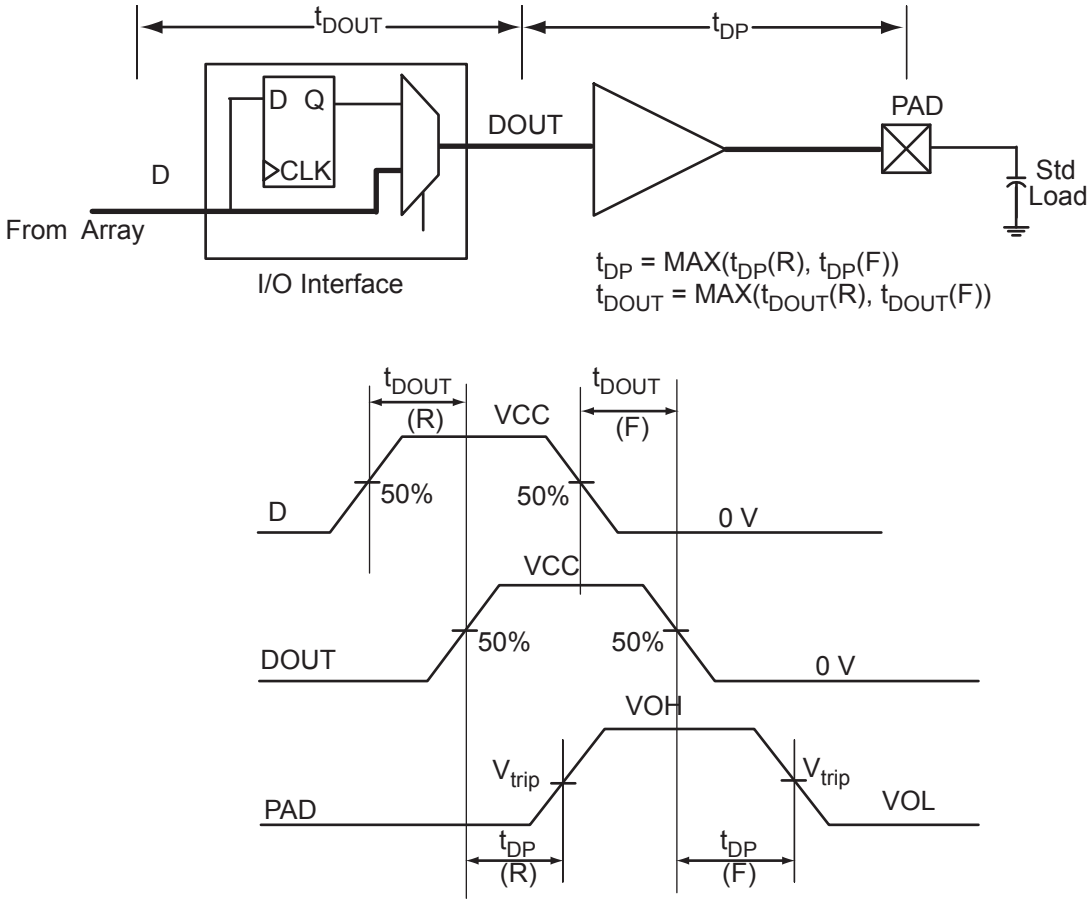

Figure 2-4 • **Output Buffer Model and Delays (example)**

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-47 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	16	16	74	91	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

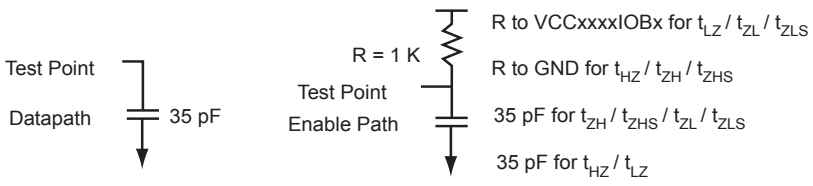

Figure 2-8 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

***Table 2-69* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-14 on page 2-44 for more information.*

Table 2-82 • A2F060 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.75	0.96	0.90	1.15	ns
t_{RCKH}	Input High Delay for Global Clock	0.72	0.98	0.86	1.17	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.31	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

RC Oscillator

The table below describes the electrical characteristics of the RC oscillator.

RC Oscillator Characteristics

Table 2-83 • Electrical Characteristics of the RC Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FRC	Operating frequency			100		MHz
	Accuracy	Temperature: –40°C to 100°C Voltage: 3.3 V ± 5%		1		%
	Output jitter	Period jitter (at 5 K cycles)		100		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles)		100		ps RMS
		Period jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
	Output duty cycle			50		%
IDYNRC	Operating current	3.3 V domain		1		mA
		1.5 V domain		2		mA

FPGA Fabric SRAM and FIFO Characteristics

FPGA Fabric SRAM

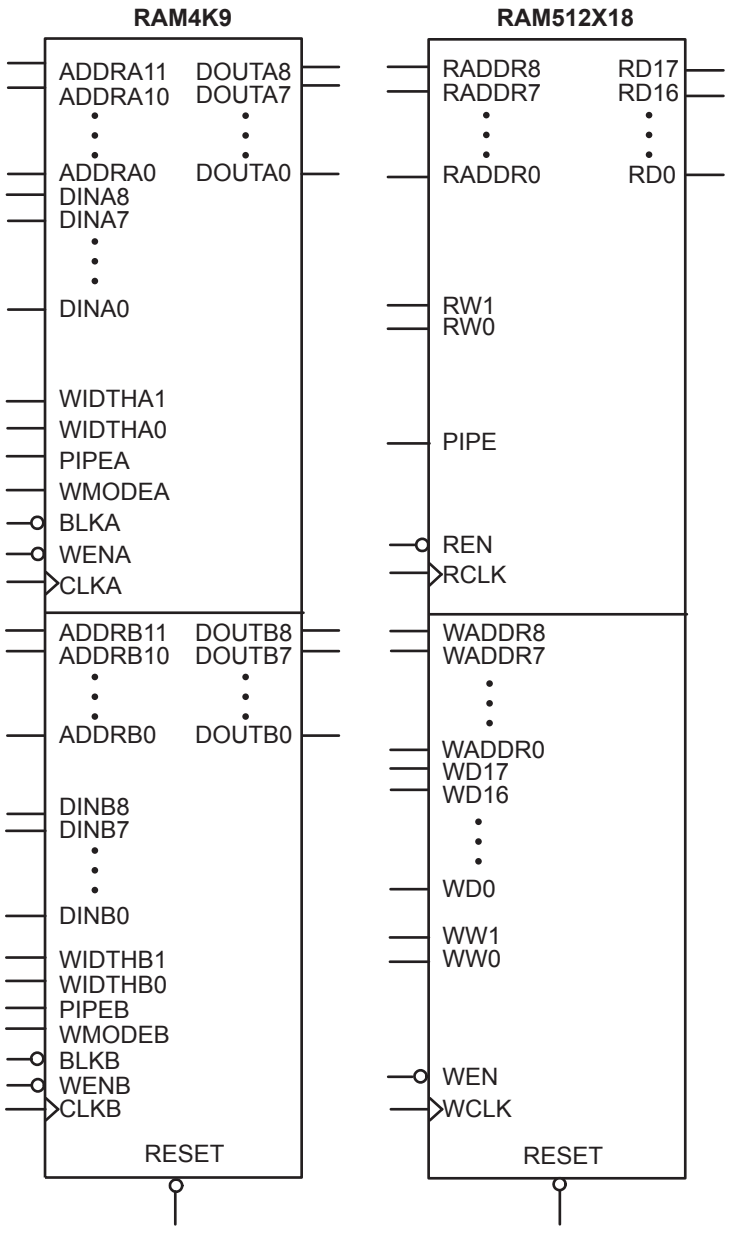

Figure 2-29 • **RAM Models**

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-96 • ABPS Performance Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Re-Programming the eNVM Blocks Using the Cortex-M3

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

Secure Programming

For background, refer to the "Security in Low Power Flash Devices" chapter of the *Fusion FPGA Fabric User's Guide* on the SoC Products Group website. SmartFusion ISP behaves identically to Fusion ISP. IAP of SmartFusion cSoCs is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed with the protection of security measures by using the IAP driver.

Typical Programming and Erase Times

Table 4-3 documents the typical programming and erase times for two components of SmartFusion cSoCs, FPGA fabric and eNVM, using the SoC Products Group's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The **Program** action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

***Table 4-3* • Typical Programming and Erase Times**

	FPGA Fabric (seconds)			eNVM (seconds)			FlashROM (seconds)		
	A2F060	**A2F200**	**A2F500**	**A2F060**	**A2F200**	**A2F500**	**A2F060**	**A2F200**	**A2F500**
Erase	21	21	21	N/A	N/A	N/A	21	21	21
Program	28	35	48	18	39	71	22	22	22
Verify	2	6	12	9	18	37	1	1	1

References

User's Guides

DirectC User's Guide

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132588

In-System Programming (ISP) of Microsemi's Low-Power Flash Devices Using FlashPro4/3/3X

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129973

Programming Flash Devices HandBook

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129930

Application Notes on IAP Programming Technique

SmartFusion cSoC: Programming FPGA Fabric and eNVM Using In-Application Programming Interface App Note

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129818

SmartFusion cSoC: Basic Bootloader and Field Upgrade eNVM Through IAP Interface App Note

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129823

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quite analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GNDA	Ground	Quiet analog ground to the analog front-end
GNDAQ	Ground	Quiet analog ground to the analog I/O of SmartFusion cSoCs
GNDENVM	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GNDLPXTAL	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GNDMAINXTAL	Ground	Analog ground to the main crystal oscillator circuitry
GNDQ	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND.
GNDRCOSC	Ground	Analog ground to the integrated RC oscillator circuit
GNDSDD0	Ground	Analog ground to the first sigma-delta DAC
GNDSDD1	Ground	Common analog ground to the second and third sigma-delta DACs
GNDTM0	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM1	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-14).
GNDTM2	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GNDVAREF	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the "PLL Power Supply Decoupling Scheme" section.*

Special Function Pins

Name	Type	Polarity/Bus Size	Description
NC			No connect This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DC			Do not connect. This pin should not be connected to any signals on the PCB. These pins should be left unconnected.
LPXIN	In	1	Low power 32 KHz crystal oscillator. Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
LPXOUT	In	1	Low power 32 KHz crystal oscillator. Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXIN	In	1	Main crystal oscillator circuit. Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXOUT	Out	1	Main crystal oscillator circuit. Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.

JTAG Pins

SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the SmartFusion cSoC part must be supplied to allow JTAG signals to transition the SmartFusion cSoC. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRSTB pin could be tied to GND.

Name	Type	Polarity/ Bus Size	Description
JTAGSEL	In	1	JTAG controller selection Depending on the state of the JTAGSEL pin, an external JTAG controller will either see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low). The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP.
TCK	In	1	Test clock Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, it is recommended to tie off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state. Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 5-1 on page 5-11 for more information. Can be left floating when unused.
TDI	In	1	Test data Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
TDO	Out	1	Test data Serial output for JTAG boundary scan, ISP, and UJTAG usage.
TMS	In	HIGH	Test mode select The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin. Can be left floating when unused.
TRSTB	In	HIGH	Boundary scan reset pin The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 5-1 on page 5-11 and must satisfy the parallel resistance value requirement. The values in Table 5-1 on page 5-11 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected via a JTAG chain. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, it is recommended that you tie off TRST to GND through a resistor placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG – debug port (SWJ-DP) circuitry within the Cortex-M3. Can be left floating when unused.

Microcontroller Subsystem (MSS)

Name	Type	Polarity/ Bus Size	Description
External Memory Controller			
EMC_ABx	Out	26	External memory controller address bus Can also be used as an FPGA user I/O (see "IO" on page 5-6).
EMC_BYTENx	Out	LOW/2	External memory controller byte enable Can also be used as an FPGA user I/O (see "IO" on page 5-6).
EMC_CLK	Out	Rise	External memory controller clock Can also be used as an FPGA user I/O (see "IO" on page 5-6).
EMC_CSx_N	Out	LOW/2	External memory controller chip selects Can also be used as an FPGA User IO (see "IO" on page 5-6).
EMC_DBx	In/out	16	External memory controller data bus Can also be used as an FPGA user I/O (see "IO" on page 5-6).
EMC_OENx_N	Out	LOW/2	External memory controller output enables Can also be used as an FPGA User IO (see "IO" on page 5-6).
EMC_RW_N	Out	Level	External memory controller read/write. Read = High, write = Low. Can also be used as an FPGA user I/O (see "IO" on page 5-6).
Inter-Integrated Circuit (I^2C) Peripherals			
I2C_0_SCL	In/out	1	I^2C bus serial clock output. First I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
I2C_0_SDA	In/out	1	I^2C bus serial data input/output. First I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
I2C_1_SCL	In/out	1	I^2C bus serial clock output. Second I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
I2C_1_SDA	In/out	1	I^2C bus serial data input/output. Second I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
Serial Peripheral Interface (SPI) Controllers			
SPI_0_CLK	Out	1	Clock. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
SPI_0_DI	In	1	Data input. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
SPI_0_DO	Out	1	Data output. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
SPI_0_SS	Out	1	Slave select (chip select). First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
SPI_1_CLK	Out	1	Clock. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
SPI_1_DI	In	1	Data input. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

TQ144	
Pin Number	**A2F060 Function**
1	VCCPLL0
2	VCOMPLA0
3	GNDQ
4	GFA2/IO42PDB5V0
5	GFB2/IO42NDB5V0
6	GFC2/IO41PDB5V0
7	IO41NDB5V0
8	VCC
9	GND
10	VCCFPGAIOB5
11	IO38PDB5V0
12	IO38NDB5V0
13	IO36PDB5V0
14	IO36NDB5V0
15	GND
16	GNDRCOSC
17	VCCRCOSC
18	MSS_RESET_N
19	GPIO_0/IO33RSB4V0
20	GPIO_1/IO32RSB4V0
21	GPIO_2/IO31RSB4V0
22	GPIO_3/IO30RSB4V0
23	GPIO_4/IO29RSB4V0
24	GND
25	VCCMSSIOB4
26	VCC
27	GPIO_5/IO28RSB4V0
28	GPIO_6/IO27RSB4V0
29	GPIO_7/IO26RSB4V0
30	GPIO_8/IO25RSB4V0
31	VCCESRAM
32	GNDSDD0
33	VCC33SDD0
34	VCC15A
35	PCAP
36	NCAP

TQ144	
Pin Number	**A2F060 Function**
109	VPP
110	GNDQ
111	GCA1/IO20PDB0V0
112	GCA0/IO20NDB0V0
113	GCB1/IO19PDB0V0
114	GCB0/IO19NDB0V0
115	GCC1/IO18PDB0V0
116	GCC0/IO18NDB0V0
117	VCCFPGAIOB0
118	GND
119	VCC
120	IO14PDB0V0
121	IO14NDB0V0
122	IO13NSB0V0
123	IO11PDB0V0
124	IO11NDB0V0
125	IO09PDB0V0
126	IO09NDB0V0
127	VCCFPGAIOB0
128	GND
129	IO07PDB0V0
130	IO07NDB0V0
131	IO06PDB0V0
132	IO06NDB0V0
133	IO05PDB0V0
134	IO05NDB0V0
135	IO03PDB0V0
136	IO03NDB0V0
137	VCCFPGAIOB0
138	GND
139	VCC
140	IO01PDB0V0
141	IO01NDB0V0
142	IO00PDB0V0
143	IO00NDB0V0
144	GNDQ

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
D15	GCA1/IO20PDB0V0	IO24NDB1V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E3	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ	GNDQ
E6	GND	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
E13	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND	GND
F8	VCC	VCC	VCC
F9	GND	GND	GND
F10	VCC	VCC	VCC
F11	GND	GND	GND
F12	IO22NDB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
F13	NC	GNDQ	GNDQ

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
T9	VAREF0	VAREF1	VAREF1
T10	ABPS0	ABPS6	ABPS6
T11	NC	ABPS5	ABPS5
T12	NC	SDD1	SDD1
T13	GNDVAREF	GNDVAREF	GNDVAREF
T14	GNDMAINXTAL	GNDMAINXTAL	GNDMAINXTAL
T15	VCCLPXTAL	VCCLPXTAL	VCCLPXTAL
T16	PU_N	PU_N	PU_N

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
C15	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO19NPB0V0	GBA0/IO23NPB0V0
C20	NC	NC
C21	GBC2/IO21PDB1V0	GBC2/IO30PDB1V0
C22	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
D1	GND	GND
D2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC	NC
D5	NC	NC
D6	GND	GND
D7	NC	IO00NPB0V0
D8	NC	IO03NPB0V0
D9	GND	GND
D10	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
D14	GND	GND
D15	GBC1/IO17PPB0V0	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
D17	GND	GND
D18	GBA1/IO19PPB0V0	GBA1/IO23PPB0V0
D19	NC	NC
D20	NC	NC
D21	IO21NDB1V0	IO30NDB1V0
D22	GND	GND
E1	GFC2/IO67PPB5V0	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5	VCCFPGAIOB5
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
L9	VCC	VCC
L10	GND	GND
L11	VCC	VCC
L12	GND	GND
L13	VCC	VCC
L14	GND	GND
L15	VCC	VCC
L16	GND	GND
L17	GNDQ	GNDQ
L18	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
L19	VCCFPGAIOB1	VCCFPGAIOB1
L20	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
L21	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
L22	GDC2/IO32PDB1V0	GDC2/IO41PDB1V0
M1	NC	IO71PDB5V0
M2	NC	IO71NDB5V0
M3	VCCFPGAIOB5	VCCFPGAIOB5
M4	NC	IO72NPB5V0
M5	GNDQ	GNDQ
M6	NC	IO68PDB5V0
M7	GND	GND
M8	VCC	VCC
M9	GND	GND
M10	VCC	VCC
M11	GND	GND
M12	VCC	VCC
M13	GND	GND
M14	VCC	VCC
M15	GND	GND
M16	VCCFPGAIOB1	VCCFPGAIOB1
M17	NC	NC
M18	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
M19	VJTAG	VJTAG
M20	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
	The A2F060 device was added to product information tables.	N/A
	The "Product Ordering Codes" table was updated to removed Std. speed and add speed grade 1. Pre-production was removed from the application ordering code category.	VI
	The "SmartFusion cSoC Block Diagram" was revised.	IV
	The "Datasheet Categories" section was updated, referencing the "SmartFusion cSoC Block Diagram" table, which is new.	1-4, IV
	The "VCCI" parameter was renamed to "VCCxxxxIOBx." "Advanced I/Os" were renamed to "FPGA I/Os." Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREFx designates VAREF0, VAREF1, and VAREF2. Modes were renamed as follows: Operating mode was renamed to SoC mode. 32KHz Active mode was renamed to Standby mode. Battery mode was renamed to Time Keeping mode. Table entries have been filled with values as data has become available.	N/A
	Table 2-1 • Absolute Maximum Ratings, Table 2-2 • Analog Maximum Ratings, and Table 2-3 • Recommended Operating Conditions[5,6] were revised extensively.	2-1 through 2-3
	Device names were updated in Table 2-6 • Package Thermal Resistance.	2-7
	Table 2-8 • Power Supplies Configuration was revised extensively.	2-10
	Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings was revised extensively.	2-11
	Removed "Example of Power Calculation."	N/A
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs was revised extensively.	2-12
	Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs was revised extensively.	2-13
	The "Power Calculation Methodology" section was revised.	2-14
	Table 2-83 • Electrical Characteristics of the RC Oscillator was revised extensively.	2-61
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator was revised extensively.	2-62
	The parameter t_{RSTBQ} was changed to T_{C2CWRH} in Table 2-87 • RAM4K9.	2-69
	The 12-bit mode row for integral non-linearity was removed from Table 2-95 • ADC Specifications. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear.	2-81
	Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted.	N/A
	Table 2-99 • Voltage Regulator was revised extensively.	2-87
	The "Serial Peripheral Interface (SPI) Characteristics" section and "Inter-Integrated Circuit (I^2C) Characteristics" section are new.	2-89, 2-91