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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | Ethernet, I²C, SPI, UART/USART |
| Speed | 80MHz |
| Primary Attributes | ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-pqg208 |

# SmartFusion cSoC Family Product Table

| FPGA Fabric | A2F060 | | | A2F200 | | | | A2F500 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | TQ144 | CS288 | FG256 | PQ208 | CS288 | FG256 | FG484 | PQ208 | CS288 | FG256 | FG484 |
| System Gates | 60,000 | | | 200,000 | | | | 500,000 | | | |
| Tiles (D-flip-flops) | 1,536 | | | 4,608 | | | | 11,520 | | | |
| RAM Blocks (4,608 bits) | 8 | | | 8 | | | | 24 | | | |
| **Microcontroller Subsystem (MSS)** | **A2F060** | | | **A2F200** | | | | **A2F500** | | | |
| | TQ144 | CS288 | FG256 | PQ208 | CS288 | FG256 | FG484 | PQ208 | CS288 | FG256 | FG484 |
| Flash (Kbytes) | 128 | | | 256 | | | | 512 | | | |
| SRAM (Kbytes) | 16 | | | 64 | | | | 64 | | | |
| Cortex-M3 processor with MPU | Yes | | | Yes | | | | Yes | | | |
| 10/100 Ethernet MAC | No | | | Yes | | | | Yes | | | |
| External Memory Controller (EMC) | – | 26-/16-bit address/data | | 26-bit address,16-bit data | | | | – | 26-/16-bit address/data | | |
| DMA | 8 Ch | | | 8 Ch | | | | 8 Ch | | | |
| $I^2C$ | 2 | | | 2 | | | | 2 | | | |
| SPI | 1 | 2 | | 1 | 2 | | | 1 | 2 | | |
| 16550 UART | 2 | | | 2 | | | | 2 | | | |
| 32-Bit Timer | 2 | | | 2 | | | | 2 | | | |
| PLL | 1 | | | 1 | | | | 1 | 2 | 1 | 2 |
| 32 KHz Low Power Oscillator | 1 | | | 1 | | | | 1 | | | |
| 100 MHz On-Chip RC Oscillator | 1 | | | 1 | | | | 1 | | | |
| Main Oscillator (32 KHz to 20 MHz) | 1 | | | 1 | | | | 1 | | | |
| **Programmable Analog** | **A2F060** | | | **A2F200** | | | | **A2F500** | | | |
| | TQ144 | CS288 | FG256 | PQ208 | CS288 | FG256 | FG484 | PQ208 | CS288 | FG256 | FG484 |
| ADCs (8-/10-/12-bit SAR) | 1 | | | 2 | | | | 2 | | | 3 |
| DACs (8-/16-/24-bit sigma-delta) | 1 | | | 2 | | | | 2 | | | 3 |
| Signal Conditioning Blocks (SCBs) | 1 | | | 4 | | | | 4 | | | 5 |
| Comparator* | 2 | | | 8 | | | | 8 | | | 10 |
| Current Monitors* | 1 | | | 4 | | | | 4 | | | 5 |
| Temperature Monitors* | 1 | | | 4 | | | | 4 | | | 5 |
| Bipolar High Voltage Monitors* | 2 | | | 8 | | | | 8 | | | 10 |

*Note: *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130925 for details.*

***Table 2-2 •*** **Analog Maximum Ratings**

| Parameter | Conditions | Min. | Max. | Units |
|---|---|---|---|---|
| ABPS[n] pad voltage (relative to ground) | GDEC[1:0] = 00 (±15.36 V range) | | | |
| | Absolute maximum | –11.5 | 14.4 | V |
| | Recommended | –11 | 14 | V |
| | GDEC[1:0] = 01 (±10.24 V range) | –11.5 | 12 | V |
| | GDEC[1:0] = 10 (±5.12 V range) | –6 | 6 | V |
| | GDEC[1:0] = 11 (±2.56 V range) | –3 | 3 | V |
| CM[n] pad voltage relative to ground) | CMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 0 (comparator off, for the associated even-numbered comparator) | | | |
| | Absolute maximum | –0.3 | 14.4 | V |
| | Recommended | –0.3 | 14 | V |
| | CMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 1 (comparator on) | –0.3 | 3 | V |
| | TMB_DI_ON = 1 (direct ADC in) | –0.3 | 3 | V |
| TM[n] pad voltage (relative to ground) | TMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 1(comparator on) | –0.3 | 3 | V |
| | TMB_DI_ON = 1 (direct ADC in) | –0.3 | 3 | V |
| ADC[n] pad voltage (relative to ground) | | –0.3 | 3.6 | V |

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of eNVM blocks used in the design
- The analog block used in the design, including the temperature monitor, current monitor, ABPS, sigma-delta DAC, comparator, low power crystal oscillator, RC oscillator and the main crystal oscillator
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-17 on page 2-18.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate to the eNVM blocks

The calculation should be repeated for each clock domain defined in the design.

### Methodology

#### Total Power Consumption—$P_{TOTAL}$

***SoC Mode, Standby Mode, and Time Keeping Mode.***

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### Total Static Power Consumption—$P_{STAT}$

***SoC Mode***

$P_{STAT} = P_{DC1} + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$N_{PLLS}$ is the number of PLLs available in the device.

***Standby Mode***

$P_{STAT} = P_{DC2}$

***Time Keeping Mode***

$P_{STAT} = P_{DC3}$

#### Total Dynamic Power Consumption—$P_{DYN}$

***SoC Mode***

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{eNVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB} + P_{LPXTAL\text{-}OSC} + P_{MSS}$

# User I/O Characteristics

## Timing Model

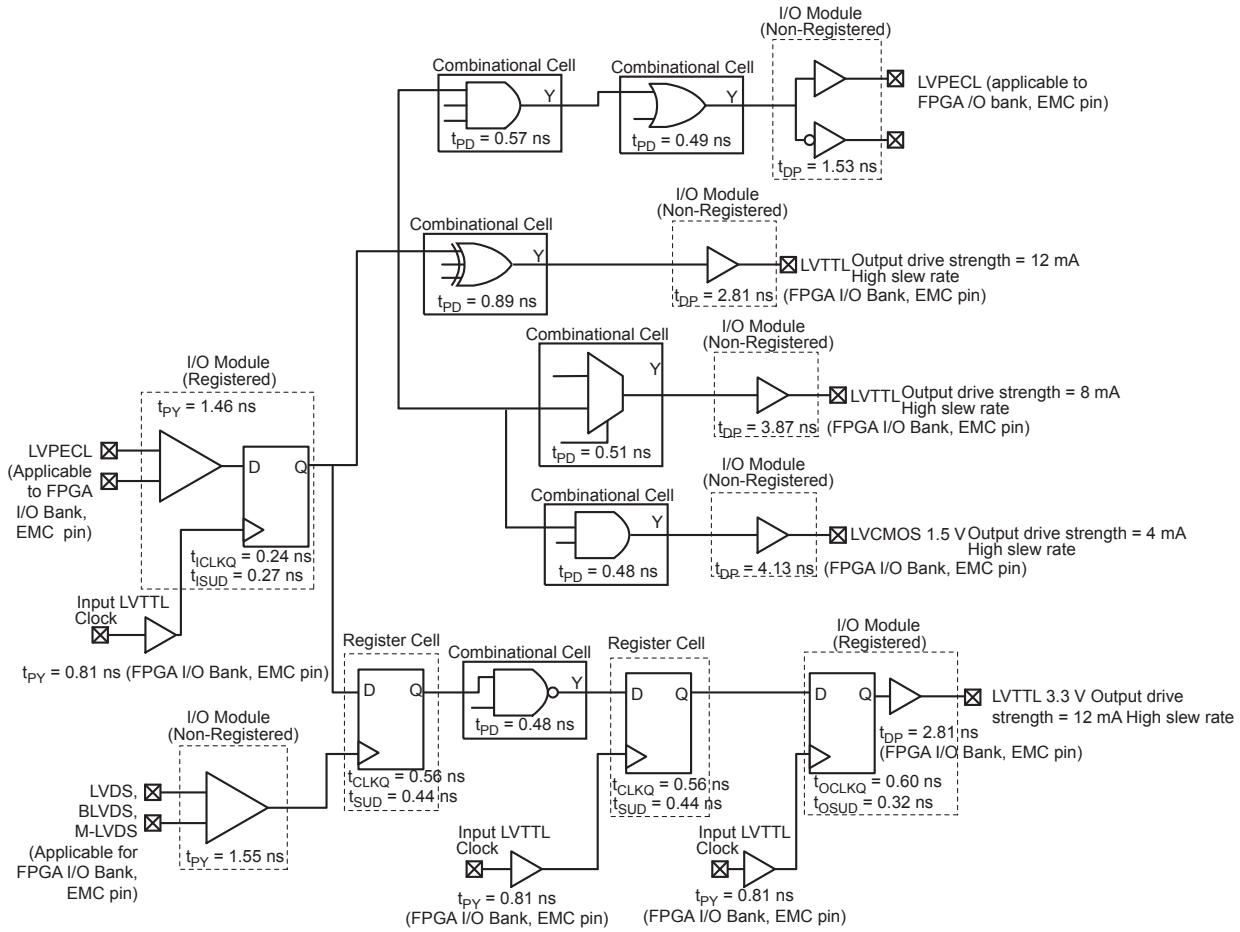


***Figure 2-2 •*** **Timing Model**
**Operating Conditions: –1 Speed, Commercial Temperature Range ($T_J$ = 85°C), Worst Case VCC = 1.425 V**

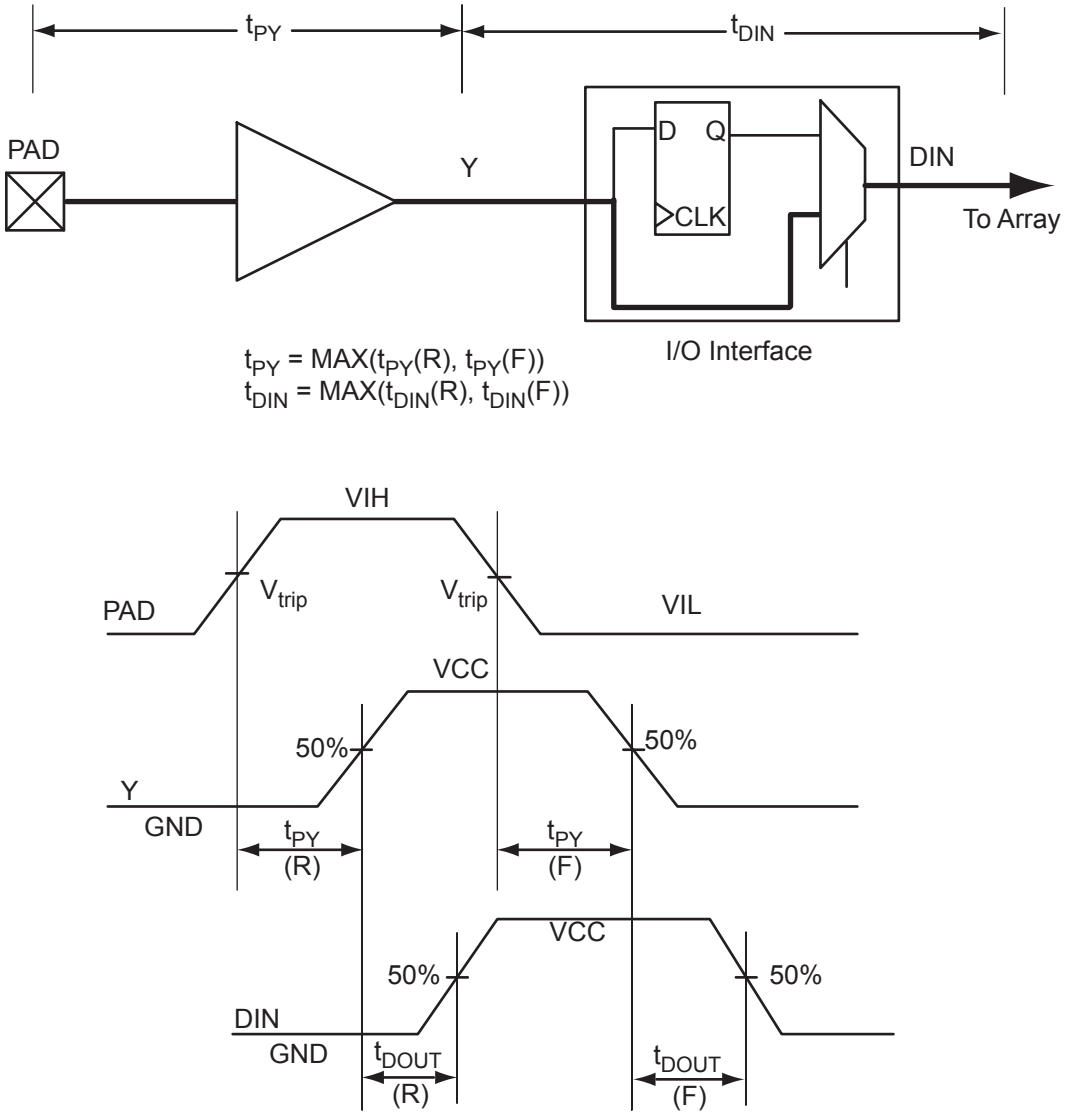


***Figure 2-3 •*** **Input Buffer Timing Model and Delays (example)**

## Detailed I/O DC Characteristics

***Table 2-26* • Input Capacitance**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | $V_{IN}$ = 0, f = 1.0 MHz | | 8 | pF |

***Table 2-27* • I/O Output Buffer Maximum Resistances[1]**
**Applicable to FPGA I/O Banks**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ ($\Omega$)[2] | $R_{PULL\text{-}UP}$ ($\Omega$)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

*Notes:*

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website (also generated by the SoC Products Group Libero SoC toolset).*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

### 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

**Table 2-41 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 2 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 15 | 15 |
| 4 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 15 | 15 |
| 6 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 15 | 15 |
| 8 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 15 | 15 |
| 12 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 15 | 15 |
| 16 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 15 | 15 |
| 24 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 15 | 15 |

*Notes:*

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

**Table 2-42 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

| 2.5 V LVCMOS | VIL | | $V_{IH}$ | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max., mA[1] | µA[2] | µA[2] |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 15 | 15 |

*Notes:*

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

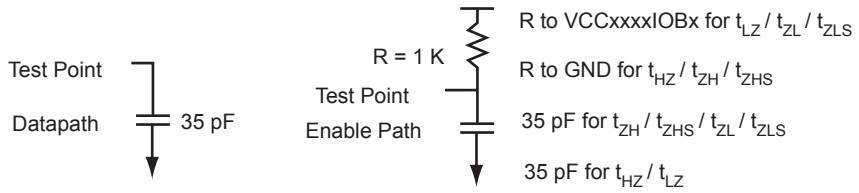


**Figure 2-7 • AC Loading**

**Table 2-43 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $V_{REF}$ (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 2.5 | 1.2 | – | 35 |

* *Measuring point = $V_{trip}$. See Table 2-22 on page 2-24 for a complete table of trip points.*

**Table 2-66 • Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VCCFPGAIOBx | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common-Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common-Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

**Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $V_{REF}$ (typ.) (V) |
|---|---|---|---|
| 1.64 | 1.94 | Cross point | – |

* *Measuring point = $V_{trip}$. See Table 2-22 on page 2-24 for a complete table of trip points.*

### Timing Characteristics

**Table 2-68 • LVPECL**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCFPGAIOBx = 3.0 V**
**Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.60 | 1.76 | 0.04 | 1.76 | ns |
| –1 | 0.50 | 1.46 | 0.03 | 1.46 | ns |

*Notes:*

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

## I/O Register Specifications

### *Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset*

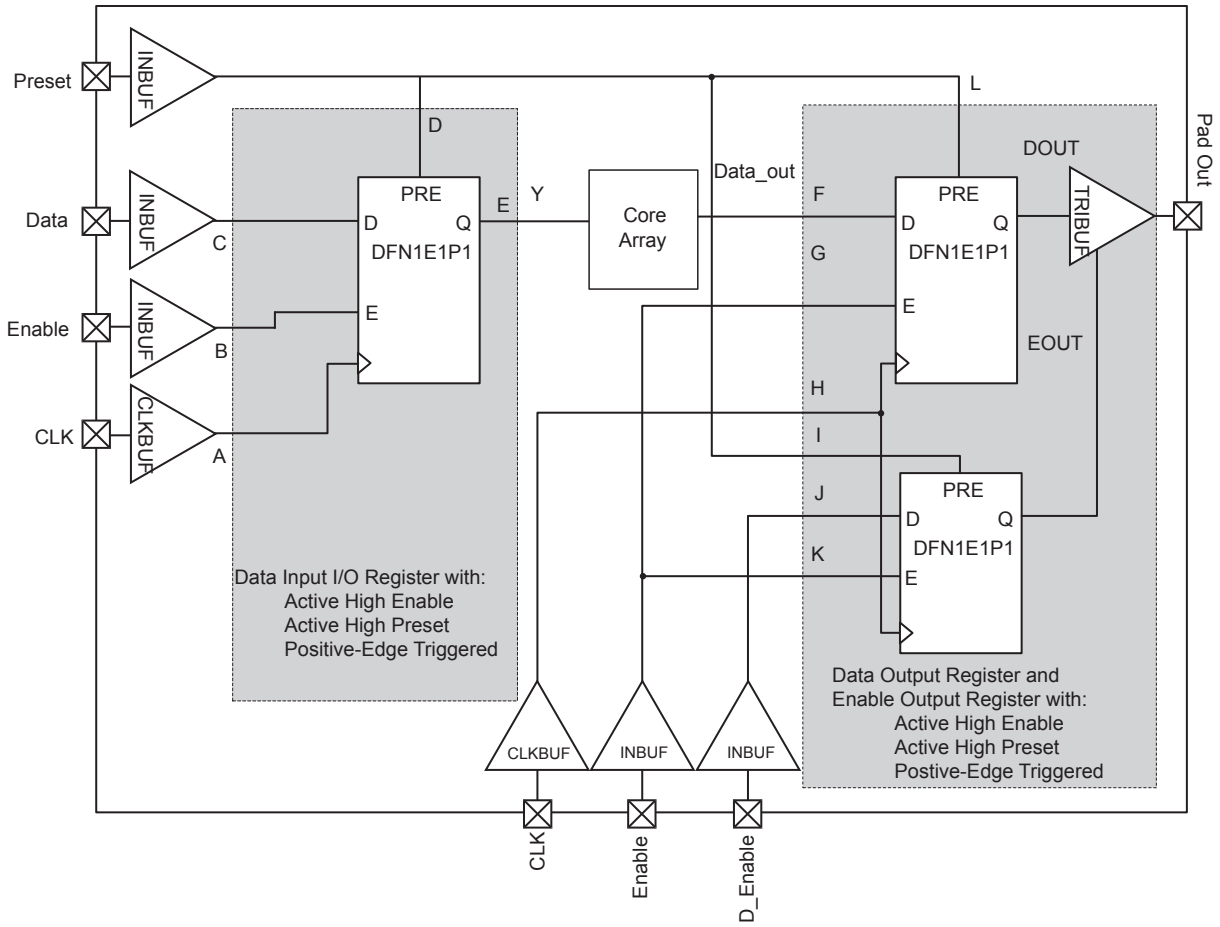


***Figure 2-14 •*** **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

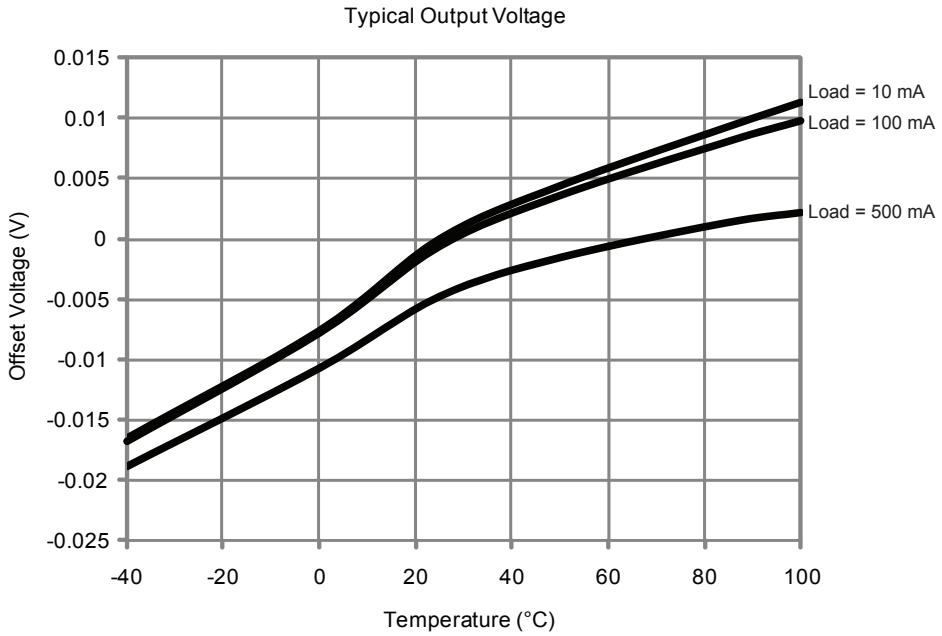


***Figure 2-45 •*** **Typical Output Voltage**

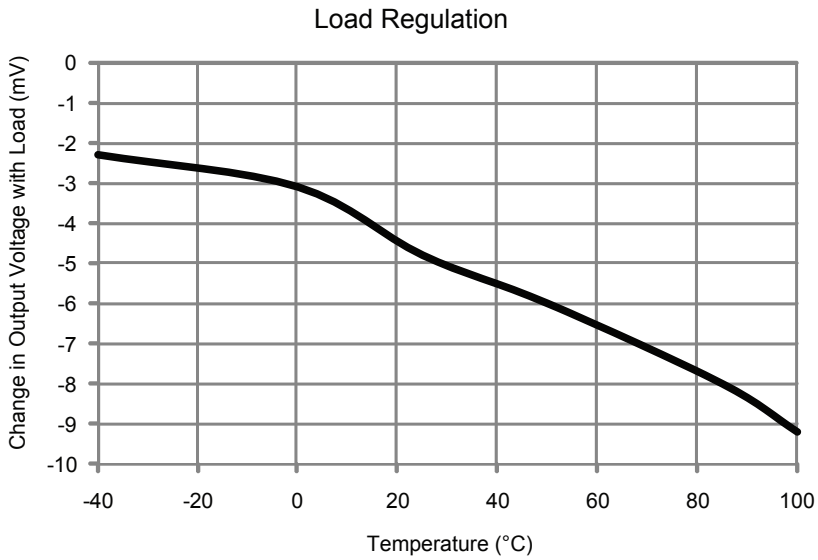


***Figure 2-46 •*** **Load Regulation**

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

| Pin | ADC Channel | Dir.-In Option | Prescaler | Current Mon. | Temp. Mon. | Compar. | LVTTL | SDD MUX | SDD |
|---|---|---|---|---|---|---|---|---|---|
| SDD2 | ADC2_CH15 | | | | | | | | SDD2_OUT |
| TM0 | ADC0_CH4 | Yes | | CM0_L | TM0_IO | CMP0_N | | | |
| TM1 | ADC0_CH8 | Yes | | CM1_L | TM1_IO | CMP2_N | | | |
| TM2 | ADC1_CH4 | Yes | | CM2_L | TM2_IO | CMP4_N | | | |
| TM3 | ADC1_CH8 | Yes | | CM3_L | TM3_IO | CMP6_N | | | |
| TM4 | ADC2_CH4 | Yes | | CM4_L | TM4_IO | CMP8_N | | | |

*Notes:*

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

| TQ144 | |
|---|---|
| **Pin Number** | **A2F060 Function** |
| 1 | VCCPLL0 |
| 2 | VCOMPLA0 |
| 3 | GNDQ |
| 4 | GFA2/IO42PDB5V0 |
| 5 | GFB2/IO42NDB5V0 |
| 6 | GFC2/IO41PDB5V0 |
| 7 | IO41NDB5V0 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCFPGAIOB5 |
| 11 | IO38PDB5V0 |
| 12 | IO38NDB5V0 |
| 13 | IO36PDB5V0 |
| 14 | IO36NDB5V0 |
| 15 | GND |
| 16 | GNDRCOSC |
| 17 | VCCRCOSC |
| 18 | MSS_RESET_N |
| 19 | GPIO_0/IO33RSB4V0 |
| 20 | GPIO_1/IO32RSB4V0 |
| 21 | GPIO_2/IO31RSB4V0 |
| 22 | GPIO_3/IO30RSB4V0 |
| 23 | GPIO_4/IO29RSB4V0 |
| 24 | GND |
| 25 | VCCMSSIOB4 |
| 26 | VCC |
| 27 | GPIO_5/IO28RSB4V0 |
| 28 | GPIO_6/IO27RSB4V0 |
| 29 | GPIO_7/IO26RSB4V0 |
| 30 | GPIO_8/IO25RSB4V0 |
| 31 | VCCESRAM |
| 32 | GNDSDD0 |
| 33 | VCC33SDD0 |
| 34 | VCC15A |
| 35 | PCAP |
| 36 | NCAP |

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| A1 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A2 | GNDQ | GNDQ | GNDQ |
| A3 | EMC_CLK/IO00NDB0V0 | EMC_CLK/GAA0/IO00NDB0V0 | EMC_CLK/GAA0/IO02NDB0V0 |
| A4 | EMC_RW_N/IO00PDB0V0 | EMC_RW_N/GAA1/IO00PDB0V0 | EMC_RW_N/GAA1/IO02PDB0V0 |
| A5 | GND | GND | GND |
| A6 | EMC_CS1_N/IO01PDB0V0 | EMC_CS1_N/GAB1/IO01PDB0V0 | EMC_CS1_N/GAB1/IO05PDB0V0 |
| A7 | EMC_CS0_N/IO01NDB0V0 | EMC_CS0_N/GAB0/IO01NDB0V0 | EMC_CS0_N/GAB0/IO05NDB0V0 |
| A8 | EMC_AB[0]/IO04NPB0V0 | EMC_AB[0]/IO04NPB0V0 | EMC_AB[0]/IO06NPB0V0 |
| A9 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A10 | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO10NDB0V0 |
| A11 | EMC_AB[8]/IO08NPB0V0 | EMC_AB[8]/IO08NPB0V0 | EMC_AB[8]/IO13NPB0V0 |
| A12 | EMC_AB[14]/IO11NPB0V0 | EMC_AB[14]/IO11NPB0V0 | EMC_AB[14]/IO15NPB0V0 |
| A13 | GND | GND | GND |
| A14 | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO18NDB0V0 |
| A15 | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO20NDB0V0 |
| A16 | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO20PDB0V0 |
| A17 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A18 | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO21NDB0V0 |
| A19 | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO21PDB0V0 |
| A20 | GNDQ | GNDQ | GNDQ |
| A21 | GND | GND | GND |
| AA1 | ADC1 | ABPS1 | ABPS1 |
| AA2 | GNDAQ | GNDAQ | GNDAQ |
| AA3 | GNDA | GNDA | GNDA |
| AA4 | VCC33N | VCC33N | VCC33N |
| AA5 | SDD0 | SDD0 | SDD0 |
| AA6 | ADC0 | ABPS0 | ABPS0 |
| AA7 | NC | GNDTM0 | GNDTM0 |
| AA8 | NC | ABPS2 | ABPS2 |
| AA9 | NC | VAREF0 | VAREF0 |
| AA10 | NC | GND15ADC0 | GND15ADC0 |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| C21 | IO17NDB0V0 | GBA2/IO20PDB1V0 | GBA2/IO27PDB1V0 |
| D1 | EMC_DB[14]/IO45NDB5V0 | EMC_DB[14]/GAB2/IO71NDB5V0 | EMC_DB[14]/GAB2/IO88NDB5V0 |
| D3 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| D19 | GND | GND | GND |
| D21 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| E1 | EMC_DB[13]/IO44PDB5V0 | EMC_DB[13]/GAC2/IO70PDB5V0 | EMC_DB[13]/GAC2/IO87PDB5V0 |
| E3 | EMC_DB[12]/IO44NDB5V0 | EMC_DB[12]/IO70NDB5V0 | EMC_DB[12]/IO87NDB5V0 |
| E5 | GNDQ | GNDQ | GNDQ |
| E6 | EMC_BYTEN[0]/IO02NDB0V0 | EMC_BYTEN[0]/GAC0/IO02NDB0V0 | EMC_BYTEN[0]/GAC0/IO07NDB0V0 |
| E7 | EMC_BYTEN[1]/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO07PDB0V0 |
| E8 | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO08PDB0V0 |
| E9 | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO09PDB0V0 |
| E10 | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO11NDB0V0 |
| E11 | EMC_AB[7]/IO07PDB0V0 | EMC_AB[7]/IO07PDB0V0 | EMC_AB[7]/IO12PDB0V0 |
| E12 | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO14PDB0V0 |
| E13 | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO17NDB0V0 |
| E14 | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO17PDB0V0 |
| E15 | GCC0/IO18NPB0V0 | GCB0/IO27NDB1V0 | GCB0/IO34NDB1V0 |
| E16 | GCA1/IO20PPB0V0 | GCB1/IO27PDB1V0 | GCB1/IO34PDB1V0 |
| E17 | GCC1/IO18PPB0V0 | GCB2/IO24PDB1V0 | GCB2/IO33PDB1V0 |
| E19 | GCB2/IO22PPB1V0 | GCA0/IO28NDB1V0 | GCA0/IO36NDB1V0 * |
| E21 | IO21NDB1V0 | GCA1/IO28PDB1V0 | GCA1/IO36PDB1V0 * |
| F1 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| F3 | GFB2/IO42NDB5V0 | GFB2/IO68NDB5V0 | GFB2/IO85NDB5V0 |
| F5 | GFA2/IO42PDB5V0 | GFA2/IO68PDB5V0 | GFA2/IO85PDB5V0 |
| F6 | EMC_DB[11]/IO43PDB5V0 | EMC_DB[11]/IO69PDB5V0 | EMC_DB[11]/IO86PDB5V0 |
| F7 | GND | GND | GND |
| F8 | NC | GFC1/IO66PPB5V0 | GFC1/IO83PPB5V0 |
| F9 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| F10 | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO11PDB0V0 |
| F11 | EMC_AB[6]/IO07NDB0V0 | EMC_AB[6]/IO07NDB0V0 | EMC_AB[6]/IO12NDB0V0 |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

# PQ208


***Note***

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| Pin Number | PQ208 | |
|---|---|---|
| | A2F200 | A2F500 |
| 63 | TM1 | TM1 |
| 64 | CM1 | CM1 |
| 65 | ABPS3 | ABPS3 |
| 66 | ABPS2 | ABPS2 |
| 67 | ADC0 | ADC0 |
| 68 | ADC1 | ADC1 |
| 69 | ADC2 | ADC2 |
| 70 | ADC3 | ADC3 |
| 71 | VAREF0 | VAREF0 |
| 72 | GND33ADC0 | GND33ADC0 |
| 73 | VCC33ADC0 | VCC33ADC0 |
| 74 | GND33ADC0 | GND33ADC0 |
| 75 | VCC15ADC0 | VCC15ADC0 |
| 76 | GND15ADC0 | GND15ADC0 |
| 77 | GND15ADC1 | GND15ADC1 |
| 78 | VCC15ADC1 | VCC15ADC1 |
| 79 | GND33ADC1 | GND33ADC1 |
| 80 | VCC33ADC1 | VCC33ADC1 |
| 81 | GND33ADC1 | GND33ADC1 |
| 82 | VAREF1 | VAREF1 |
| 83 | ADC7 | ADC7 |
| 84 | ADC6 | ADC6 |
| 85 | ADC5 | ADC5 |
| 86 | ADC4 | ADC4 |
| 87 | ABPS6 | ABPS6 |
| 88 | ABPS7 | ABPS7 |
| 89 | CM3 | CM3 |
| 90 | TM3 | TM3 |
| 91 | GNDTM1 | GNDTM1 |
| 92 | TM2 | TM2 |
| 93 | CM2 | CM2 |

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| Pin Number | PQ208 | |
|---|---|---|
| | A2F200 | A2F500 |
| 94 | ABPS5 | ABPS5 |
| 95 | ABPS4 | ABPS4 |
| 96 | GNDAQ | GNDAQ |
| 97 | GNDA | GNDA |
| 98 | NC | NC |
| 99 | GNDVAREF | GNDVAREF |
| 100 | VAREFOUT | VAREFOUT |
| 101 | PU_N | PU_N |
| 102 | VCC33A | VCC33A |
| 103 | PTEM | PTEM |
| 104 | PTBASE | PTBASE |
| 105 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 |
| 106 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 |
| 107 | SPI_0_CLK/GPIO_18 | SPI_0_CLK/GPIO_18 |
| 108 | SPI_0_SS/GPIO_19 | SPI_0_SS/GPIO_19 |
| 109 | UART_0_RXD/GPIO_21 | UART_0_RXD/GPIO_21 |
| 110 | UART_0_TXD/GPIO_20 | UART_0_TXD/GPIO_20 |
| 111 | UART_1_RXD/GPIO_29 | UART_1_RXD/GPIO_29 |
| 112 | UART_1_TXD/GPIO_28 | UART_1_TXD/GPIO_28 |
| 113 | VCC | VCC |
| 114 | VCCMSSIOB2 | VCCMSSIOB2 |
| 115 | GND | GND |
| 116 | I2C_1_SDA/GPIO_30 | I2C_1_SDA/GPIO_30 |
| 117 | I2C_1_SCL/GPIO_31 | I2C_1_SCL/GPIO_31 |
| 118 | I2C_0_SDA/GPIO_22 | I2C_0_SDA/GPIO_22 |
| 119 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 |
| 120 | GNDENVM | GNDENVM |
| 121 | VCCENVM | VCCENVM |
| 122 | JTAGSEL | JTAGSEL |
| 123 | TCK | TCK |
| 124 | TDI | TDI |

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| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| A1 | GND | GND | GND |
| A2 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A3 | EMC_AB[0]/IO04NDB0V0 | EMC_AB[0]/IO04NDB0V0 | EMC_AB[0]/IO06NDB0V0 |
| A4 | EMC_AB[1]/IO04PDB0V0 | EMC_AB[1]/IO04PDB0V0 | EMC_AB[1]/IO06PDB0V0 |
| A5 | GND | GND | GND |
| A6 | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO09PDB0V0 |
| A7 | EMC_AB[5]/IO06PDB0V0 | EMC_AB[5]/IO06PDB0V0 | EMC_AB[5]/IO10PDB0V0 |
| A8 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A9 | GND | GND | GND |
| A10 | EMC_AB[14]/IO11NDB0V0 | EMC_AB[14]/IO11NDB0V0 | EMC_AB[14]/IO15NDB0V0 |
| A11 | EMC_AB[15]/IO11PDB0V0 | EMC_AB[15]/IO11PDB0V0 | EMC_AB[15]/IO15PDB0V0 |
| A12 | GND | GND | GND |
| A13 | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO21NDB0V0 |
| A14 | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO20NDB0V0 |
| A15 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A16 | GND | GND | GND |
| B1 | EMC_DB[15]/IO45PDB5V0 | EMC_DB[15]/GAA2/IO71PDB5V0 | EMC_DB[15]/GAA2/IO88PDB5V0 |
| B2 | GND | GND | GND |
| B3 | EMC_BYTEN[1]/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO07PDB0V0 |
| B4 | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO08NDB0V0 |
| B5 | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO08PDB0V0 |
| B6 | EMC_AB[2]/IO05NDB0V0 | EMC_AB[2]/IO05NDB0V0 | EMC_AB[2]/IO09NDB0V0 |
| B7 | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO10NDB0V0 |
| B8 | EMC_AB[9]/IO08PDB0V0 | EMC_AB[9]/IO08PDB0V0 | EMC_AB[9]/IO13PDB0V0 |
| B9 | EMC_AB[12]/IO10NDB0V0 | EMC_AB[12]/IO10NDB0V0 | EMC_AB[12]/IO14NDB0V0 |
| B10 | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO14PDB0V0 |
| B11 | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO17NDB0V0 |
| B12 | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO18NDB0V0 |
| B13 | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO21PDB0V0 |
| B14 | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO20PDB0V0 |
| B15 | GND | GND | GND |

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| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| C15 | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO17PDB0V0 |
| C16 | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO20NDB0V0 |
| C17 | EMC_AB[22]/IO15NDB0V0 | EMC_AB[22]/IO19NDB0V0 |
| C18 | EMC_AB[23]/IO15PDB0V0 | EMC_AB[23]/IO19PDB0V0 |
| C19 | GBA0/IO19NPB0V0 | GBA0/IO23NPB0V0 |
| C20 | NC | NC |
| C21 | GBC2/IO21PDB1V0 | GBC2/IO30PDB1V0 |
| C22 | GBB2/IO20NDB1V0 | GBB2/IO27NDB1V0 |
| D1 | GND | GND |
| D2 | EMC_DB[12]/IO70NDB5V0 | EMC_DB[12]/IO87NDB5V0 |
| D3 | EMC_DB[13]/GAC2/IO70PDB5V0 | EMC_DB[13]/GAC2/IO87PDB5V0 |
| D4 | NC | NC |
| D5 | NC | NC |
| D6 | GND | GND |
| D7 | NC | IO00NPB0V0 |
| D8 | NC | IO03NPB0V0 |
| D9 | GND | GND |
| D10 | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO08NDB0V0 |
| D11 | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO11NDB0V0 |
| D12 | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO11PDB0V0 |
| D13 | EMC_AB[9]/IO08PDB0V0 | EMC_AB[9]/IO13PDB0V0 |
| D14 | GND | GND |
| D15 | GBC1/IO17PPB0V0 | GBC1/IO22PPB0V0 |
| D16 | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO20PDB0V0 |
| D17 | GND | GND |
| D18 | GBA1/IO19PPB0V0 | GBA1/IO23PPB0V0 |
| D19 | NC | NC |
| D20 | NC | NC |
| D21 | IO21NDB1V0 | IO30NDB1V0 |
| D22 | GND | GND |
| E1 | GFC2/IO67PPB5V0 | GFC2/IO84PPB5V0 |
| E2 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| E3 | GFA2/IO68PDB5V0 | GFA2/IO85PDB5V0 |
| E4 | GND | GND |

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1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
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# Datasheet Categories

### *Categories*

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion cSoC Device Status" table on page III, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### *Product Brief*

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### *Advance*

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### *Preliminary*

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### *Production*

This version contains information that is considered to be final.

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