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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | Ethernet, I²C, SPI, UART/USART |
| Speed | 80MHz |
| Primary Attributes | ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-pqg208i |

This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

### Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

***Table 2-2 •*** **Analog Maximum Ratings**

| Parameter | Conditions | Min. | Max. | Units |
|---|---|---|---|---|
| ABPS[n] pad voltage (relative to ground) | GDEC[1:0] = 00 (±15.36 V range) | | | |
| | Absolute maximum | –11.5 | 14.4 | V |
| | Recommended | –11 | 14 | V |
| | GDEC[1:0] = 01 (±10.24 V range) | –11.5 | 12 | V |
| | GDEC[1:0] = 10 (±5.12 V range) | –6 | 6 | V |
| | GDEC[1:0] = 11 (±2.56 V range) | –3 | 3 | V |
| CM[n] pad voltage relative to ground) | CMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 0 (comparator off, for the associated even-numbered comparator) | | | |
| | Absolute maximum | –0.3 | 14.4 | V |
| | Recommended | –0.3 | 14 | V |
| | CMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 1 (comparator on) | –0.3 | 3 | V |
| | TMB_DI_ON = 1 (direct ADC in) | –0.3 | 3 | V |
| TM[n] pad voltage (relative to ground) | TMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 1(comparator on) | –0.3 | 3 | V |
| | TMB_DI_ON = 1 (direct ADC in) | –0.3 | 3 | V |
| ADC[n] pad voltage (relative to ground) | | –0.3 | 3.6 | V |

## Power Consumption of Various Internal Resources

***Table 2-14* • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

| Parameter | Definition | Power Supply | | Device | | | Units |
|---|---|---|---|---|---|---|---|
| | | Name | Domain | A2F060 | A2F200 | A2F500 | |
| PAC1 | Clock contribution of a Global Rib | VCC | 1.5 V | 3.39 | 3.40 | 5.05 | µW/MHz |
| PAC2 | Clock contribution of a Global Spine | VCC | 1.5 V | 1.14 | 1.83 | 2.50 | µW/MHz |
| PAC3 | Clock contribution of a VersaTile row | VCC | 1.5 V | 1.15 | 1.15 | 1.15 | µW/MHz |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | VCC | 1.5 V | 0.12 | 0.12 | 0.12 | µW/MHz |
| PAC5 | First contribution of a VersaTile used as a sequential module | VCC | 1.5 V | 0.07 | 0.07 | 0.07 | µW/MHz |
| PAC6 | Second contribution of a VersaTile used as a sequential module | VCC | 1.5 V | 0.29 | 0.29 | 0.29 | µW/MHz |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | VCC | 1.5 V | 0.29 | 0.29 | 0.29 | µW/MHz |
| PAC8 | Average contribution of a routing net | VCC | 1.5 V | 1.04 | 0.79 | 0.79 | µW/MHz |
| PAC9 | Contribution of an I/O input pin (standard dependent) | VCCxxxxIOBx/VCC | See Table 2-10 and Table 2-11 on page 2-11 | | | | |
| PAC10 | Contribution of an I/O output pin (standard dependent) | VCCxxxxIOBx/VCC | See Table 2-12 and Table 2-13 on page 2-11 | | | | |
| PAC11 | Average contribution of a RAM block during a read operation | VCC | 1.5 V | 25.00 | | | µW/MHz |
| PAC12 | Average contribution of a RAM block during a write operation | VCC | 1.5 V | 30.00 | | | µW/MHz |
| PAC13 | Dynamic Contribution for PLL | VCC | 1.5 V | 2.60 | | | µW/MHz |
| PAC15 | Contribution of NVM block during a read operation (F < 33MHz) | VCC | 1.5 V | 358.00 | | | µW/MHz |
| PAC16 | 1st contribution of NVM block during a read operation (F > 33MHz) | VCC | 1.5 V | 12.88 | | | mW |
| PAC17 | 2nd contribution of NVM block during a read operation (F > 33MHz) | VCC | 1.5 V | 4.80 | | | µW/MHz |
| PAC18 | Main Crystal Oscillator contribution | VCCMAINXTAL | 3.3 V | 1.98 | | | mW |
| PAC19a | RC Oscillator contribution | VCCRCOSC | 3.3 V | 3.30 | | | mW |
| PAC19b | RC Oscillator contribution | VCC | 1.5 V | 3.00 | | | mW |
| PAC20a | Analog Block Dynamic Power Contribution of the ADC | VCC33ADCx | 3.3 V | 8.25 | | | mW |
| PAC20b | Analog Block Dynamic Power Contribution of the ADC | VCC15ADCx | 1.5 V | 3.00 | | | mW |
| PAC21 | Low Power Crystal Oscillator contribution | VCCLPXTAL | 3.3 V | 33.00 | | | µW |
| PAC22 | MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1] | VCC | 1.5 V | 67.50 | | | mW |
| PAC23 | Temperature Monitor Power Contribution | See Table 2-94 on page 2-79 | – | 1.23 | | | mW |

***Standby Mode***

$P_{DYN} = P_{RC\text{-}OSC} + P_{LPXTAL\text{-}OSC}$

***Time Keeping Mode***

$P_{DYN} = P_{LPXTAL\text{-}OSC}$

### Global Clock Dynamic Contribution—$P_{CLOCK}$

***SoC Mode***

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

***Standby Mode and Time Keeping Mode***

$P_{CLOCK} = 0$ W

### Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

***SoC Mode***

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

$F_{CLK}$ is the global clock signal frequency.

***Standby Mode and Time Keeping Mode***

$P_{S\text{-}CELL} = 0$ W

### Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

***SoC Mode***

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

$F_{CLK}$ is the global clock signal frequency.

***Standby Mode and Time Keeping Mode***

$P_{C\text{-}CELL} = 0$ W

### Routing Net Dynamic Contribution—$P_{NET}$

***SoC Mode***

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-18.

$F_{CLK}$ is the frequency of the clock driving the logic including these nets.

## Single-Ended I/O Characteristics

### 3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

**Table 2-35 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

| 3.3 V LVTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 15 | 15 |
| 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 15 | 15 |
| 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 15 | 15 |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 15 | 15 |
| 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 15 | 15 |
| 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 127 | 132 | 15 | 15 |
| 24 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 181 | 268 | 10 | 10 |

*Notes:*

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

**Table 2-36 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

| 3.3 V LVTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 15 | 15 |

*Notes:*

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

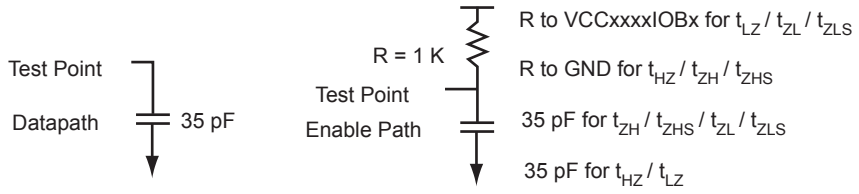



**Figure 2-6 • AC Loading**

**Table 2-37 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $V_{REF}$ (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 1.4 | – | 35 |

*Note: *Measuring point = $V_{trip}$. See Table 2-22 on page 2-24 for a complete table of trip points.*

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

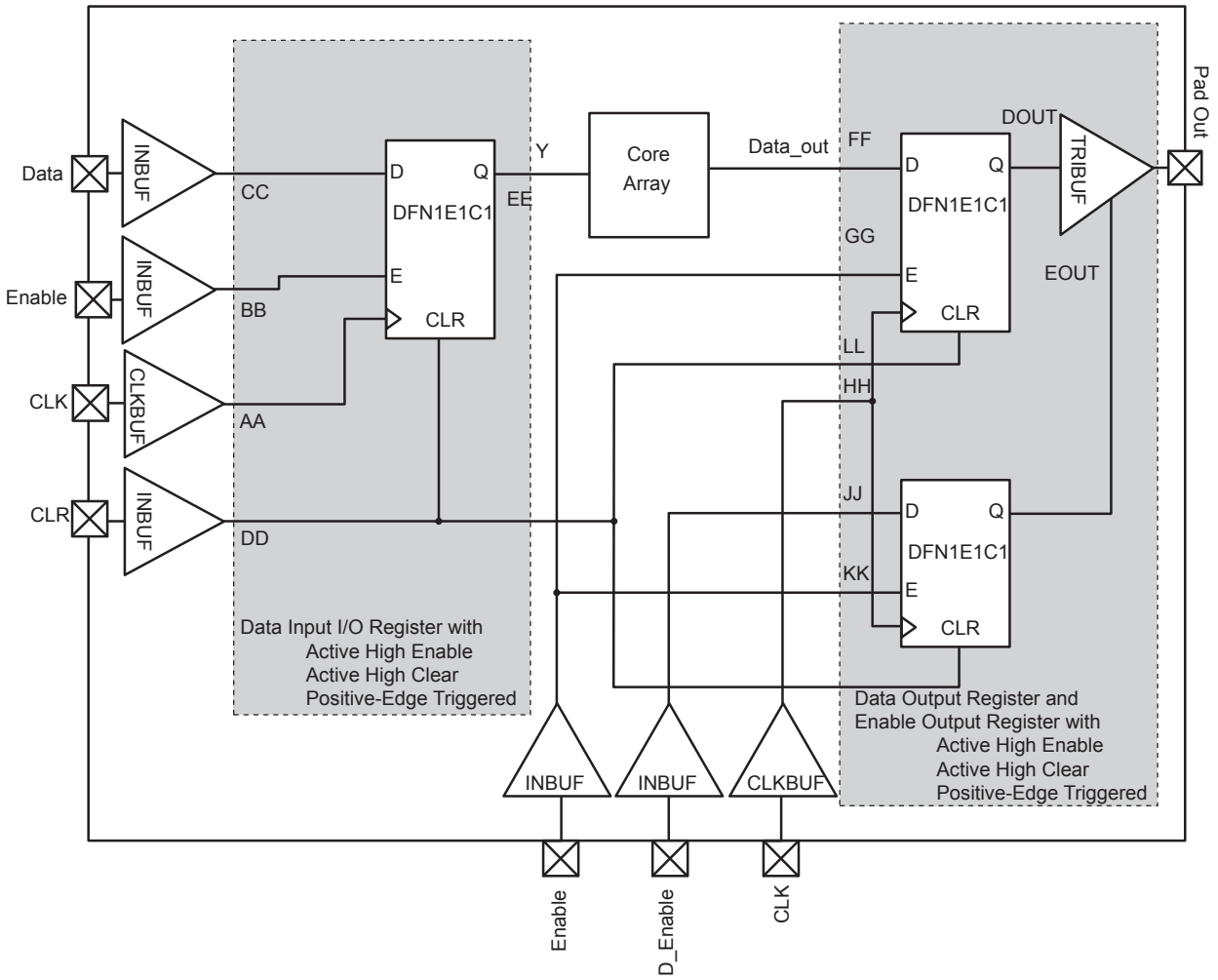



***Figure 2-15 •*** **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

# Clock Conditioning Circuits

## CCC Electrical Specifications

### Timing Characteristics

***Table 2-86* • SmartFusion CCC/PLL Specification**

| Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$ | 1.5 | | 350 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$ | 0.75 | | 350[1] | MHz |
| Delay Increments in Programmable Delay Blocks[2,3,4] | | 160 | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Input Period Jitter | | | 1.5 | ns |
| Acquisition Time | | | | |
| LockControl = 0 | | | 300 | µs |
| LockControl = 1 | | | 6.0 | ms |
| Tracking Jitter[5] | | | | |
| LockControl = 0 | | | 1.6 | ns |
| LockControl = 1 | | | 0.8 | ns |
| Output Duty Cycle | 48.5 | | 5.15 | % |
| Delay Range in Block: Programmable Delay 1[2,3] | 0.6 | | 5.56 | ns |
| Delay Range in Block: Programmable Delay 2[2,3] | 0.025 | | 5.56 | ns |
| Delay Range in Block: Fixed Delay[2,3] | | 2.2 | | ns |
| CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ [6,7] | Maximum Peak-to-Peak Period Jitter | | | |

| | SSO ≤ 2 | | SSO ≤ 4 | | SSO ≤ 8 | | SSO ≤ 16 | |
|---|---|---|---|---|---|---|---|---|
| | FG/CS | PQ | FG/CS | PQ | FG/CS | PQ | FG/CS | PQ |
| 0.75 MHz to 50 MHz | 0.5% | 1.6% | 0.9% | 1.6% | 0.9% | 1.6% | 0.9% | 1.8% |
| 50 MHz to 250 MHz | 1.75% | 3.5% | 9.3% | 9.3% | 9.3% | 17.9% | 10.0% | 17.9% |
| 250 MHz to 350 MHz | 2.5% | 5.2% | 13.0% | 13.0% | 13.0% | 25.0% | 14.0% | 25.0% |

*Notes:*

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *$T_J$ = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*

# FPGA Fabric SRAM and FIFO Characteristics

## FPGA Fabric SRAM

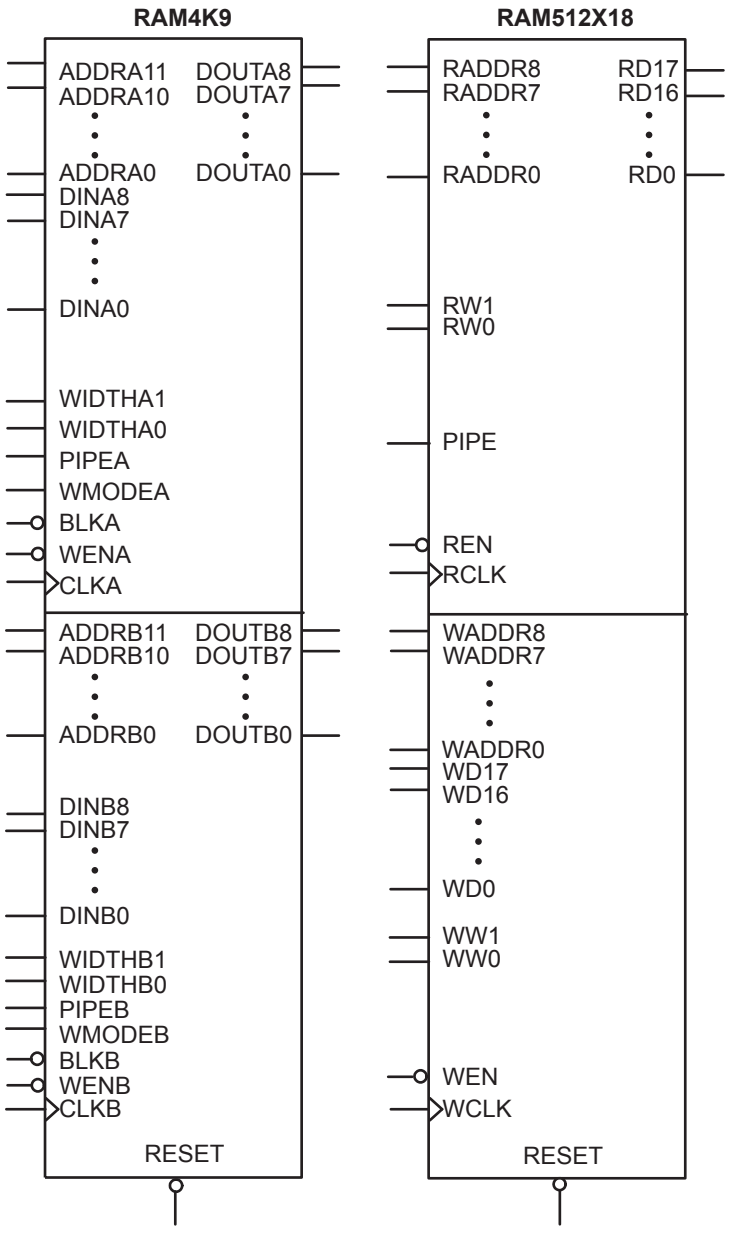



***Figure 2-29 •*** **RAM Models**

**Table 2-88 • RAM512X18**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.30 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.09 | 0.11 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.06 | 0.07 | ns |
| $t_{DS}$ | Input data (WD) setup time | 0.19 | 0.22 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained, WMODE = 0) | 2.19 | 2.63 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 0.91 | 1.09 | ns |
| $t_{C2CRWH}$ [1] | Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge | 0.38 | 0.43 | ns |
| $t_{C2CWRH}$ [1] | Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge | 0.44 | 0.50 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on RD (flow-through) | 0.94 | 1.12 | ns |
| | RESET Low to data out Low on RD (pipelined) | 0.94 | 1.12 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.35 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.52 | 1.83 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.22 | 0.22 | ns |
| $t_{CYC}$ | Clock cycle time | 3.28 | 3.28 | ns |
| $F_{MAX}$ | Maximum clock frequency | 305 | 305 | MHz |

*Notes:*

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

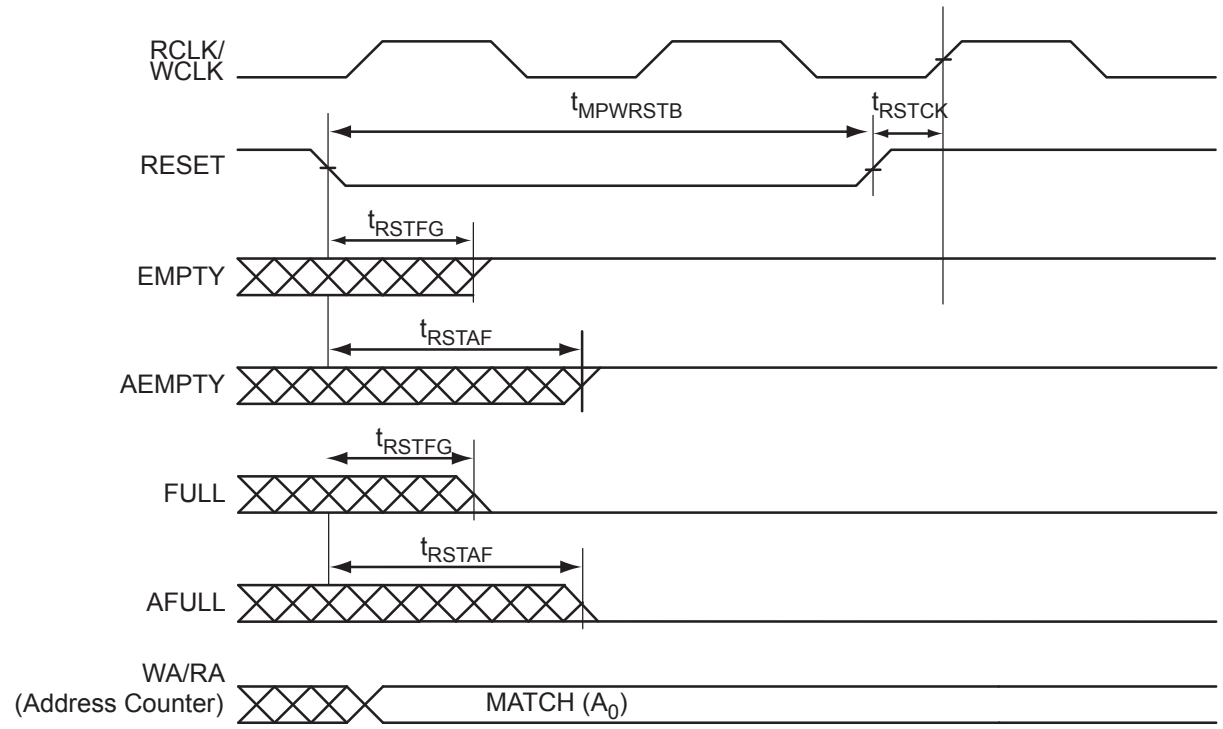



***Figure 2-38 •*** **FIFO Reset**

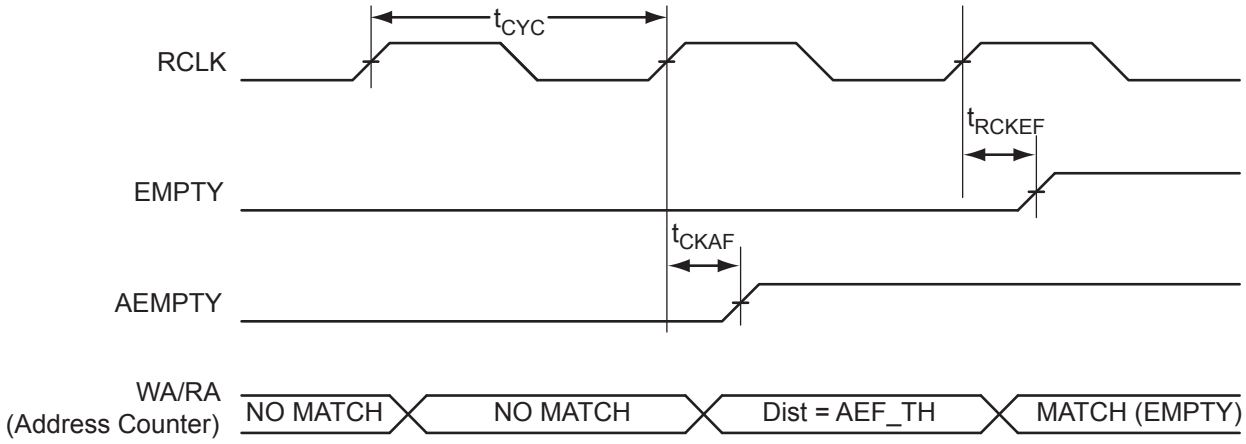



***Figure 2-39 •*** **FIFO EMPTY Flag and AEMPTY Flag Assertion**

## Temperature Monitor

Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion cSoC and the sensing diode are at the same temperature.

***Table 2-94 •*** **Temperature Monitor Performance Specifications**

| Specification | Test Conditions | Min. | Typical | Max. | Units |
|---|---|---|---|---|---|
| Input diode temperature range | | –55 | | 150 | °C |
| | | 233.2 | | 378.15 | K |
| Temperature sensitivity | | | 2.5 | | mV/K |
| Intercept | Extrapolated to 0K | | 0 | | V |
| Input referred temperature offset error | At 25°C (298.15K) | | ±1 | 1.5 | °C |
| Gain error | Slope of BFSL vs. 2.5 mV/K | | ±1 | 2.5 | % nom. |
| Overall accuracy | Peak error from ideal transfer function | | ±2 | ±3 | °C |
| Input referred noise | At 25°C (298.15K) – no output averaging | | 4 | | °C rms |
| Output current | Idle mode | | 100 | | µA |
| | Final measurement phases | | 10 | | µA |
| Analog settling time | Measured to 0.1% of final value, (with ADC load) | | | | |
| | From TM_STB (High) | 5 | | | µs |
| | From ADC_START (High) | 5 | | 105 | µs |
| AT parasitic capacitance | | | | 500 | pF |
| Power supply rejection ratio | DC (0–10 KHz) | 1.2 | 0.7 | | °C/V |
| Input referred temperature sensitivity error | Variation due to device temperature (–40°C to +100°C). External temperature sensor held constant. | | 0.005 | 0.008 | °C/°C |
| Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREFx) | VCC33A | | 200 | | µA |
| | VCC33AP | | 150 | | µA |
| | VCC15A | | 50 | | µA |

*Note: All results are based on averaging over 64 samples.*

# 3 – SmartFusion Development Tools

Designing with SmartFusion cSoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity.

## Types of Design Tools

Microsemi has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project (Figure 3-1).

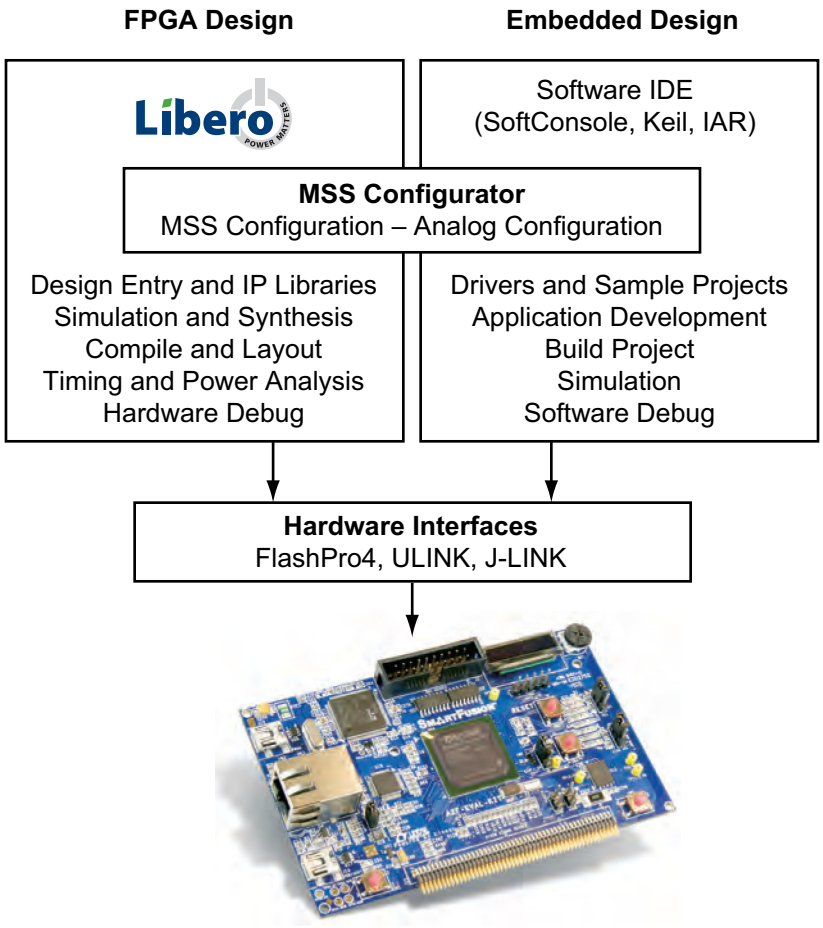



***Figure 3-1 •*** **Three Design Roles**

### FPGA Design

Libero System-on-Chip (SoC) software is Microsemi's comprehensive software toolset for designing with all Microsemi FPGAs and cSoCs. Libero SoC includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics®, as well as innovative timing and power optimization and analysis.

## Compile and Debug

Microsemi's SoftConsole is a free Eclipse-based IDE that enables the rapid production of C and C++ executables for Microsemi FPGA and cSoCs using Cortex-M3, Cortex-M1 and Core8051s. For SmartFusion support, SoftConsole includes the GNU C/C++ compiler and GDB debugger. Additional examples can be found on the SoftConsole page:

- Using UART with SmartFusion: SoftConsole Standalone Flow Tutorial
  - Design Files
- Displaying POT Level with LEDs: Libero SoC and SoftConsole Flow Tutorial for SmartFusion
  - Design Files

IAR Embedded Workbench® for ARM/Cortex is an integrated development environment for building and debugging embedded ARM applications using assembler, C and C++. It includes a project manager, editor, build and debugger tools with support for RTOS-aware debugging on hardware or in a simulator.

- Designing SmartFusion cSoC with IAR Systems
- IAR Embedded Workbench IDE User Guide for ARM
- Download Evaluation or Kickstart version of IAR Embedded Workbench for ARM

Keil's Microcontroller Development Kit comes in two editions: MDK-ARM and MDK Basic. Both editions feature µVision®, the ARM Compiler, MicroLib, and RTX, but the MDK Basic edition is limited to 256K so that small applications are more affordable.

- Designing SmartFusion cSoC with Keil
- Using Keil µVision and Microsemi SmartFusion cSoC
  - Programming file for use with this tutorial
- Keil Microcontroller Development Kit for ARM Product Manuals
- Download Evaluation version of Keil MDK-ARM

| CMSIS COMPLIANT ARM® Cortex™ Microcontroller Software Interface Standard | Microsemi | KEIL™ An ARM® Company | IAR SYSTEMS |
|---|---|---|---|
| **Software IDE** | **SoftConsole** | **Vision IDE** | **Embedded Workbench** |
| **Website** | www.microsemi.com/soc | www.keil.com | www.iar.com |
| **Free versions from SoC Products Group** | Free with Libero SoC | 32 K code limited | 32 K code limited |
| **Available from Vendor** | N/A | Full version | Full version |
| **Compiler** | GNU GCC | RealView C/C++ | IAR ARM Compiler |
| **Debugger** | GDB debug | Vision Debugger | C-SPY Debugger |
| **Instruction Set Simulator** | No | Vision Simulator | Yes |
| **Debug Hardware** | FlashPro4 | ULINK2 or ULINK-ME | J-LINK or J-LINK Lite |

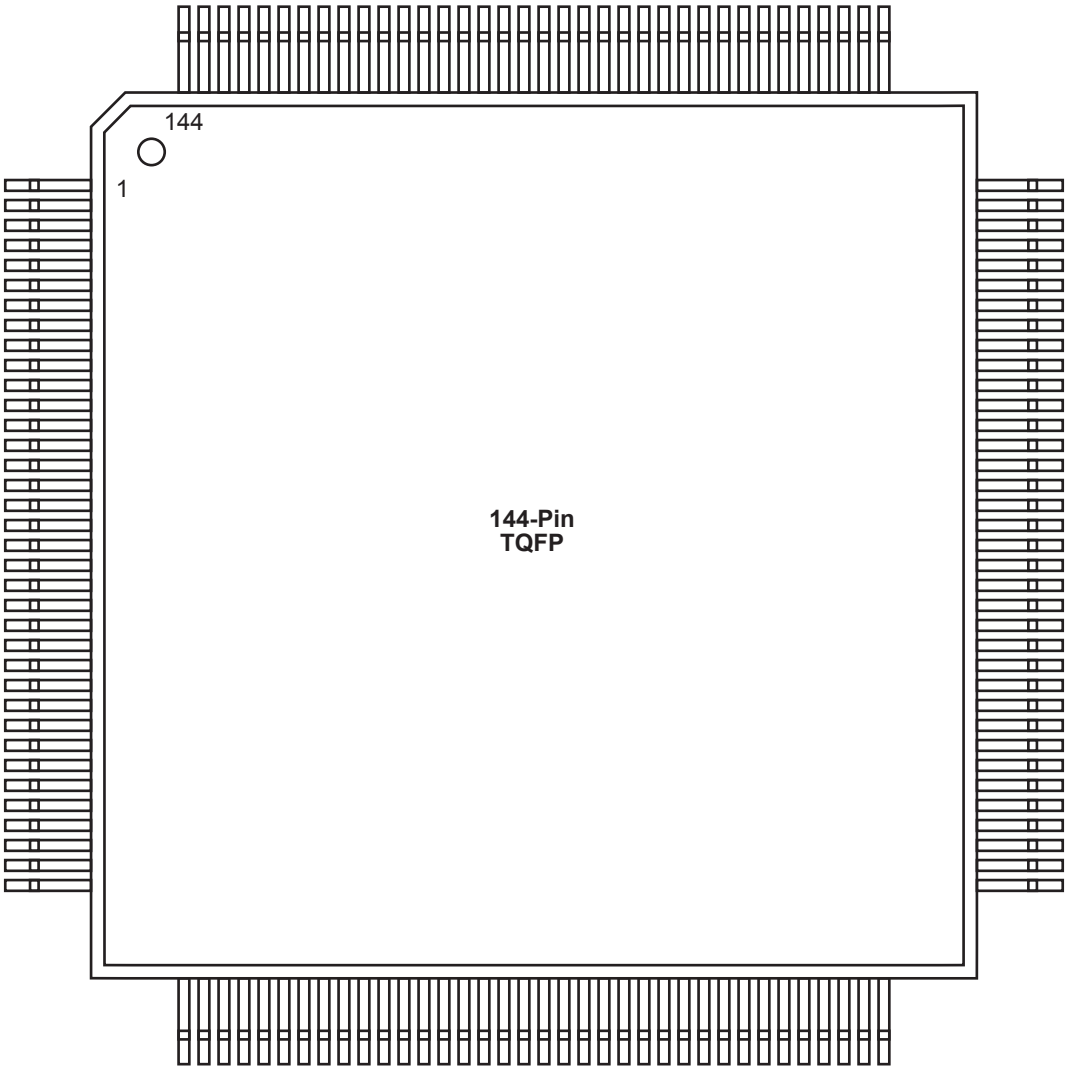
## Operating Systems

FreeRTOS™ is a portable, open source, royalty free, mini real-time kernel (a free-to-download and free-to-deploy RTOS that can be used in commercial applications without any requirement to expose your proprietary source code). FreeRTOS is scalable and designed specifically for small embedded systems. This FreeRTOS version ported by Microsemi is 6.0.1. For more information, visit the FreeRTOS website: www.freertos.org

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion cSoC: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

# Pin Assignment Tables

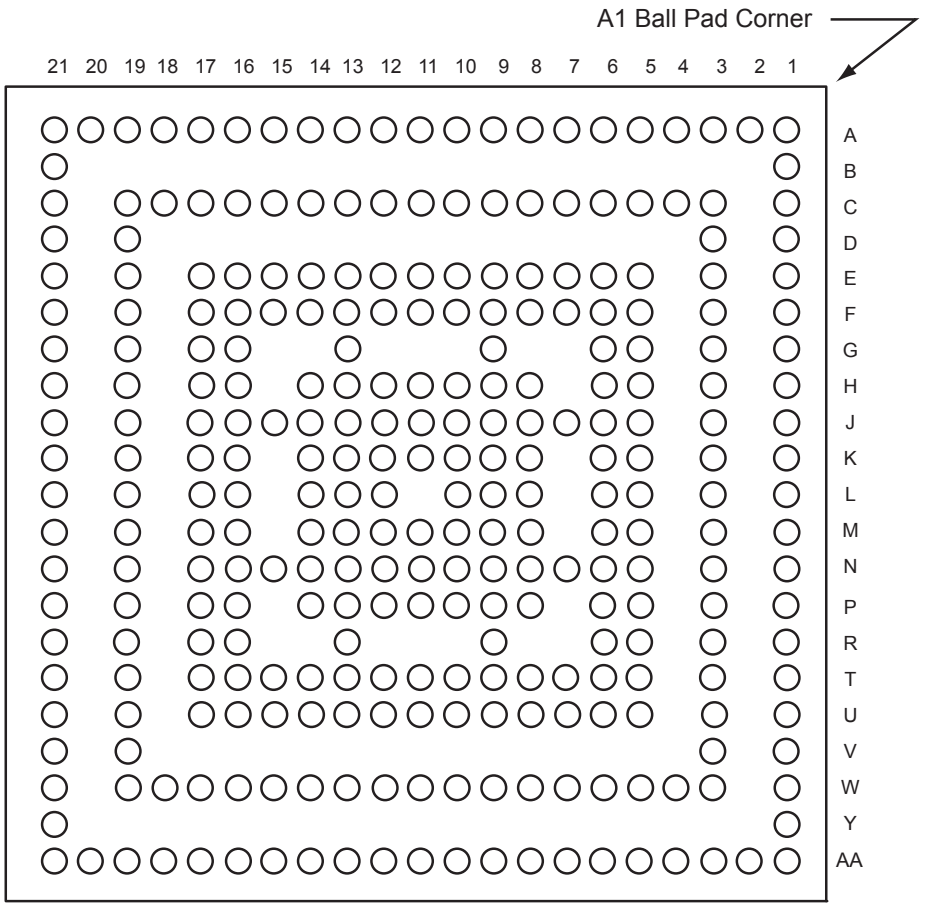
## TQ144




***Note***

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

# CS288




*Note: Bottom view*

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| K17 | GNDLPXTAL | GNDLPXTAL | GNDLPXTAL |
| K19 | GNDMAINXTAL | GNDMAINXTAL | GNDMAINXTAL |
| K21 | MAINXIN | MAINXIN | MAINXIN |
| L1 | GNDRCOSC | GNDRCOSC | GNDRCOSC |
| L3 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| L5 | EMC_DB[2]/IO37NPB5V0 | EMC_DB[2]/IO60NPB5V0 | EMC_DB[2]/IO77NPB5V0 |
| L6 | NC | GNDQ | GNDQ |
| L8 | VCC | VCC | VCC |
| L9 | GND | GND | GND |
| L10 | VCC | VCC | VCC |
| L12 | VCC | VCC | VCC |
| L13 | GND | GND | GND |
| L14 | VCC | VCC | VCC |
| L16 | VCCLPXTAL | VCCLPXTAL | VCCLPXTAL |
| L17 | VDDBAT | VDDBAT | VDDBAT |
| L19 | LPXIN | LPXIN | LPXIN |
| L21 | MAINXOUT | MAINXOUT | MAINXOUT |
| M1 | VCCRCOSC | VCCRCOSC | VCCRCOSC |
| M3 | MSS_RESET_N | MSS_RESET_N | MSS_RESET_N |
| M5 | GPIO_5/IO28RSB4V0 | GPIO_5/IO42RSB4V0 | GPIO_5/IO51RSB4V0 |
| M6 | GND | GND | GND |
| M8 | GND | GND | GND |
| M9 | VCC | VCC | VCC |
| M10 | GND | GND | GND |
| M11 | VCC | VCC | VCC |
| M12 | GND | GND | GND |
| M13 | VCC | VCC | VCC |
| M14 | GND | GND | GND |
| M16 | TMS | TMS | TMS |
| M17 | VJTAG | VJTAG | VJTAG |
| M19 | TDO | TDO | TDO |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| M21 | TRSTB | TRSTB | TRSTB |
| N1 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |
| N3 | GND | GND | GND |
| N5 | GPIO_4/IO29RSB4V0 | GPIO_4/IO43RSB4V0 | GPIO_4/IO52RSB4V0 |
| N6 | GPIO_8/IO25RSB4V0 | GPIO_8/IO39RSB4V0 | GPIO_8/IO48RSB4V0 |
| N7 | GPIO_9/IO24RSB4V0 | GPIO_9/IO38RSB4V0 | GPIO_9/IO47RSB4V0 |
| N8 | VCC | VCC | VCC |
| N9 | GND | GND | GND |
| N10 | VCC | VCC | VCC |
| N11 | GND | GND | GND |
| N12 | VCC | VCC | VCC |
| N13 | GND | GND | GND |
| N14 | VCC | VCC | VCC |
| N15 | GND | GND | GND |
| N16 | TCK | TCK | TCK |
| N17 | TDI | TDI | TDI |
| N19 | GNDENVM | GNDENVM | GNDENVM |
| N21 | VCCENVM | VCCENVM | VCCENVM |
| P1 | GPIO_0/IO33RSB4V0 | MAC_MDC/IO48RSB4V0 | MAC_MDC/IO57RSB4V0 |
| P3 | GPIO_7/IO26RSB4V0 | GPIO_7/IO40RSB4V0 | GPIO_7/IO49RSB4V0 |
| P5 | GPIO_6/IO27RSB4V0 | GPIO_6/IO41RSB4V0 | GPIO_6/IO50RSB4V0 |
| P6 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |
| P8 | GND | GND | GND |
| P9 | VCC | VCC | VCC |
| P10 | GND | GND | GND |
| P11 | VCC | VCC | VCC |
| P12 | GND | GND | GND |
| P13 | VCC | VCC | VCC |
| P14 | GND | GND | GND |
| P16 | JTAGSEL | JTAGSEL | JTAGSEL |
| P17 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| W14 | ADC5 | CM2 | CM2 |
| W15 | NC | ABPS5 | ABPS5 |
| W16 | GNDAQ | GNDAQ | GNDAQ |
| W17 | NC | VCC33SDD1 | VCC33SDD1 |
| W18 | NC | GNDSDD1 | GNDSDD1 |
| W19 | PTBASE | PTBASE | PTBASE |
| W21 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 |
| Y1 | VCC33AP | VCC33AP | VCC33AP |
| Y21 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060 Function | A2F200 Function | A2F500 Function |
| F14 | IO21NDB1V0 | GCB0/IO27NDB1V0 | GCB0/IO34NDB1V0 |
| F15 | GND | GND | GND |
| F16 | VCCENVM | VCCENVM | VCCENVM |
| G1 | EMC_DB[8]/IO40NDB5V0 | EMC_DB[8]/GEC0/IO63NDB5V0 | EMC_DB[8]/GEC0/IO80NDB5V0 |
| G2 | EMC_DB[7]/IO39PDB5V0 | EMC_DB[7]/GEB1/IO62PDB5V0 | EMC_DB[7]/GEB1/IO79PDB5V0 |
| G3 | EMC_DB[6]/IO39NDB5V0 | EMC_DB[6]/GEB0/IO62NDB5V0 | EMC_DB[6]/GEB0/IO79NDB5V0 |
| G4 | GFC2/IO41PDB5V0 | GFC2/IO67PDB5V0 | GFC2/IO84PDB5V0 |
| G5 | IO41NDB5V0 | IO67NDB5V0 | IO84NDB5V0 |
| G6 | GND | GND | GND |
| G7 | VCC | VCC | VCC |
| G8 | GND | GND | GND |
| G9 | VCC | VCC | VCC |
| G10 | GND | GND | GND |
| G11 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| G12 | VPP | VPP | VPP |
| G13 | TRSTB | TRSTB | TRSTB |
| G14 | TMS | TMS | TMS |
| G15 | TCK | TCK | TCK |
| G16 | GNDENVM | GNDENVM | GNDENVM |
| H1 | GND | GND | GND |
| H2 | EMC_DB[5]/IO38PPB5V0 | EMC_DB[5]/GEA1/IO61PPB5V0 | EMC_DB[5]/GEA1/IO78PPB5V0 |
| H3 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| H4 | EMC_DB[1]/IO36PDB5V0 | EMC_DB[1]/GEB2/IO59PDB5V0 | EMC_DB[1]/GEB2/IO76PDB5V0 |
| H5 | EMC_DB[0]/IO36NDB5V0 | EMC_DB[0]/GEA2/IO59NDB5V0 | EMC_DB[0]/GEA2/IO76NDB5V0 |
| H6 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| H7 | GND | GND | GND |
| H8 | VCC | VCC | VCC |
| H9 | GND | GND | GND |
| H10 | VCC | VCC | VCC |
| H11 | GND | GND | GND |
| H12 | VJTAG | VJTAG | VJTAG |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| H7 | GND | GND |
| H8 | VCC | VCC |
| H9 | GND | GND |
| H10 | VCC | VCC |
| H11 | GND | GND |
| H12 | VCC | VCC |
| H13 | GND | GND |
| H14 | VCC | VCC |
| H15 | GND | GND |
| H16 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| H17 | IO25NDB1V0 | IO29NDB1V0 |
| H18 | GCC2/IO25PDB1V0 | GCC2/IO29PDB1V0 |
| H19 | GND | GND |
| H20 | GCC0/IO26NPB1V0 | GCC0/IO35NPB1V0 |
| H21 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| H22 | GCB0/IO27NDB1V0 | GCB0/IO34NDB1V0 |
| J1 | EMC_DB[6]/GEB0/IO62NDB5V0 | EMC_DB[6]/GEB0/IO79NDB5V0 |
| J2 | EMC_DB[5]/GEA1/IO61PDB5V0 | EMC_DB[5]/GEA1/IO78PDB5V0 |
| J3 | EMC_DB[4]/GEA0/IO61NDB5V0 | EMC_DB[4]/GEA0/IO78NDB5V0 |
| J4 | EMC_DB[3]/GEC2/IO60PPB5V0 | EMC_DB[3]/GEC2/IO77PPB5V0 |
| J5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| J6 | GFA0/IO64NDB5V0 | GFA0/IO81NDB5V0 |
| J7 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| J8 | GND | GND |
| J9 | VCC | VCC |
| J10 | GND | GND |
| J11 | VCC | VCC |
| J12 | GND | GND |
| J13 | VCC | VCC |
| J14 | GND | GND |
| J15 | VCC | VCC |
| J16 | GND | GND |
| J17 | NC | IO37PDB1V0 |
| J18 | VCCFPGAIOB1 | VCCFPGAIOB1 |

*Notes:*

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*