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Details

| | |
|----------------------------|---|
| Product Status | Obsolete |
| Core Processor | HC08 |
| Core Size | 8-Bit |
| Speed | 2MHz |
| Connectivity | - |
| Peripherals | LVD, POR, PWM |
| Number of I/O | 5 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | 8-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mchlc908qt4cpe |

Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

| Date | Revision Level | Description | Page Number(s) |
|---------------|----------------|--|--|
| August, 2003 | N/A | Initial release | N/A |
| October, 2003 | 1.0 | Figure 2-2. Control, Status, and Data Registers Deleted unimplemented areas from \$FFB0–\$FFBD and \$FFC2–\$FFCF as they are actually available. Also corrected \$FFBF designation from unimplemented to reserved. | 26 |
| | | Figure 6-1. COP Block Diagram — Reworked for clarity | 57 |
| | | 6.3.2 STOP Instruction — Added subsection for STOP instruction | 58 |
| | | 13.4.2 Active Resets from Internal Sources — Reworked notes for clarity. | 115 |
| | | 15.3 Monitor Module (MON) — Clarified seventh bullet. | 154 |
| | | 16.5 DC Electrical Characteristics — Corrected notes 4 and 5. | 169 |
| | | 16.6 Control Timing — Updated values for $\overline{\text{RST}}$ input pulse width low and $\overline{\text{IRQ}}$ interrupt pulse width low | 170 |
| January, 2004 | 2.0 | Figure 2-2. Control, Status, and Data Registers — Corrected reset state for the FLASH Block Protect Register at address location \$FFBE and the Internal Oscillator Trim Value at \$FFC0. | 30 |
| | | Figure 2-5. FLASH Block Protect Register (FLBPR) — Restated reset state for clarity. | 37 |
| July, 2005 | 3.0 | Reformatted to meet current documentation standards | Throughout |
| | | Chapter 7 Central Processor Unit (CPU) — In 7.7 Instruction Set Summary : Reworked definitions for STOP instruction Added WAIT instruction | 70 71 |
| | | 13.8.1 SIM Reset Status Register — Clarified SRSR flag setting. | 117 |
| | | 14.9.1 TIM Status and Control Register — Added information to TSTOP note. | 127 |
| | | 17.3 Package Dimensions — Updated package information. | 163 |

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Chapter 7

Central Processor Unit (CPU)

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Memory

| Addr. | Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|-----------------------|---|--------|--|-----------------|-------|-------|-------|------------|-------|----------------|
| \$FE0B | Break Status and Control Register (BRKSCR) See page 138. | Read: | BRKE | BRKA | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$FE0C | LVI Status Register (LVISR) See page 87. | Read: | LVIOUT | 0 | 0 | 0 | 0 | 0 | 0 | R |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$FE0D ↓ \$FE0F | Reserved for FLASH Test | | R | R | R | R | R | R | R | R |
| \$FFBE | FLASH Block Protect Register (FLBPR) See page 37. | Read: | BPR7 | BPR6 | BPR5 | BPR4 | BPR3 | BPR2 | BPR1 | BPR0 |
| | | Write: | | | | | | | | |
| | | Reset: | Unaffected by reset | | | | | | | |
| \$FFBF | Reserved | | R | R | R | R | R | R | R | R |
| \$FFC0 | Internal Oscillator Trim Value (Optional) | Read: | TRIM7 | TRIM6 | TRIM5 | TRIM4 | TRIM3 | TRIM2 | TRIM1 | TRIM0 |
| | | Write: | | | | | | | | |
| | | Reset: | Unaffected by reset | | | | | | | |
| \$FFC1 | Reserved | | R | R | R | R | R | R | R | R |
| \$FFFF | COP Control Register (COPCTL) See page 59. | Read: | LOW BYTE OF RESET VECTOR | | | | | | | |
| | | Write: | WRITING CLEARS COP COUNTER (ANY VALUE) | | | | | | | |
| | | Reset: | Unaffected by reset | | | | | | | |
| | | | | = Unimplemented | | | R | = Reserved | | U = Unaffected |

Figure 2-2. Control, Status, and Data Registers (Sheet 6 of 6)

3.3.3 Conversion Time

Sixteen ADC internal clocks are required to perform one conversion. The ADC starts a conversion on the first rising edge of the ADC internal clock immediately following a write to the ADSCR. If the ADC internal clock is selected to run at 1 MHz, then one conversion will take 16 μ s to complete. With a 1-MHz ADC internal clock the maximum sample rate is 62.5 kHz.

$$\text{Conversion Time} = \frac{16 \text{ ADC Clock Cycles}}{\text{ADC Clock Frequency}}$$

$$\text{Number of Bus Cycles} = \text{Conversion Time} \times \text{Bus Frequency}$$

3.3.4 Continuous Conversion

In the continuous conversion mode (ADCO = 1), the ADC continuously converts the selected channel filling the ADC data register (ADR) with new data after each conversion. Data from the previous conversion will be overwritten whether that data has been read or not. Conversions will continue until the ADCO bit is cleared. The COCO bit (ADSCR, \$003C) is set after each conversion and will stay set until the next read of the ADC data register.

When a conversion is in process and the ADSCR is written, the current conversion data should be discarded to prevent an incorrect reading.

3.3.5 Accuracy and Precision

The conversion process is monotonic and has no missing codes.

3.4 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a central processor unit (CPU) interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit is at 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled.

3.5 Low-Power Modes

The following subsections describe the ADC in low-power modes.

3.5.1 Wait Mode

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the microcontroller unit (MCU) out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting the CH[4:0] bits in ADSCR to 1s before executing the WAIT instruction.

3.5.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode. Allow one conversion cycle to stabilize the analog circuitry before using ADC data after exiting stop mode.



6.3.7 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register 1 (CONFIG1). See [Chapter 5 Configuration Register \(CONFIG\)](#).

6.4 COP Control Register

The COP control register (COPCTL) is located at address \$FFFF and overlaps the reset vector. Writing any value to \$FFFF clears the COP counter and starts a new timeout period. Reading location \$FFFF returns the low byte of the reset vector.

| | | | | | | | | |
|-----------------|--------------------------|---|---|---|---|---|---|-------|
| Address: \$FFFF | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Read: | LOW BYTE OF RESET VECTOR | | | | | | | |
| Write: | CLEAR COP COUNTER | | | | | | | |
| Reset: | Unaffected by reset | | | | | | | |

Figure 6-2. COP Control Register (COPCTL)

6.5 Interrupts

The COP does not generate CPU interrupt requests.

6.6 Monitor Mode

The COP is disabled in monitor mode when V_{TST} is present on the \overline{IRQ} pin.

6.7 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

6.7.1 Wait Mode

The COP continues to operate during wait mode. To prevent a COP reset during wait mode, periodically clear the COP counter.

6.7.2 Stop Mode

Stop mode turns off the BUSCLKX4 input to the COP and clears the SIM counter. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

6.8 COP Module During Break Mode

The COP is disabled during a break interrupt with monitor mode when BDCOP bit is set in break auxiliary register (BRKAR).

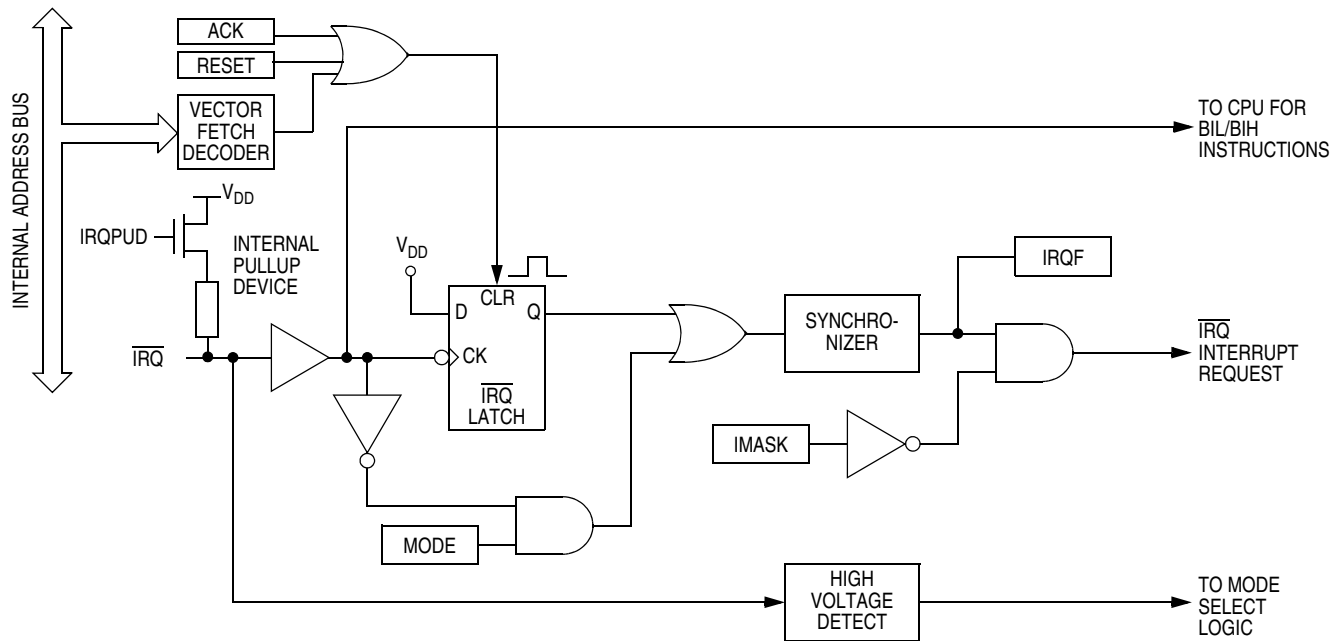


Figure 8-2. IRQ Module Block Diagram

8.3.1 MODE = 1

If the MODE bit is set, the $\overline{\text{IRQ}}$ pin is both falling edge sensitive and low level sensitive. With MODE set, both of the following actions must occur to clear the $\overline{\text{IRQ}}$ interrupt request:

- Return of the $\overline{\text{IRQ}}$ pin to a high level. As long as the $\overline{\text{IRQ}}$ pin is low, the IRQ request remains active.
- IRQ vector fetch or software clear. An IRQ vector fetch generates an interrupt acknowledge signal to clear the IRQ latch. Software generates the interrupt acknowledge signal by writing a 1 to ACK in INTSCR. The ACK bit is useful in applications that poll the $\overline{\text{IRQ}}$ pin and require software to clear the IRQ latch. Writing to ACK prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACK does not affect subsequent transitions on the $\overline{\text{IRQ}}$ pin. A falling edge that occurs after writing to ACK latches another interrupt request. If the IRQ mask bit, IMASK, is clear, the CPU loads the program counter with the IRQ vector address.

The IRQ vector fetch or software clear and the return of the $\overline{\text{IRQ}}$ pin to a high level may occur in any order. The interrupt request remains pending as long as the $\overline{\text{IRQ}}$ pin is low. A reset will clear the IRQ latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

Use the BIH or BIL instruction to read the logic level on the $\overline{\text{IRQ}}$ pin.

8.3.2 MODE = 0

If the MODE bit is clear, the $\overline{\text{IRQ}}$ pin is falling edge sensitive only. With MODE clear, an IRQ vector fetch or software clear immediately clears the IRQ latch.

The IRQF bit in INTSCR can be read to check for pending interrupts. The IRQF bit is not affected by IMASK, which makes it useful in applications where polling is preferred.

NOTE

When using the level-sensitive interrupt trigger, avoid false IRQ interrupts by masking interrupt requests in the interrupt routine.

Low-Voltage Inhibit (LVI)

The LVI is enabled out of reset. The LVI module contains a bandgap reference circuit and comparator. Clearing the LVI power disable bit (LVIPWRD) enables the LVI to monitor V_{DD} voltage. Clearing the LVI reset disable bit (LVIRSTD) enables the LVI module to generate a reset when V_{DD} falls below a voltage, V_{TRIPF} or V_{DTRIPF} . Setting the LVI enable in stop mode bit (LVISTOP) enables the LVI to operate in stop mode. Setting the LVD or LVR trip point bit (LVDLVR) selects the LVD trip point voltage. The actual trip thresholds are specified in [16.5 DC Electrical Characteristics](#). Either trip level can be used as a detect or reset.

NOTE

After a power-on reset, the LVI's default mode of operation is LVR trip voltage. If a higher trip voltage is desired, the user must set the LVDLVR bit to raise the trip point to the LVD voltage.

If the user requires the higher trip voltage and sets the LVDLVR bit after power-on reset while the V_{DD} supply is not above the V_{TRIPR} for LVD mode, the microcontroller unit (MCU) will immediately go into reset. The next time the LVI releases the reset, the supply will be above the V_{TRIPR} for LVD mode.

Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR} , which causes the MCU to exit reset. See [Chapter 13 System Integration Module \(SIM\)](#) for the reset recovery sequence.

The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR) and can be used for polling LVI operation when the LVI reset is disabled.

10.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be cleared to enable the LVI module, and the LVIRSTD bit must be set to disable LVI resets.

10.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, the LVIPWRD and LVIRSTD bits must be cleared to enable the LVI module and to enable LVI resets.

10.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR} . This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF} . V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS} .

10.3.4 LVI Trip Selection

The LVDLVR bit in the configuration register selects whether the LVI is configured for LVD (low voltage detect) or LVR (low voltage reset) protection. The LVD trip voltage can be used as a low voltage warning. The LVR trip voltage will commonly be configured as a reset condition since it is very close to the minimum operating voltage of the device. The LVDLVR bit can be written to anytime so that battery applications can make use of the LVI as both a warning indicator and to generate a system reset.

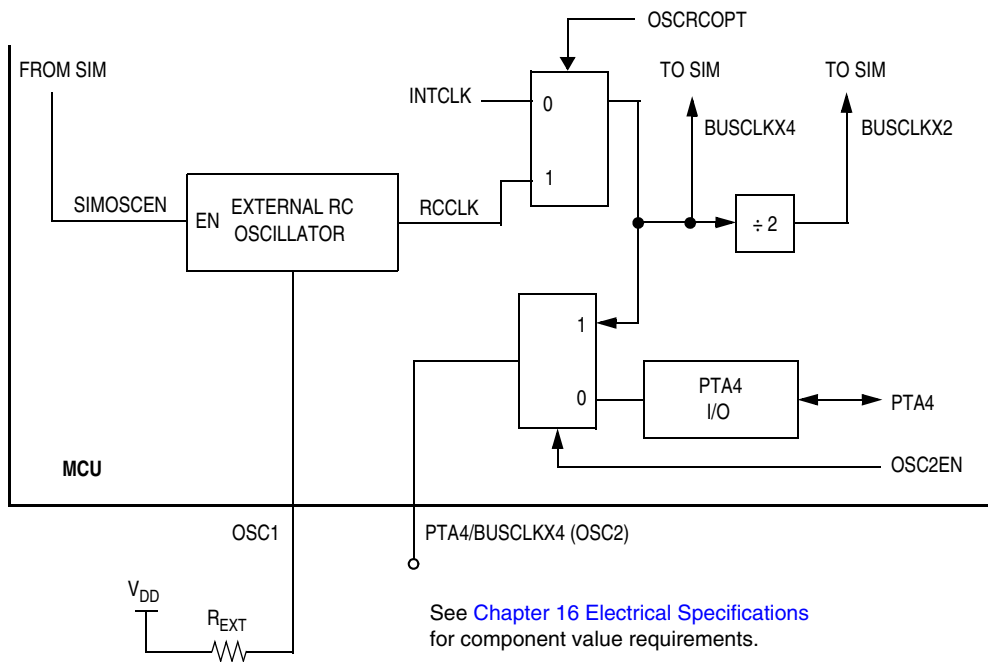


Figure 11-3. RC Oscillator External Connections

11.4 Oscillator Module Signals

The following paragraphs describe the signals that are inputs to and outputs from the oscillator module.

11.4.1 Crystal Amplifier Input Pin (OSC1)

The OSC1 pin is either an input to the crystal oscillator amplifier, an input to the RC oscillator circuit, or an external clock source.

For the internal oscillator configuration, the OSC1 pin can assume other functions according to [Table 1-3. Function Priority in Shared Pins](#).

11.4.2 Crystal Amplifier Output Pin (OSC2/PTA4/BUSCLKX4)

For the XTAL oscillator device, the OSC2 pin is the crystal oscillator inverting amplifier output.

For the external clock option, the OSC2 pin is dedicated to the PTA4 I/O function. The OSC2EN bit has no effect.

For the internal oscillator or RC oscillator options, the OSC2 pin can assume other functions according to [Table 1-3. Function Priority in Shared Pins](#), or the output of the oscillator clock (BUSCLKX4).

Table 11-1. OSC2 Pin Function

| Option | OSC2 Pin Function |
|--|--|
| XTAL oscillator | Inverting OSC1 |
| External clock | PTA4 I/O |
| Internal oscillator or RC oscillator | Controlled by OSC2EN bit in PTAPUE register OSC2EN = 0: PTA4 I/O OSC2EN = 1: BUSCLKX4 output |

12.3.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output. Writing a 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a 0 disables the output buffer.

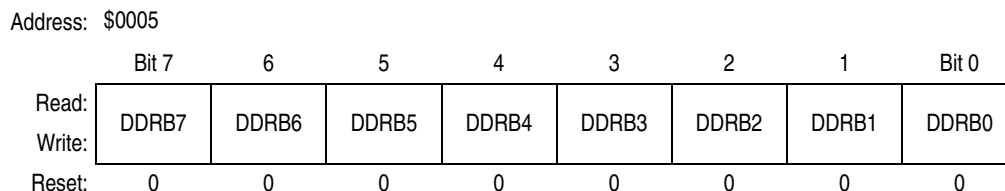


Figure 12-6. Data Direction Register B (DDRB)

DDRB[7:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[7:0], configuring all port B pins as inputs.

- 1 = Corresponding port B pin configured as output
- 0 = Corresponding port B pin configured as input

NOTE

Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1. [Figure 12-7](#) shows the port B I/O logic.

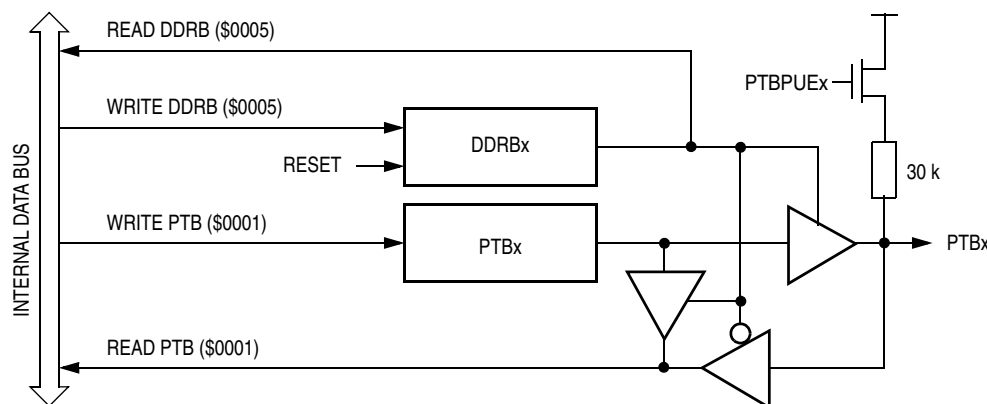


Figure 12-7. Port B I/O Circuit

When DDRBx is a 1, reading address \$0001 reads the PTBx data latch. When DDRBx is a 0, reading address \$0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. [Table 12-2](#) summarizes the operation of the port B pins.

Table 12-2. Port B Pin Functions

| DDRB Bit | PTB Bit | I/O Pin Mode | Accesses to DDRB | Accesses to PTB | |
|----------|------------------|----------------------------|------------------|-----------------|--------------------------|
| | | | Read/Write | Read | Write |
| 0 | X ⁽¹⁾ | Input, Hi-Z ⁽²⁾ | DDRB7–DDRB0 | Pin | PTB7–PTB0 ⁽³⁾ |
| 1 | X | Output | DDRB7–DDRB0 | Pin | PTB7–PTB0 |

1. X = don't care

2. Hi-Z = high impedance

3. Writing affects data register, but does not affect the input.

The LDA opcode is prefetched by both the INT1 and INT2 return-from-interrupt (RTI) instructions. However, in the case of the INT1 RTI prefetch, this is a redundant operation.

NOTE

To maintain compatibility with the M6805 Family, the H register is not pushed on the stack during interrupt entry. If the interrupt service routine modifies the H register or uses the indexed addressing mode, software should save the H register and then restore it prior to exiting the routine.

13.6.1.2 SWI Instruction

The SWI instruction is a non-maskable instruction that causes an interrupt regardless of the state of the interrupt mask (I bit) in the condition code register.

NOTE

*A software interrupt pushes PC onto the stack. A software interrupt does **not** push PC – 1, as a hardware interrupt does.*

13.6.2 Interrupt Status Registers

The flags in the interrupt status registers identify maskable interrupt sources. [Table 13-3](#) summarizes the interrupt sources and the interrupt status register flags that they set. The interrupt status registers can be useful for debugging.

Table 13-3. Interrupt Sources

| Priority | Source | Flag | Mask ⁽¹⁾ | INT Register Flag | Vector Address |
|-----------------------------|-----------------------------------|------|---------------------|-------------------|----------------|
| Highest ↑ ↓ Lowest | Reset | — | — | — | \$FFFE–\$FFFF |
| | SWI instruction | — | — | — | \$FFFC–\$FFFD |
| | IRQ pin | IRQF | IMASK | IF1 | \$FFFA–\$FFFB |
| | Timer channel 0 interrupt | CH0F | CH0IE | IF3 | \$FFF6–\$FFF7 |
| | Timer channel 1 interrupt | CH1F | CH1IE | IF4 | \$FFF4–\$FFF5 |
| | Timer overflow interrupt | TOF | TOIE | IF5 | \$FFF2–\$FFF3 |
| | Keyboard interrupt | KEYF | IMASKK | IF14 | \$FFE0–\$FFE1 |
| | ADC conversion complete interrupt | COCO | AIEN | IF15 | \$FFDE–\$FFDF |

1. The I bit in the condition code register is a global mask for all interrupt sources except the SWI instruction.

13.6.2.1 Interrupt Status Register 1

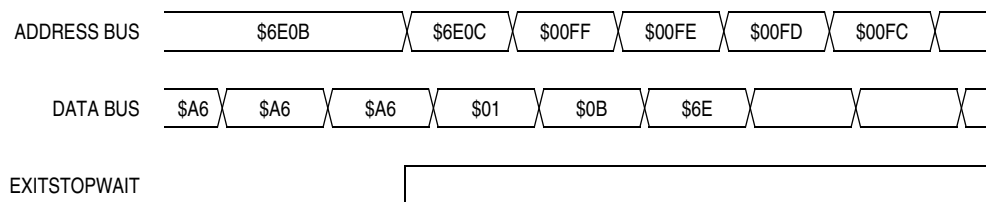
Address: \$FE04

| | | | | | | | | |
|--------|-------|-----|-----|-----|---|-----|---|-------|
| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Read: | 0 | IF5 | IF4 | IF3 | 0 | IF1 | 0 | 0 |
| Write: | R | R | R | R | R | R | R | R |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

R = Reserved

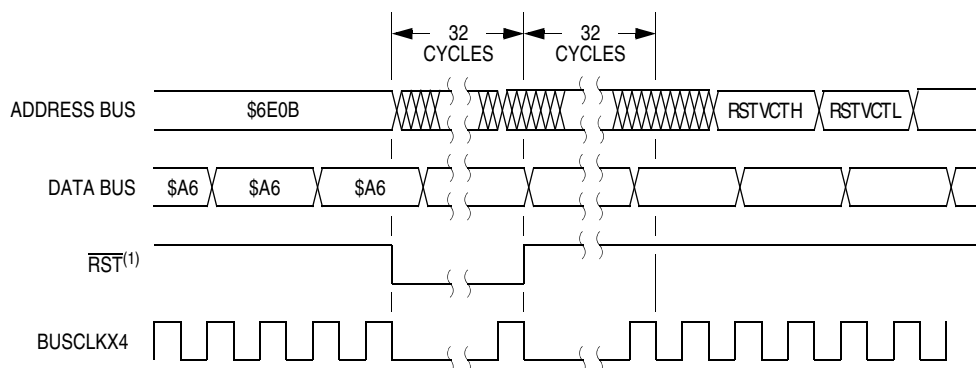
Figure 13-11. Interrupt Status Register 1 (INT1)

Figure 13-15 and Figure 13-16 show the timing for wait recovery.



NOTE: EXITSTOPWAIT = $\overline{\text{RST}}$ pin OR CPU interrupt

Figure 13-15. Wait Recovery from Interrupt



1. $\overline{\text{RST}}$ is only available if the RSTEN bit in the CONFIG1 register is set.

Figure 13-16. Wait Recovery from Internal Reset

13.7.2 Stop Mode

In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

The SIM disables the oscillator signals (BUSCLKX2 and BUSCLKX4) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register 1 (CONFIG1). If SSREC is set, stop recovery is reduced from the normal delay of 4096 BUSCLKX4 cycles down to 32. This is ideal for the internal oscillator, RC oscillator, and external oscillator options which do not require long start-up times from stop mode.

NOTE

External crystal applications should use the full stop recovery time by clearing the SSREC bit.

control the output are the ones written to last. TSC0 controls and monitors the buffered output compare function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

NOTE

In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.

14.4.4 Pulse Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM can generate a PWM signal. The value in the TIM counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM counter modulo registers. The time between overflows is the period of the PWM signal.

As [Figure 14-3](#) shows, the output compare value in the TIM channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM to clear the channel pin on output compare if the state of the PWM pulse is logic 1 (ELSxA = 0). Program the TIM to set the pin if the state of the PWM pulse is logic 0 (ELSxA = 1).

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing \$00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is 000. See [14.9.1 TIM Status and Control Register](#).

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing \$0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50%.

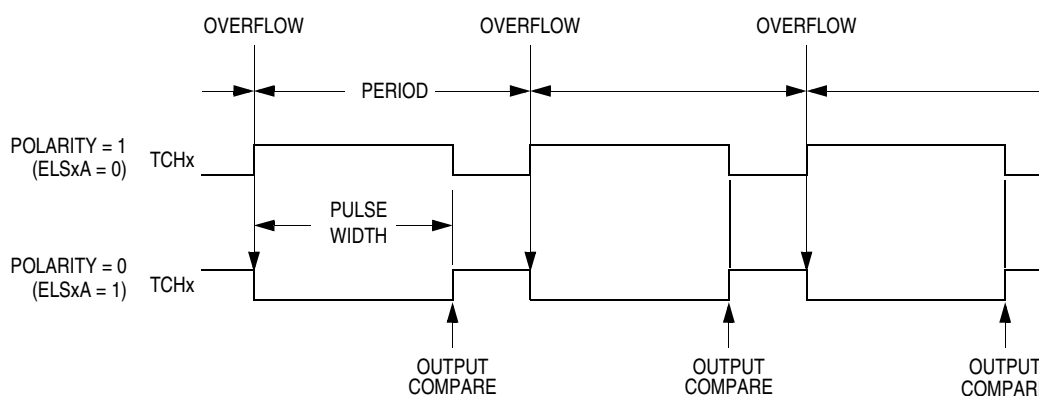


Figure 14-3. PWM Period and Pulse Width

14.6 Wait Mode

The WAIT instruction puts the MCU in low power-consumption standby mode.

The TIM remains active after the execution of a WAIT instruction. In wait mode the TIM registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

14.7 TIM During Break Interrupts

A break interrupt stops the TIM counter.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See [13.8.2 Break Flag Control Register](#).

To allow software to clear status bits during a break interrupt, write a 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at 0. After the break, doing the second step clears the status bit.

14.8 Input/Output Signals

Port A shares three of its pins with the TIM. Two TIM channel I/O pins are PTA0/TCH0 and PTA1/TCH1 and an alternate clock source is PTA2/TCLK.

14.8.1 TIM Clock Pin (PTA2/TCLK)

PTA2/TCLK is an external clock input that can be the clock source for the TIM counter instead of the prescaled internal bus clock. Select the PTA2/TCLK input by writing 1s to the three prescaler select bits, PS[2–0]. (See [14.9.1 TIM Status and Control Register](#).) When the PTA2/TCLK pin is the TIM clock input, it is an input regardless of port pin initialization.

14.8.2 TIM Channel I/O Pins (PTA0/TCH0 and PTA1/TCH1)

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. PTA0/TCH0 can be configured as a buffered output compare or buffered PWM pin.

14.9 Input/Output Registers

The following I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM counter registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0 and TSC1)
- TIM channel registers (TCH0H:TCH0L and TCH1H:TCH1L)

15.3.1.2 Forced Monitor Mode

If entering monitor mode without high voltage on $\overline{\text{IRQ}}$, then startup port pin requirements and conditions, (PTA1/PTA4) are not in effect. This is to reduce circuit requirements when performing in-circuit programming.

NOTE

If the reset vector is blank and monitor mode is entered, the chip will see an additional reset cycle after the initial power-on reset (POR). Once the reset vector has been programmed, the traditional method of applying a voltage, V_{TST} , to $\overline{\text{IRQ}}$ must be used to enter monitor mode.

If monitor mode was entered as a result of the reset vector being blank, the COP is always disabled regardless of the state of $\overline{\text{IRQ}}$.

If the voltage applied to the $\overline{\text{IRQ}}$ is less than V_{TST} , the MCU will come out of reset in user mode. Internal circuitry monitors the reset vector fetches and will assert an internal reset if it detects that the reset vectors are erased (\$FF). When the MCU comes out of reset, it is forced into monitor mode without requiring high voltage on the $\overline{\text{IRQ}}$ pin. Once out of reset, the monitor code is initially executing with the internal clock at its default frequency.

If $\overline{\text{IRQ}}$ is held high, all pins will default to regular input port functions except for PTA0 and PTA5 which will operate as a serial communication port and OSC1 input respectively (refer to Figure 15-11). That will allow the clock to be driven from an external source through OSC1 pin.

If $\overline{\text{IRQ}}$ is held low, all pins will default to regular input port function except for PTA0 which will operate as serial communication port. Refer to Figure 15-12.

Regardless of the state of the $\overline{\text{IRQ}}$ pin, it will not function as a port input pin in monitor mode. Bit 2 of the Port A data register will always read 0. The BIH and BIL instructions will behave as if the $\overline{\text{IRQ}}$ pin is enabled, regardless of the settings in the configuration register. See Chapter 5 Configuration Register (CONFIG).

The COP module is disabled in forced monitor mode. Any reset other than a power-on reset (POR) will automatically force the MCU to come back to the forced monitor mode.

15.3.1.3 Monitor Vectors

In monitor mode, the MCU uses different vectors for reset, SWI (software interrupt), and break interrupt than those for user mode. The alternate vectors are in the \$FE page instead of the \$FF page and allow code execution from the internal monitor firmware instead of user code.

NOTE

Exiting monitor mode after it has been initiated by having a blank reset vector requires a power-on reset (POR). Pulling $\overline{\text{RST}}$ (when $\overline{\text{RST}}$ pin available) low will not exit monitor mode in this situation.

Table 15-2 summarizes the differences between user mode and monitor mode regarding vectors.

Table 15-2. Mode Difference

| Modes | Functions | | | | | |
|---------|-------------------|------------------|-------------------|------------------|-----------------|----------------|
| | Reset Vector High | Reset Vector Low | Break Vector High | Break Vector Low | SWI Vector High | SWI Vector Low |
| User | \$FFFE | \$FFFF | \$FFFC | \$FFFD | \$FFFC | \$FFFD |
| Monitor | \$FEFE | \$FEFF | \$FEFC | \$FEFD | \$FEFC | \$FEFD |

Electrical Specifications

| Characteristic ⁽¹⁾ | Symbol | Min | Typ ⁽²⁾ | Max | Unit |
|---|--------------|------|--------------------|------|------|
| Low-voltage inhibit reset, trip falling voltage (LVR) | V_{TRIPF} | 2.00 | 2.12 | 2.24 | V |
| Low-voltage inhibit reset, trip rising voltage (LVR) | V_{TRIPR} | 2.04 | 2.18 | 2.30 | V |
| Low-voltage inhibit reset/recover hysteresis | V_{HYS} | — | 60 | — | mV |
| Low-voltage detect, trip falling voltage (LVD) | V_{DTRIPF} | 2.20 | 2.32 | 2.44 | V |
| Low-voltage detect, trip rising voltage (LVD) | V_{DTRIPR} | 2.21 | 2.33 | 2.45 | V |
| Low-voltage detect reset/recover hysteresis | V_{DHYS} | — | 10 | — | mV |

1. $V_{DD} = V_{DDMIN}$ to V_{DDMAX} , $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H , unless otherwise noted.

2. Typical values reflect average measurements at $V_{DD} = 3.0$ V, 25°C only.

3. Maximum is highest voltage that POR is guaranteed.

4. If minimum V_{DD} is not reached before the internal POR reset is released, the LVI will hold the part in reset until minimum V_{DD} is reached.

5. R_{PU} is measured at $V_{DD} = 3.0$ V.

16.6 Control Timing

| Characteristic ⁽¹⁾ | Symbol | Min | Max | Unit |
|---|------------------------|---------------------|-----|-----------|
| Internal operating frequency | f_{OP} (f_{Bus}) | — | 2 | MHz |
| Internal clock period ($1/f_{OP}$) | t_{cyc} | 500 | — | ns |
| \overline{RST} input pulse width low | t_{RL} | 400 | — | ns |
| \overline{IRQ} interrupt pulse width low (edge-triggered) | t_{LIH} | 400 | — | ns |
| \overline{IRQ} interrupt pulse period | t_{LIL} | Note ⁽²⁾ | — | t_{cyc} |

1. $V_{DD} \geq 2.2$ V, $V_{SS} = 0$ Vdc; timing shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.

2. The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{cyc} .

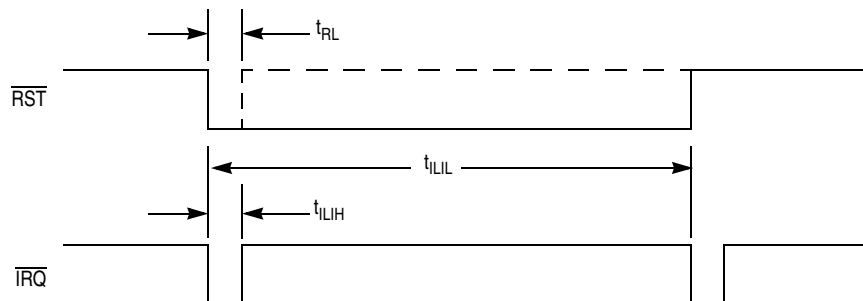


Figure 16-1. \overline{RST} and \overline{IRQ} Timing

16.7 Typical 3.0-V Output Drive Characteristics

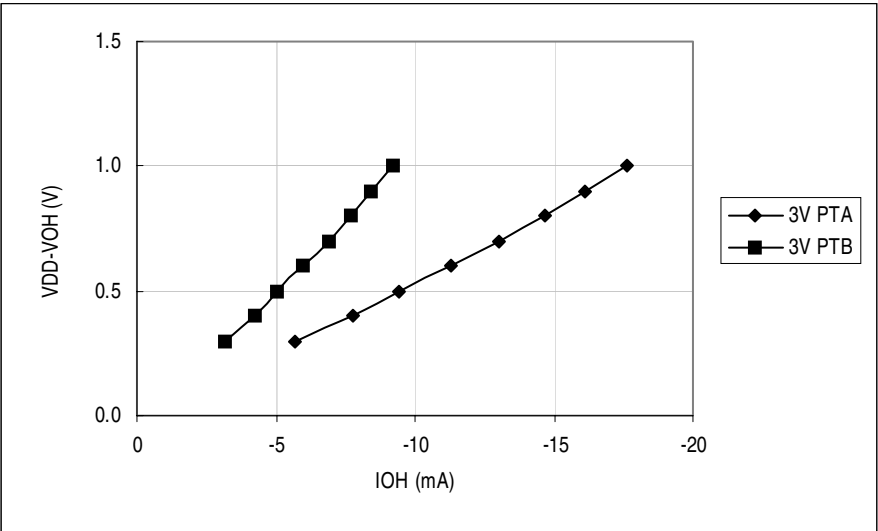


Figure 16-2. Typical 3-Volt Output High Voltage versus Output High Current (25°C)

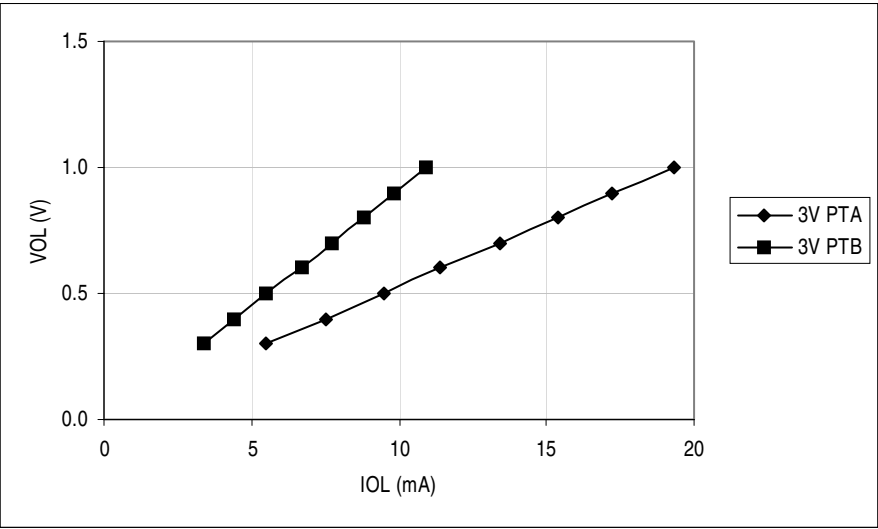


Figure 16-3. Typical 3-Volt Output Low Voltage versus Output Low Current (25°C)



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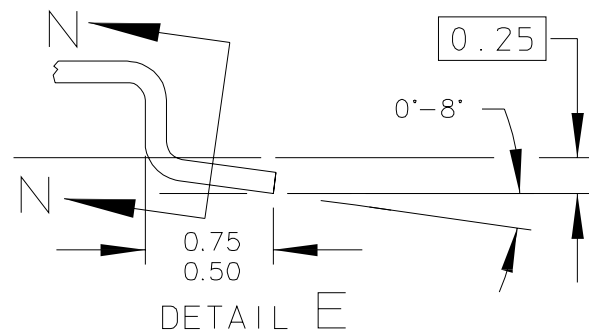
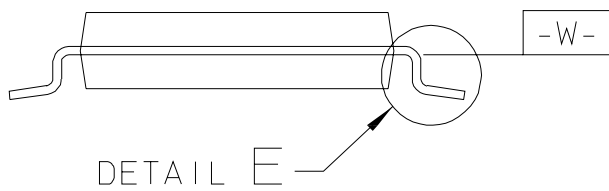
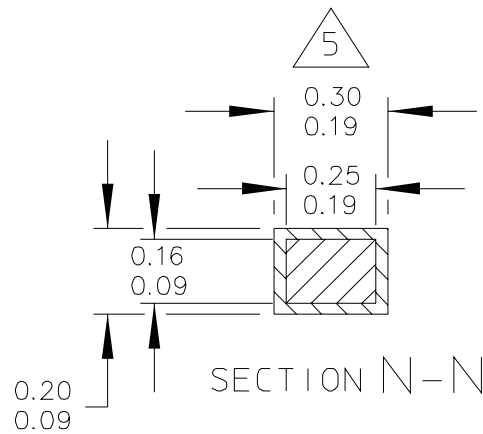
DO NOT SCALE THIS DRAWING

REV: T

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

| DIM | MILLIMETERS | | INCHES | | DIM | MILLIMETERS | | INCHES | |
|--------------------------|-------------|-------|-----------|-------|---------------------|-------------|---------------|--------|-----|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | 18.80 | 19.55 | 0.740 | 0.770 | | | | | |
| B | 6.35 | 6.85 | 0.250 | 0.270 | | | | | |
| C | 3.69 | 4.44 | 0.145 | 0.175 | | | | | |
| D | 0.39 | 0.53 | 0.015 | 0.021 | | | | | |
| F | 1.02 | 1.77 | 0.040 | 0.070 | | | | | |
| G | 2.54 BSC | | 0.100 BSC | | | | | | |
| H | 1.27 BSC | | 0.050 BSC | | | | | | |
| J | 0.21 | 0.38 | 0.008 | 0.015 | | | | | |
| K | 2.80 | 3.30 | 0.110 | 0.130 | | | | | |
| L | 7.50 | 7.74 | 0.295 | 0.305 | | | | | |
| M | 0° | 10° | 0° | 10° | | | | | |
| S | 0.51 | 1.01 | 0.020 | 0.040 | | | | | |
| TITLE: 16 LD PDIP | | | | | CASE NUMBER: 648-08 | | | | |
| | | | | | STANDARD: NON-JEDEC | | | | |
| | | | | | PACKAGE CODE: 0006 | | SHEET: 2 OF 4 | | |



TITLE:

16 LD TSSOP, PITCH 0.65MM

CASE NUMBER: 948F-01

STANDARD: JEDEC

PACKAGE CODE: 6117

SHEET: 2 OF 4