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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchlc908qy2pe

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Chapter 1 General Description

1.1 Introduction

The MC68HLC908QY4 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is a Complex Instruction Set Computer (CISC) with a Von Neumann architecture. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Device	FLASH Memory Size	Analog-to-Digital Converter	Pin Count
MC68HLC908QT1	1536 bytes	_	8 pins
MC68HLC908QT2	1536 bytes	4 ch, 8 bit	8 pins
MC68HLC908QT4	4096 bytes	4 ch, 8 bit	8 pins
MC68HLC908QY1	1536 bytes	—	16 pins
MC68HLC908QY2	1536 bytes	4 ch, 8 bit	16 pins
MC68HLC908QY4	4096 bytes	4 ch, 8 bit	16 pins

Table 1-1. Summary of Device Variations

1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- Operating voltage range of 2.2 V to 3.6 V
- 2-MHz internal bus operation
- Trimmable internal oscillator
 - 1.0 MHz internal bus operation
 - 8-bit trim capability allows 0.4% accuracy⁽¹⁾
 - ± 25% untrimmed
- Auto wakeup from STOP capability
- Configuration (CONFIG) register for MCU configuration options, including:
 - Low-voltage inhibit (LVI) trip point
- In-system FLASH programming
- FLASH security⁽²⁾

^{1.} The oscillator frequency is guaranteed to $\pm 5\%$ over temperature and voltage range after trimming.

No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.



MASS — Mass Erase Control Bit

This read/write bit configures the memory for mass erase operation.

- 1 = Mass Erase operation selected
 - 0 = Mass Erase operation unselected

ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation. ERASE is interlocked with the PGM bit such that both bits cannot be equal to 1 or set to 1 at the same time.

- 1 = Erase operation selected
- 0 = Erase operation unselected

PGM — Program Control Bit

This read/write bit configures the memory for program operation. PGM is interlocked with the ERASE bit such that both bits cannot be equal to 1 or set to 1 at the same time.

1 = Program operation selected

0 = Program operation unselected

2.6.2 FLASH Page Erase Operation

Use the following procedure to erase a page of FLASH memory. A page consists of 64 consecutive bytes starting from addresses \$XX00, \$XX40, \$XX80, or \$XXC0. The 48-byte user interrupt vectors area also forms a page. Any FLASH memory page can be erased alone.

- 1. Set the ERASE bit and clear the MASS bit in the FLASH control register.
- 2. Read the FLASH block protect register.
- 3. Write any data to any FLASH location within the address range of the block to be erased.
- 4. Wait for a time, t_{NVS} (minimum 10 μ s).
- 5. Set the HVEN bit.
- 6. Wait for a time, t_{Erase} (minimum 1 ms or 4 ms).
- 7. Clear the ERASE bit.
- 8. Wait for a time, t_{NVH} (minimum 5 μ s).
- 9. Clear the HVEN bit.
- 10. After time, t_{BCV} (typical 1 µs), the memory can be accessed in read mode again.

NOTE

Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.

CAUTION

A page erase of the vector page will erase the internal oscillator trim value at \$FFC0.

In applications that require more than 1000 program/erase cycles, use the 4 ms page erase specification to get improved long-term reliability. Any application can use this 4 ms page erase specification. However, in applications where a FLASH location will be erased and reprogrammed less than 1000 times, and speed is important, use the 1 ms page erase specification to get a shorter cycle time.



Memory

2.6.3 FLASH Mass Erase Operation

Use the following procedure to erase the entire FLASH memory to read as a 1:

- 1. Set both the ERASE bit and the MASS bit in the FLASH control register.
- 2. Read the FLASH block protect register.
- 3. Write any data to any FLASH address⁽¹⁾ within the FLASH memory address range.
- 4. Wait for a time, t_{NVS} (minimum 10 μ s).
- 5. Set the HVEN bit.
- 6. Wait for a time, t_{MErase} (minimum 4 ms).
- 7. Clear the ERASE and MASS bits.

NOTE

Mass erase is disabled whenever any block is protected (FLBPR does not equal \$FF).

- 8. Wait for a time, t_{NVH} (minimum 100 μ s).
- 9. Clear the HVEN bit.
- 10. After time, t_{RCV} (typical 1 µs), the memory can be accessed in read mode again.

NOTE

Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.

CAUTION

A mass erase will erase the internal oscillator trim value at \$FFC0.

2.6.4 FLASH Program Operation

Programming of the FLASH memory is done on a row basis. A row consists of 32 consecutive bytes starting from addresses \$XX00, \$XX20, \$XX40, \$XX60, \$XX80, \$XXA0, \$XXC0, or \$XXE0. Use the following step-by-step procedure to program a row of FLASH memory

Figure 2-4 shows a flowchart of the programming algorithm.

NOTE

Only bytes which are currently \$FF may be programmed.

- 1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
- 2. Read the FLASH block protect register.
- 3. Write any data to any FLASH location within the address range desired.
- 4. Wait for a time, t_{NVS} (minimum 10 μ s).
- 5. Set the HVEN bit.
- 6. Wait for a time, t_{PGS} (minimum 5 μ s).
- 7. Write data to the FLASH address being $programmed^{(2)}$.

^{1.} When in monitor mode, with security sequence failed (see 15.3.2 Security), write to the FLASH block protect register instead of any FLASH address.

^{2.} The time between each FLASH address change, or the time between the last FLASH address programmed to clearing PGM bit, must not exceed the maximum programming time, t_{PROG} maximum.



Central Processor Unit (CPU)



Figure 7-1. CPU Registers

7.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.



Figure 7-2. Accumulator (A)

7.3.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.



Figure 7-3. Index Register (H:X)





|--|

Source	Operation	Description		Effect on CCR						ess e	ode	and	es	
Form	Operation	Description		Ī	v	н	I	N	z	С	Addi Mod	Opce	Ореі	Cycl
SWI	Software Interrupt	n (PCL sh (PCH sh (X) sh (A) i (CCR ← 1 High E Low B)) Byte	_	_	1	_	_	_	INH	83		9	
TAP	Transfer A to CCR	$CCR \gets (A)$			1	\$	1	1	1	\$	INH	84		2
TAX	Transfer A to X	$X \gets (A)$			-	-	-	- ·	_	Ι	INH	97		1
TPA	Transfer CCR to A	$A \gets (CCR)$			-	-	-		_	Ι	INH	85		1
TST opr TSTA TSTX TST opr,X TST ,X TST opr,SP	Test for Negative or Zero	- (M) –	\$00	0	-	_	t	ţ	_	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4	
TSX	Transfer SP to H:X	$H:X \gets (SP) +$	1		-	-	-		-	١	INH	95		2
TXA	Transfer X to A	$A \gets (X)$		-	-	-		_	Ι	INH	9F		1	
TXS	Transfer H:X to SP	$(SP) \gets (H{:}X) -$		-	-	-	- ·	_	Ι	INH	94		2	
WAIT	Enable Interrupts; Wait for Interrupt	I bit ← 0; Inhibit CPU until interrupte	clockin d	ıg	-	-	0	-	-	-	INH	8F		1
A Accumu C Carry/bo CCR Conditio dd Direct a DD Direct a DD Direct to DIR Direct a DIX+ Direct a DIX+ Direct to ee ff High an EXT Extende ff Offset b H Half-car H Index re hh II High an I Interrup ii Immedia IMD Immedia IMD Immedia IMH Inheren IX Indexed IX+ Indexed IX+ Indexed IX+ Indexed IX1 Indexed IX1 Indexed IX2 Indexed IX3 Indexed IX2 Indexed IX3 Indexed IX2 Indexed IX3 Indexed IX2 Indexed IX3 Indexed IX3 Indexed IX3 Indexed IX4 Indexed IX4 Indexed IX4 Indexed IX4 Indexed IX4 Indexed IX1 Indexed IX2 Indexed IX2 Indexed IX3 Indexed IX3 Indexed IX3 Indexed IX3 Indexed IX4	n opc PCH PCLL REI rr SSP U ∨ X Z & \oplus () () # « \leftarrow ? : ‡	Any bit Operar Progra Progra Relativ Relativ Relativ Stack p Stack p Undefii Overfic Index r Zero bi Logical Logical Conter Negatid Immed Sign ep Loadec If Concat Set or o Not affi	nd (m c a p poir poir poir poir poir poir poir poir	(on- could a could a c	e or nter nter ress gram r, 8-I r 16- r lov LUS o's c alue d wi d	two hig low ing co co bit co bit V by	o b gh v b mount off off /te	oyte byt odd iter iter set fset OR em	es) e offset byt offset byt addressir t addressi	e eg mode ng mod	e le			

7.8 Opcode Map

See Table 7-2.

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Central Processor Unit (CPU)

Table 7-2, Opcode Map

	Bit Mani	oulation	Branch	i		Read-Mo	dify-Write		_	Cor	trol	i			Register	/Memory			
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
MSB LSB	0	1	2	3	4	5	6	9E6	7	8	9	Α	в	с	D	9ED	Е	9EE	F
0	5 BRSET0 3 DIR	4 BSET0 2 DIR	3 BRA 2 REL	4 NEG 2 DIR	1 NEGA 1 INH	1 NEGX 1 INH	A NEG 2 IX1	5 NEG 3 SP1	3 NEG 1 IX	7 RTI 1 INH	3 BGE 2 REL	2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	4 SUB 3 IX2	5 SUB 4 SP2	3 SUB 2 IX1	4 SUB 3 SP1	2 SUB 1 IX
1	5 BRCLR0 3 DIR	4 BCLR0 2 DIR	3 BRN 2 REL	5 CBEQ 3 DIR	4 CBEQA 3 IMM	4 CBEQX 3 IMM	5 CBEQ 3 IX1+	6 CBEQ 4 SP1	4 CBEQ 2 IX+	4 RTS 1 INH	3 BLT 2 REL	2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	4 CMP 3 IX2	5 CMP 4 SP2	3 CMP 2 IX1	4 CMP 3 SP1	2 CMP 1 IX
2	5 BRSET1 3 DIR	4 BSET1 2 DIR	3 BHI 2 REL		5 MUL 1 INH	7 DIV 1 INH	3 NSA 1 INH		2 DAA 1 INH		3 BGT 2 REL	SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	4 SBC 3 IX2	5 SBC 4 SP2	3 SBC 2 IX1	4 SBC 3 SP1	2 SBC 1 IX
3	5 BRCLR1 3 DIR	4 BCLR1 2 DIR	3 BLS 2 REL	4 COM 2 DIR	1 COMA 1 INH	1 COMX 1 INH	4 COM 2 IX1	5 COM 3 SP1	3 COM 1 IX	9 SWI 1 INH	3 BLE 2 REL	CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	4 CPX 3 IX2	5 CPX 4 SP2	3 CPX 2 IX1	4 CPX 3 SP1	2 CPX 1 IX
4	5 BRSET2 3 DIR	4 BSET2 2 DIR	3 BCC 2 REL	4 LSR 2 DIR	1 LSRA 1 INH	1 LSRX 1 INH	4 LSR 2 IX1	5 LSR 3 SP1	3 LSR 1 IX	2 TAP 1 INH	2 TXS 1 INH	2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	4 AND 3 IX2	5 AND 4 SP2	3 AND 2 IX1	4 AND 3 SP1	2 AND 1 IX
5	5 BRCLR2 3 DIR	4 BCLR2 2 DIR	3 BCS 2 REL	4 STHX 2 DIR	3 LDHX 3 IMM	4 LDHX 2 DIR	3 CPHX 3 IMM		4 CPHX 2 DIR	1 TPA 1 INH	2 TSX 1 INH	BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	4 BIT 3 IX2	5 BIT 4 SP2	3 BIT 2 IX1	4 BIT 3 SP1	2 BIT 1 IX
6	5 BRSET3 3 DIR	4 BSET3 2 DIR	3 BNE 2 REL	4 ROR 2 DIR	1 RORA 1 INH	1 RORX 1 INH	4 ROR 2 IX1	5 ROR 3 SP1	3 ROR 1 IX	2 PULA 1 INH		2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	4 LDA 3 IX2	5 LDA 4 SP2	3 LDA 2 IX1	4 LDA 3 SP1	2 LDA 1 IX
7	5 BRCLR3 3 DIR	4 BCLR3 2 DIR	3 BEQ 2 REL	4 ASR 2 DIR	1 ASRA 1 INH	1 ASRX 1 INH	4 ASR 2 IX1	5 ASR 3 SP1	3 ASR 1 IX	2 PSHA 1 INH	1 TAX 1 INH	AIS 2 IMM	3 STA 2 DIR	4 STA 3 EXT	4 STA 3 IX2	STA 4 SP2	3 STA 2 IX1	4 STA 3 SP1	2 STA 1 IX
8	5 BRSET4 3 DIR	4 BSET4 2 DIR	3 BHCC 2 REL	4 LSL 2 DIR	1 LSLA 1 INH	1 LSLX 1 INH	4 LSL 2 IX1	5 LSL 3 SP1	3 LSL 1 IX	2 PULX 1 INH	1 CLC 1 INH	EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	4 EOR 3 IX2	5 EOR 4 SP2	3 EOR 2 IX1	4 EOR 3 SP1	2 EOR 1 IX
9	5 BRCLR4 3 DIR	4 BCLR4 2 DIR	3 BHCS 2 REL	4 ROL 2 DIR	1 ROLA 1 INH	1 ROLX 1 INH	4 ROL 2 IX1	5 ROL 3 SP1	3 ROL 1 IX	2 PSHX 1 INH	1 SEC 1 INH	ADC 2 IMM	3 ADC 2 DIR	ADC 3 EXT	4 ADC 3 IX2	ADC 4 SP2	3 ADC 2 IX1	4 ADC 3 SP1	2 ADC 1 IX
Α	5 BRSET5 3 DIR	4 BSET5 2 DIR	3 BPL 2 REL	4 DEC 2 DIR	1 DECA 1 INH	1 DECX 1 INH	4 DEC 2 IX1	5 DEC 3 SP1	3 DEC 1 IX	2 PULH 1 INH	2 CLI 1 INH	ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	4 ORA 3 IX2	5 ORA 4 SP2	3 ORA 2 IX1	4 ORA 3 SP1	2 ORA 1 IX
в	5 BRCLR5 3 DIR	4 BCLR5 2 DIR	3 BMI 2 REL	5 DBNZ 3 DIR	3 DBNZA 2 INH	3 DBNZX 2 INH	5 DBNZ 3 IX1	6 DBNZ 4 SP1	4 DBNZ 2 IX	2 PSHH 1 INH	2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	4 ADD 3 IX2	5 ADD 4 SP2	3 ADD 2 IX1	4 ADD 3 SP1	2 ADD 1 IX
с	5 BRSET6 3 DIR	4 BSET6 2 DIR	3 BMC 2 REL	4 INC 2 DIR	1 INCA 1 INH	1 INCX 1 INH	4 INC 2 IX1	5 INC 3 SP1	3 INC 1 IX	1 CLRH 1 INH	1 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2		3 JMP 2 IX1		2 JMP 1 IX
D	5 BRCLR6 3 DIR	4 BCLR6 2 DIR	3 BMS 2 REL	3 TST 2 DIR	1 TSTA 1 INH	1 TSTX 1 INH	3 TST 2 IX1	4 TST 3 SP1	2 TST 1 IX		1 NOP 1 INH	4 BSR 2 REL	4 JSR 2 DIR	5 JSR 3 EXT	6 JSR 3 IX2		5 JSR 2 IX1		4 JSR 1 IX
E	5 BRSET7 3 DIR	4 BSET7 2 DIR	3 BIL 2 REL		5 MOV 3 DD	4 MOV 2 DIX+	4 MOV 3 IMD		4 MOV 2 IX+D	1 STOP 1 INH	*	2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	4 LDX 3 IX2	5 LDX 4 SP2	3 LDX 2 IX1	4 LDX 3 SP1	2 LDX 1 IX
F	5 BRCLR7 3 DIR	4 BCLR7 2 DIR	3 BIH 2 REL	3 CLR 2 DIR	1 CLRA 1 INH	1 CLRX 1 INH	3 CLR 2 IX1	4 CLR 3 SP1	CLR 1 IX	1 WAIT 1 INH	1 TXA 1 INH	AIX 2 IMM	3 STX 2 DIR	STX 3 EXT	4 STX 3 IX2	5 STX 4 SP2	3 STX 2 IX1	4 STX 3 SP1	2 STX 1 IX

MC68HLC908QY/QT Family Data Sheet, Rev. 3

REL Relative IX Indexed, No Offset

- Indexed, 8-Bit Offset Indexed, 16-Bit Offset IX1 IX2
- DIR Direct EXT Extended
- DD Direct-Direct IMD Immediate-Direct IX+D Indexed-Direct DIX+ Direct-Indexed
- SP1 Stack Pointer, 8-Bit Offset SP2 Stack Pointer, 16-Bit Offset IX+ Indexed, No Offset with
 - Post Increment
- IX1+ Indexed, 1-Byte Offset with Post Increment

Low Byte of Opcode in Hexadecimal

0 High Byte of Opcode in Hexadecimal

MSB

LSB

0

5 Cycles BRSET0 Opcode Mnemonic 3 DIR Number of Bytes / Addressing Mode

*Pre-byte for stack pointer indexed instructions

INH Inherent IMM Immediate



Functional Description



Figure 8-2. IRQ Module Block Diagram

8.3.1 MODE = 1

If the MODE bit is set, the IRQ pin is both falling edge sensitive and low level sensitive. With MODE set, both of the following actions must occur to clear the IRQ interrupt request:

- Return of the IRQ pin to a high level. As long as the IRQ pin is low, the IRQ request remains active.
- IRQ vector fetch or software clear. An IRQ vector fetch generates an interrupt acknowledge signal to clear the IRQ latch. Software generates the interrupt acknowledge signal by writing a 1 to ACK in INTSCR. The ACK bit is useful in applications that poll the IRQ pin and require software to clear the IRQ latch. Writing to ACK prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACK does not affect subsequent transitions on the IRQ pin. A falling edge that occurs after writing to ACK latches another interrupt request. If the IRQ mask bit, IMASK, is clear, the CPU loads the program counter with the IRQ vector address.

The IRQ vector fetch or software clear and the return of the \overline{IRQ} pin to a high level may occur in any order. The interrupt request remains pending as long as the \overline{IRQ} pin is low. A reset will clear the IRQ latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

Use the BIH or BIL instruction to read the logic level on the IRQ pin.

8.3.2 MODE = 0

If the MODE bit is clear, the IRQ pin is falling edge sensitive only. With MODE clear, an IRQ vector fetch or software clear immediately clears the IRQ latch.

The IRQF bit in INTSCR can be read to check for pending interrupts. The IRQF bit is not affected by IMASK, which makes it useful in applications where polling is preferred.

NOTE

When using the level-sensitive interrupt trigger, avoid false IRQ interrupts by masking interrupt requests in the interrupt routine.

MC68HLC908QY/QT Family Data Sheet, Rev. 3

Keyboard Interrupt Module (KBI)



RST, IRQ: Pins have internal (about 30K Ohms) pull up PTA[0:5]: High current sink and source capability

PTA[0:5]: Pins have programmable keyboard interrupt and pull up

PTB[0:7]: Not available on 8-pin devices – MC68HLC908QT1, MC68HLC908QT2, and MC68HLC908QT4 (see note in 12.1 Introduction)

ADC: Not available on the MC68HLC908QY1 and MC68HC9L08QT1

Figure 9-1. Block Diagram Highlighting KBI Block and Pins



System Integration Module (SIM)

state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

13.6.5 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a two-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

13.7 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described below. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

13.7.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. Figure 13-14 shows the timing for wait mode entry.

ADDRESS BUS	WAIT ADDR		DR + 1	SAME	X	SAME	X
DATA BUS	PREVIOUS	S DATA		CODE	SAME		SAME
R/W							

NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 13-14. Wait Mode Entry Timing

A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

Wait mode can also be exited by a reset (or break in emulation mode). A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the break status register (BSR). If the COP disable bit, COPD, in the configuration register is 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.



System Integration Module (SIM)

13.8.2 Break Flag Control Register

The break control register (BFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.



Figure 13-20. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break



Timer Interface Module (TIM)

14.4.4.1 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in 14.4.4 Pulse Width Modulation (PWM). The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIM overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the PWM pulse width on channel x:

- When changing to a shorter pulse width, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current pulse. The interrupt routine has until the end of the PWM period to write the new value.
- When changing to a longer pulse width, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current PWM period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same PWM period.

NOTE

In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare also can cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.

14.4.4.2 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The TIM channel 0 registers initially control the pulse width on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIM channel registers (0 or 1) that control the pulse width are the ones written to last. TSC0 controls and monitors the buffered PWM function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

NOTE

In buffered PWM signal generation, do not write new pulse width values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered PWM signals.





14.9.1 TIM Status and Control Register

The TIM status and control register (TSC) does the following:

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock



Figure 14-4. TIM Status and Control Register (TSC)

TOF — TIM Overflow Flag Bit

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

- 1 = TIM counter has reached modulo value
- 0 = TIM counter has not reached modulo value

TOIE — **TIM** Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled

0 = TIM overflow interrupts disabled

TSTOP — TIM Stop Bit

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped

0 = TIM counter active

NOTE

Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode. When the TSTOP bit is set and the timer is configured for input capture operation, input captures are inhibited until the TSTOP bit is cleared.

When using TSTOP to stop the timer counter, see if any timer flags are set. If a timer flag is set, it must be cleared by clearing TSTOP, then clearing the flag, then setting TSTOP again.



Timer Interface Module (TIM)

TRST — TIM Reset Bit

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from \$0000. TRST is cleared automatically after the TIM counter is reset and always reads as a 0. Reset clears the TRST bit.

1 = Prescaler and TIM counter cleared

0 = No effect

NOTE

Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of \$0000.

PS[2:0] — Prescaler Select Bits

These read/write bits select either the PTA2/TCLK pin or one of the seven prescaler outputs as the input to the TIM counter as Table 14-2 shows. Reset clears the PS[2:0] bits.

PS2	PS1	PS0	TIM Clock Source	
0	0	0	Internal bus clock ÷ 1	
0	0	1	Internal bus clock ÷ 2	
0	1	0	Internal bus clock ÷ 4	
0	1	1	Internal bus clock ÷ 8	
1	0	0	Internal bus clock ÷ 16	
1	0	1	Internal bus clock ÷ 32	
1	1 0		Internal bus clock ÷ 64	
1	1	1	PTA2/TCLK	

Table 14-2.	Prescaler	Selection
-------------	-----------	-----------

14.9.2 TIM Counter Registers

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

NOTE

If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.











The MCU executes the SWI and PSHH instructions when it enters monitor mode. The RUN command tells the MCU to execute the PULH and RTI instructions. Before sending the RUN command, the host can modify the stacked CPU registers to prepare to run the host program. The READSP command returns the incremented stack pointer value, SP + 1. The high and low bytes of the program counter are at addresses SP + 5 and SP + 6.

	SP
HIGH BYTE OF INDEX REGISTER	SP + 1
CONDITION CODE REGISTER	SP + 2
ACCUMULATOR	SP + 3
LOW BYTE OF INDEX REGISTER	SP + 4
HIGH BYTE OF PROGRAM COUNTER	SP + 5
LOW BYTE OF PROGRAM COUNTER	SP + 6
	SP + 7

Figure 15-17. Stack Pointer at Monitor Mode Entry

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16.9 Supply Current Characteristics

Characteristic	Voltage	Bus Freq. (MHz)	Symbol	Тур	Мах	Unit
Run mode V _{DD} supply current ⁽¹⁾	3.0 2.2	1 1	RI _{DD}	1.5 1.0	2.5 1.5	mA
WAIT mode V _{DD} supply current ⁽²⁾	3.0 2.2	1 1	WI _{DD}	1.2 1.0	2.0 1.0	mA
Stop mode V _{DD} supply current ⁽³⁾ 25°C 0 to 70°C -40 to 85°C 25°C with auto wake-up enabled Incremental current with LVI enabled at 25°C	3.0		Slaa	0.006 0.08 0.12 5.70 110	 2.0 	μΑ
25°C 0 to 70°C -40 to 85°C 25°C with auto wake-up enabled Incremental current with LVI enabled at 25°C	2.2			0.005 0.08 0.12 1.30 100	 .0 	μΑ

1. Run (operating) I_{DD} measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Measured with all modules except ADC enabled.

 Wait (operating) I_{DD} measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Measured with all modules except ADC enabled.

3. Stop I_{DD} measured with all ports driven 0.2 V or less from rail. No dc loads. On the 8-pin versions, port B is configured as inputs with pullups enabled.



Figure 16-5. Typical Run Current versus V_{DD} (25°C) (f_{Bus} = 1 MHz for Internal Oscillator, f_{Bus} = 8 kHz for Crystal Oscillator)

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16.10 Analog-to-Digital (ADC) Converter Characteristics

16.10.1 ADC Electrical Operating Conditions

The ADC accuracy characteristics below are guaranteed over two operating conditions as stated here.

	Characteristic	Symbol	Min	Max	Unit
Condition A	ATD supply	V _{DD}	2.7	3.6	V
	ADC internal clock	f _{ADIC}	0.008	1	MHz
	Ambient temperature	T _A	Τ _L	т _н	°C
Condition B	ATD supply	V _{DD}	2.3	2.7	V
	ADC internal clock	f _{ADIC}	8	63	kHz
	Ambient temperature	T _A	0	т _н	°C

16.10.2 ADC Performance Characteristics

Characteristic		Symbol	Min	Max	Unit	Comments	
Input voltages		V _{ADIN}	V_{SS}	V _{DD}	V	—	
Resolution (1 LSB)	Condition A Condition B	RES	10.5 8.99	14.1 10.5	mV	_	
Absolute accuracy (Total unadjusted error)	Condition A Condition B	E _{TUE}		± 1.5 ± 2.0	LSB	Includes quantization	
Conversion range		V _{AIN}	V_{SS}	V_{DD}	V	_	
Power-up time		t _{ADPU}	16	—	t _{ADIC} cycles	$t_{ADIC} = 1/f_{ADIC}$	
Conversion time		t _{ADC}	16	17	t _{ADIC} cycles	$t_{ADIC} = 1/f_{ADIC}$	
Sample time ⁽¹⁾		t _{ADS}	5	—	t _{ADIC} cycles	$t_{ADIC} = 1/f_{ADIC}$	
Zero input reading ⁽²⁾		Z _{ADI}	00	01	Hex	$V_{IN} = V_{SS}$	
Full-scale reading ⁽³⁾		F _{ADI}	FE	FF	Hex	$V_{IN} = V_{DD}$	
Input capacitance		C _{ADI}	_	8	pF	Not tested	
Input leakage ⁽³⁾		١ _{١L}	—	± 1	μA	_	
ADC supply current (V _{DD} = 3 V)		I _{ADAD}	Typical	= 0.45	mA	Enabled	

1. Source impedances greater than 10 k Ω adversely affect internal RC charging time during input sampling.

2. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.

3. The external system error caused by input leakage current is approximately equal to the product of R source and input current.

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NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
- A DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
- 5. ROUNDED CORNERS OPTIONAL.
- 6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

	MILLIN	ETERS	INC	HES		MILLIMETERS		11	NCHES
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
А	18.80	19.55	0.740	0.770					
В	6.35	6.85	0.250	0.270					
С	3.69	4.44	0.145	0.175					
D	0.39	0.53	0.015	0.021					
F	1.02	1.77	0.040	0.070					
G	2.54	BSC	0.100	BSC					
Н	1.27	BSC	0.050) BSC					
J	0.21	0.38	0.008	0.015					
K	2.80	3.30	0.110	0.130					
L	7.50	7.74	0.295	0.305					
М	0.	10°	0.	10°					
S	0.51	1.01	0.020	0.040					
TITLE:			CASE NUMBER: 648–08						
16 LD PDIP					STANDARD: NON-JEDEC				
	PACKAGE CODE: 0006 SHEET: 2 OF 4						2 OF 4		

