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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	5
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcl908qt1cdwe

List of Chapters

- Chapter 1 General Description.15
- Chapter 2 Memory.23
- Chapter 3 Analog-to-Digital Converter (ADC).39
- Chapter 4 Auto Wakeup Module (AWU)47
- Chapter 5 Configuration Register (CONFIG)53
- Chapter 6 Computer Operating Properly (COP).57
- Chapter 7 Central Processor Unit (CPU).61
- Chapter 8 External Interrupt (IRQ).73
- Chapter 9 Keyboard Interrupt Module (KBI).79
- Chapter 10 Low-Voltage Inhibit (LVI).85
- Chapter 11 Oscillator Module (OSC)89
- Chapter 12 Input/Output Ports (PORTS).97
- Chapter 13 System Integration Module (SIM).103
- Chapter 14 Timer Interface Module (TIM)119
- Chapter 15 Development Support135
- Chapter 16 Electrical Specifications151
- Chapter 17 Ordering Information and Mechanical Specifications163

Table of Contents

Chapter 1 General Description

1.1	Introduction	15
1.2	Features	15
1.3	MCU Block Diagram	17
1.4	Pin Assignments	17
1.5	Pin Functions	20
1.6	Pin Function Priority	21

Chapter 2 Memory

2.1	Introduction	23
2.2	Unimplemented Memory Locations	23
2.3	Reserved Memory Locations	23
2.4	Input/Output (I/O) Section	25
2.5	Random-Access Memory (RAM)	31
2.6	FLASH Memory (FLASH)	32
2.6.1	FLASH Control Register	32
2.6.2	FLASH Page Erase Operation	33
2.6.3	FLASH Mass Erase Operation	34
2.6.4	FLASH Program Operation	34
2.6.5	FLASH Protection	35
2.6.6	FLASH Block Protect Register	37
2.6.7	Wait Mode	38
2.6.8	Stop Mode	38

Chapter 3 Analog-to-Digital Converter (ADC)

3.1	Introduction	39
3.2	Features	39
3.3	Functional Description	39
3.3.1	ADC Port I/O Pins	39
3.3.2	Voltage Conversion	41
3.3.3	Conversion Time	42
3.3.4	Continuous Conversion	42
3.3.5	Accuracy and Precision	42
3.4	Interrupts	42
3.5	Low-Power Modes	42
3.5.1	Wait Mode	42
3.5.2	Stop Mode	42

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8×8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

[Figure 1-1](#) shows the structure of the MC68HLC908QY4.

1.4 Pin Assignments

The MC68HLC908QT4, MC68HLC908QT2, and MC68HLC908QT1 are available in 8-pin packages and the MC68HLC908QY4, MC68HLC908QY2, and MC68HLC908QY1 in 16-pin packages. [Figure 1-2](#) shows the pin assignment for these packages.

CH[4:0] — ADC Channel Select Bits

CH4, CH3, CH2, CH1, and CH0 form a 5-bit field which is used to select one of the four ADC channels. The five select bits are detailed in [Table 3-1](#). Care should be taken when using a port pin as both an analog and a digital input simultaneously to prevent switching noise from corrupting the analog signal. The ADC subsystem is turned off when the channel select bits are all set to 1. This feature allows for reduced power consumption for the MCU when the ADC is not used. Reset sets all of these bits to a 1.

NOTE

Recovery from the disabled state requires one conversion cycle to stabilize.

Table 3-1. MUX Channel Select

CH4	CH3	CH2	CH1	CH0	ADC Channel	Input Select
0	0	0	0	0	AD0	PTA0
0	0	0	0	1	AD1	PTA1
0	0	0	1	0	AD2	PTA4
0	0	0	1	1	AD3	PTA5
0	0	1	0	0	—	Unused ⁽¹⁾
↓	↓	↓	↓	↓	—	
1	1	0	1	0	—	
1	1	0	1	1	—	Reserved
1	1	1	0	0	—	Unused
1	1	1	0	1	—	V _{DDA} ⁽²⁾
1	1	1	1	0	—	V _{SSA} ⁽²⁾
1	1	1	1	1	—	ADC power off

1. If any unused channels are selected, the resulting ADC conversion will be unknown.
2. The voltage levels supplied from internal reference nodes, as specified in the table, are used to verify the operation of the ADC converter both in production test and for user applications.

3.7.2 ADC Data Register

One 8-bit result register is provided. This register is updated each time an ADC conversion completes.

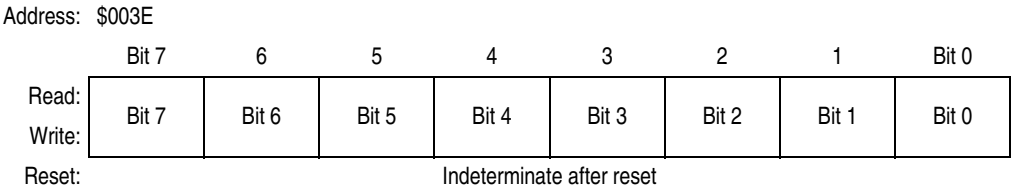


Figure 3-4. ADC Data Register (ADR)



4.6.2 Keyboard Status and Control Register

The keyboard status and control register (KBSCR):

- Flags keyboard/auto wakeup interrupt requests
- Acknowledges keyboard/auto wakeup interrupt requests
- Masks keyboard/auto wakeup interrupt requests

Address: \$001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:						ACKK		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-3. Keyboard Status and Control Register (KBSCR)

Bits 7–4 — Not used

These read-only bits always read as 0s.

KEYF — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending on port A or auto wakeup. Reset clears the KEYF bit.

- 1 = Keyboard/auto wakeup interrupt pending
- 0 = No keyboard/auto wakeup interrupt pending

ACKK — Keyboard Acknowledge Bit

Writing a 1 to this write-only bit clears the keyboard/auto wakeup interrupt request on port A and auto wakeup logic. ACKK always reads as 0. Reset clears ACKK.

IMASKK— Keyboard Interrupt Mask Bit

Writing a 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests on port A or auto wakeup. Reset clears the IMASKK bit.

- 1 = Keyboard/auto wakeup interrupt requests masked
- 0 = Keyboard/auto wakeup interrupt requests not masked

NOTE

MODEK is not used in conjunction with the auto wakeup feature. To see a description of this bit, see [9.7.1 Keyboard Status and Control Register](#).

Central Processor Unit (CPU)

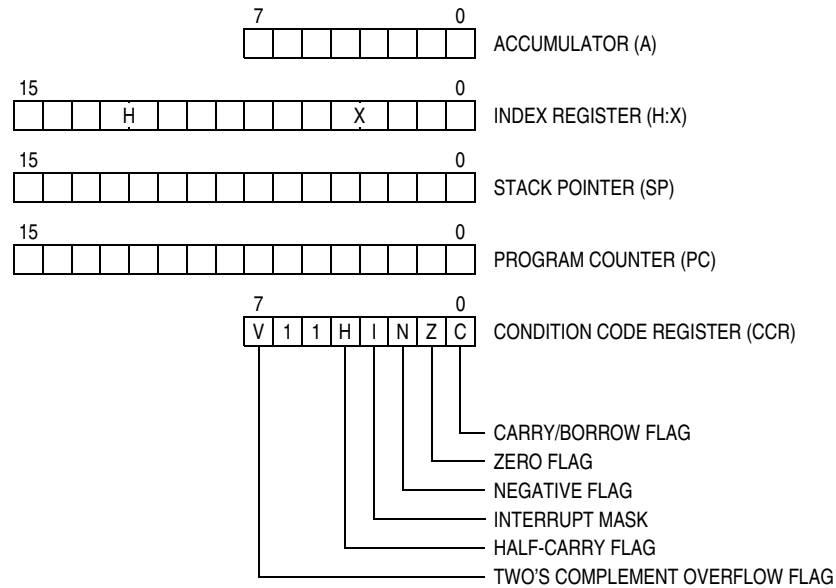


Figure 7-1. CPU Registers

7.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

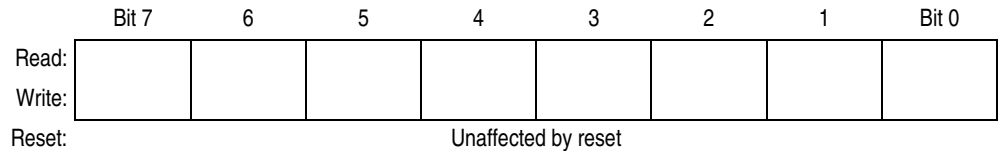


Figure 7-2. Accumulator (A)

7.3.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.

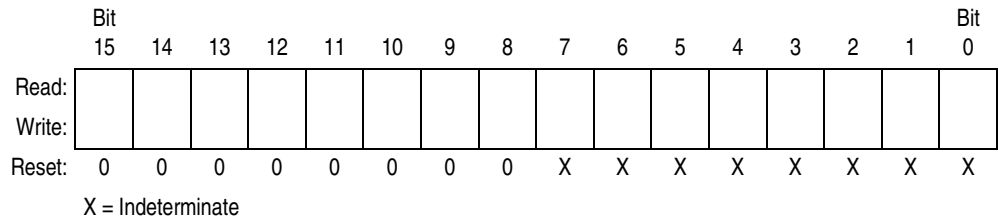


Figure 7-3. Index Register (H:X)

Table 7-2. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write						Control		Register/Memory							
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
MSB LSB	0	1	2	3	4	5	6	9E6	7	8	9	A	B	C	D	9ED	E	9EE	F
0	BRSET0 3 DIR	BSET0 2 DIR	BRA 2 REL	NEG 2 DIR	NEGA 1 INH	NEGX 1 INH	NEG 2 IX1	NEG 3 SP1	NEG 1 IX	RTI 1 INH	BGE 2 REL	SUB 2 IMM	SUB 2 DIR	SUB 3 EXT	SUB 3 IX2	SUB 4 SP2	SUB 2 IX1	SUB 3 SP1	SUB 1 IX
1	BRCLR0 3 DIR	BCLR0 2 DIR	BRN 2 REL	CBEQ 3 DIR	CBEQA 3 IMM	CBEQX 3 IMM	CBEQ 3 IX1+	CBEQ 4 SP1	CBEQ 2 IX+	RTS 1 INH	BLT 2 REL	CMP 2 IMM	CMP 2 DIR	CMP 3 EXT	CMP 3 IX2	CMP 4 SP2	CMP 2 IX1	CMP 3 SP1	CMP 1 IX
2	BRSET1 3 DIR	BSET1 2 DIR	BHI 2 REL		MUL 1 INH	DIV 1 INH	NSA 1 INH		DAA 1 INH		BGT 2 REL	SBC 2 IMM	SBC 2 DIR	SBC 3 EXT	SBC 3 IX2	SBC 4 SP2	SBC 2 IX1	SBC 3 SP1	SBC 1 IX
3	BRCLR1 3 DIR	BCLR1 2 DIR	BLS 2 REL	COM 2 DIR	COMA 1 INH	COMX 1 INH	COM 2 IX1	COM 3 SP1	COM 1 IX	SWI 1 INH	BLE 2 REL	CPX 2 IMM	CPX 2 DIR	CPX 3 EXT	CPX 3 IX2	CPX 4 SP2	CPX 2 IX1	CPX 3 SP1	CPX 1 IX
4	BRSET2 3 DIR	BSET2 2 DIR	BCC 2 REL	LSR 2 DIR	LSRA 1 INH	LSRX 1 INH	LSR 2 IX1	LSR 3 SP1	LSR 1 IX	TAP 1 INH	TXS 1 INH	AND 2 IMM	AND 2 DIR	AND 3 EXT	AND 3 IX2	AND 4 SP2	AND 2 IX1	AND 3 SP1	AND 1 IX
5	BRCLR2 3 DIR	BCLR2 2 DIR	BCS 2 REL	STHX 2 DIR	LDHX 3 IMM	LDHX 2 DIR	CPHX 3 IMM		CPHX 2 DIR	TPA 1 INH	TSX 1 INH	BIT 2 IMM	BIT 2 DIR	BIT 3 EXT	BIT 3 IX2	BIT 4 SP2	BIT 2 IX1	BIT 3 SP1	BIT 1 IX
6	BRSET3 3 DIR	BSET3 2 DIR	BNE 2 REL	ROR 2 DIR	RORA 1 INH	RORX 1 INH	ROR 2 IX1	ROR 3 SP1	ROR 1 IX	PULA 1 INH		LDA 2 IMM	LDA 2 DIR	LDA 3 EXT	LDA 3 IX2	LDA 4 SP2	LDA 2 IX1	LDA 3 SP1	LDA 1 IX
7	BRCLR3 3 DIR	BCLR3 2 DIR	BEQ 2 REL	ASR 2 DIR	ASRA 1 INH	ASRX 1 INH	ASR 2 IX1	ASR 3 SP1	ASR 1 IX	PSHA 1 INH	TAX 1 INH	AIS 2 IMM	STA 2 DIR	STA 3 EXT	STA 3 IX2	STA 4 SP2	STA 2 IX1	STA 3 SP1	STA 1 IX
8	BRSET4 3 DIR	BSET4 2 DIR	BHCC 2 REL	LSL 2 DIR	LSLA 1 INH	LSLX 1 INH	LSL 2 IX1	LSL 3 SP1	LSL 1 IX	PULX 1 INH	CLC 1 INH	EOR 2 IMM	EOR 2 DIR	EOR 3 EXT	EOR 3 IX2	EOR 4 SP2	EOR 2 IX1	EOR 3 SP1	EOR 1 IX
9	BRCLR4 3 DIR	BCLR4 2 DIR	BHCS 2 REL	ROL 2 DIR	ROLA 1 INH	ROLX 1 INH	ROL 2 IX1	ROL 3 SP1	ROL 1 IX	PSHX 1 INH	SEC 1 INH	ADC 2 IMM	ADC 2 DIR	ADC 3 EXT	ADC 3 IX2	ADC 4 SP2	ADC 2 IX1	ADC 3 SP1	ADC 1 IX
A	BRSET5 3 DIR	BSET5 2 DIR	BPL 2 REL	DEC 2 DIR	DECA 1 INH	DECX 1 INH	DEC 2 IX1	DEC 3 SP1	DEC 1 IX	PULH 1 INH	CLI 1 INH	ORA 2 IMM	ORA 2 DIR	ORA 3 EXT	ORA 3 IX2	ORA 4 SP2	ORA 2 IX1	ORA 3 SP1	ORA 1 IX
B	BRCLR5 3 DIR	BCLR5 2 DIR	BMI 2 REL	DBNZ 3 DIR	DBNZA 2 INH	DBNZX 2 INH	DBNZ 3 IX1	DBNZ 4 SP1	DBNZ 2 IX	PSHH 1 INH	SEI 1 INH	ADD 2 IMM	ADD 2 DIR	ADD 3 EXT	ADD 3 IX2	ADD 4 SP2	ADD 2 IX1	ADD 3 SP1	ADD 1 IX
C	BRSET6 3 DIR	BSET6 2 DIR	BMC 2 REL	INC 2 DIR	INCA 1 INH	INCX 1 INH	INC 2 IX1	INC 3 SP1	INC 1 IX	CLRH 1 INH	RSP 1 INH		JMP 2 DIR	JMP 3 EXT	JMP 3 IX2		JMP 2 IX1		JMP 1 IX
D	BRCLR6 3 DIR	BCLR6 2 DIR	BMS 2 REL	TST 2 DIR	TSTA 1 INH	TSTX 1 INH	TST 2 IX1	TST 3 SP1	TST 1 IX		NOP 1 INH	BSR 2 REL	JSR 2 DIR	JSR 3 EXT	JSR 3 IX2		JSR 2 IX1		JSR 1 IX
E	BRSET7 3 DIR	BSET7 2 DIR	BIL 2 REL		MOV 3 DD	MOV 2 DIX+	MOV 3 IMD		MOV 2 IX+D	STOP 1 INH	*	LDX 2 IMM	LDX 2 DIR	LDX 3 EXT	LDX 3 IX2	LDX 4 SP2	LDX 2 IX1	LDX 3 SP1	LDX 1 IX
F	BRCLR7 3 DIR	BCLR7 2 DIR	BIH 2 REL	CLR 2 DIR	CLRA 1 INH	CLRAX 1 INH	CLR 2 IX1	CLR 3 SP1	CLR 1 IX	WAIT 1 INH	TXA 1 INH	AIX 2 IMM	STX 2 DIR	STX 3 EXT	STX 3 IX2	STX 4 SP2	STX 2 IX1	STX 3 SP1	STX 1 IX

INH Inherent
IMM Immediate
DIR Direct
EXT Extended
DD Direct-Direct
IX+D Indexed-Direct
REL Relative
IX Indexed, No Offset
IX1 Indexed, 8-Bit Offset
IX2 Indexed, 16-Bit Offset
IMD Immediate-Direct
DIX+ Direct-Indexed

SP1 Stack Pointer, 8-Bit Offset
SP2 Stack Pointer, 16-Bit Offset
IX+ Indexed, No Offset with Post Increment
IX1+ Indexed, 1-Byte Offset with Post Increment

Low Byte of Opcode in Hexadecimal

MSB LSB	0	High Byte of Opcode in Hexadecimal
0	5 BRSET0 3 DIR	Cycles Opcode Mnemonic Number of Bytes / Addressing Mode



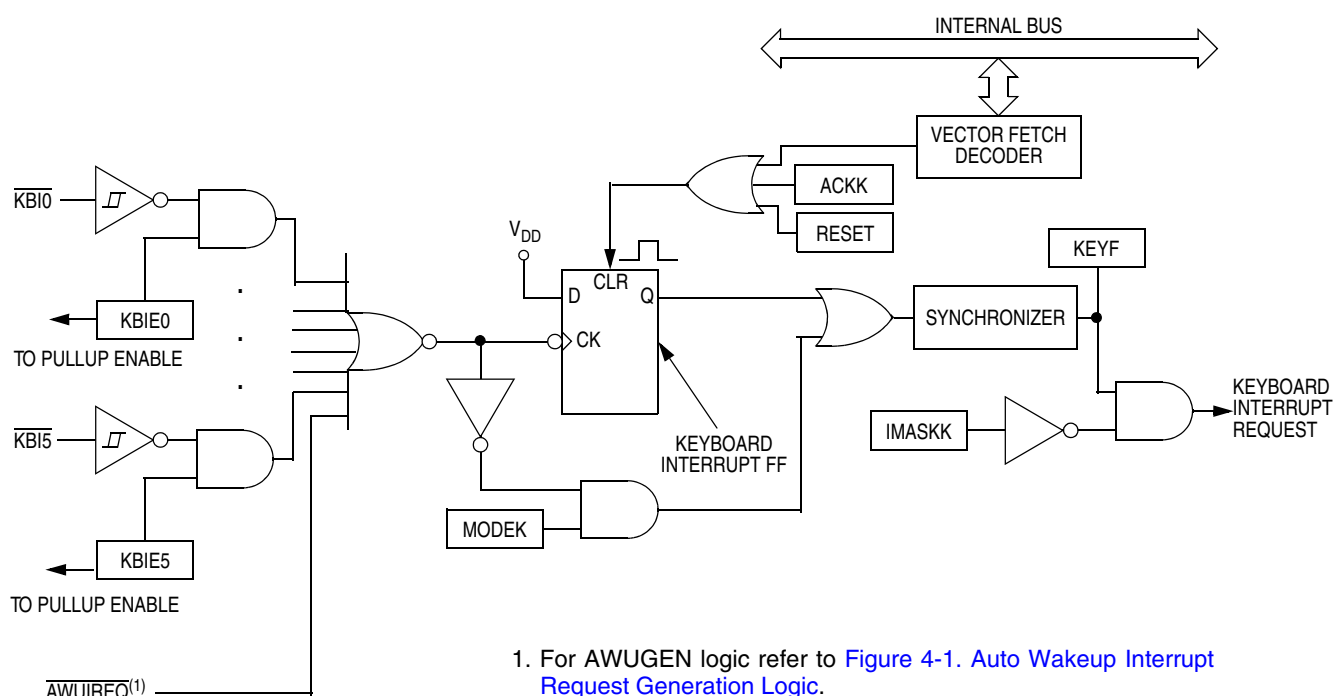


Figure 9-2. Keyboard Interrupt Block Diagram

If the MODEK bit is set, the keyboard interrupt inputs are both falling edge and low-level sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt inputs and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt inputs. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the central processor unit (CPU) loads the program counter with the vector address at locations \$FFE0 and \$FFE1.
- Return of all enabled keyboard interrupt inputs to logic 1 — As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set. The auto wakeup interrupt input, AWUIREQ, will be cleared only by writing to ACKK bit in KBSCR or reset.

The vector fetch or software clear and the return of all enabled keyboard interrupt pins to logic 1 may occur in any order.

If the MODEK bit is clear, the keyboard interrupt pin is falling-edge sensitive only. With MODEK clear, a vector fetch or software clear immediately clears the keyboard interrupt request.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt input stays at logic 0.

The keyboard flag bit (KEYF) in the keyboard status and control register can be used to see if a pending interrupt exists. The KEYF bit is not affected by the keyboard interrupt mask bit (IMASKK) which makes it useful in applications where polling is preferred.

Low-Voltage Inhibit (LVI)

The LVI is enabled out of reset. The LVI module contains a bandgap reference circuit and comparator. Clearing the LVI power disable bit (LVIPWRD) enables the LVI to monitor V_{DD} voltage. Clearing the LVI reset disable bit (LVIRSTD) enables the LVI module to generate a reset when V_{DD} falls below a voltage, V_{TRIPF} or V_{DTRIPF} . Setting the LVI enable in stop mode bit (LVISTOP) enables the LVI to operate in stop mode. Setting the LVD or LVR trip point bit (LVDLVR) selects the LVD trip point voltage. The actual trip thresholds are specified in [16.5 DC Electrical Characteristics](#). Either trip level can be used as a detect or reset.

NOTE

After a power-on reset, the LVI's default mode of operation is LVR trip voltage. If a higher trip voltage is desired, the user must set the LVDLVR bit to raise the trip point to the LVD voltage.

If the user requires the higher trip voltage and sets the LVDLVR bit after power-on reset while the V_{DD} supply is not above the V_{TRIPR} for LVD mode, the microcontroller unit (MCU) will immediately go into reset. The next time the LVI releases the reset, the supply will be above the V_{TRIPR} for LVD mode.

Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR} , which causes the MCU to exit reset. See [Chapter 13 System Integration Module \(SIM\)](#) for the reset recovery sequence.

The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR) and can be used for polling LVI operation when the LVI reset is disabled.

10.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be cleared to enable the LVI module, and the LVIRSTD bit must be set to disable LVI resets.

10.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, the LVIPWRD and LVIRSTD bits must be cleared to enable the LVI module and to enable LVI resets.

10.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR} . This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF} . V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS} .

10.3.4 LVI Trip Selection

The LVDLVR bit in the configuration register selects whether the LVI is configured for LVD (low voltage detect) or LVR (low voltage reset) protection. The LVD trip voltage can be used as a low voltage warning. The LVR trip voltage will commonly be configured as a reset condition since it is very close to the minimum operating voltage of the device. The LVDLVR bit can be written to anytime so that battery applications can make use of the LVI as both a warning indicator and to generate a system reset.

Chapter 11

Oscillator Module (OSC)

11.1 Introduction

The oscillator module is used to provide a stable clock source for the microcontroller system and bus. The oscillator module generates two output clocks, BUSCLKX2 and BUSCLKX4. The BUSCLKX4 clock is used by the system integration module (SIM) and the computer operating properly module (COP). The BUSCLKX2 clock is divided by two in the SIM to be used as the bus clock for the microcontroller. Therefore the bus frequency will be one forth of the BUSCLKX4 frequency.

11.2 Features

The oscillator has these four clock source options available:

1. Internal oscillator: An internally generated, fixed frequency clock, trimmable to $\pm 5\%$. This is the default option out of reset.
2. External oscillator: An external clock that can be driven directly into OSC1.
3. External RC: A built-in oscillator module (RC oscillator) that requires an external R connection only. The capacitor is internal to the chip.
4. External crystal: A built-in oscillator module (XTAL oscillator) that requires an external crystal or ceramic-resonator.

11.3 Functional Description

The oscillator contains these major subsystems:

- Internal oscillator circuit
- Internal or external clock switch control
- External clock circuit
- External crystal circuit
- External RC clock circuit

11.3.1 Internal Oscillator

The internal oscillator circuit is designed for use with no external components to provide a clock source with tolerance less than $\pm 25\%$ untrimmed. An 8-bit trimming register allows adjustment to a tolerance of less than $\pm 5\%$.

The internal oscillator will generate a clock of 4.0 MHz typical (INTCLK) resulting in a bus speed (internal clock $\div 4$) of 1.0 MHz.

[Figure 11-3](#) shows how BUSCLKX4 is derived from INTCLK and, like the RC oscillator, OSC2 can output BUSCLKX4 by setting OSC2EN in PTAPUE register. See [Chapter 12 Input/Output Ports \(PORTS\)](#).

Input/Output Ports (PORTS)

PTAPUE[5:0] — Port A Input Pullup Enable Bits

These read/write bits are software programmable to enable pullup devices on port A pins.

1 = Corresponding port A pin configured to have internal pull if its DDRA bit is set to 0

0 = Pullup device is disconnected on the corresponding port A pin regardless of the state of its DDRA bit

Table 12-1 summarizes the operation of the port A pins.

Table 12-1. Port A Pin Functions

PTAPUE Bit	DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
				Read/Write	Read	Write
1	0	X ⁽¹⁾	Input, V _{DD} ⁽²⁾	DDRA5–DDRA0	Pin	PTA5–PTA0 ⁽³⁾
0	0	X	Input, Hi-Z ⁽⁴⁾	DDRA5–DDRA0	Pin	PTA5–PTA0 ⁽³⁾
X	1	X	Output	DDRA5–DDRA0	PTA5–PTA0	PTA5–PTA0 ⁽⁵⁾

1. X = don't care
2. I/O pin pulled to V_{DD} by internal pullup.
3. Writing affects data register, but does not affect input.
4. Hi-Z = high impedance
5. Output does not apply to PTA2

12.3 Port B

Port B is an 8-bit general purpose I/O port. Port B is only available on the MC68HLC908QY1, MC68HLC908QY2, and MC68HLC908QY4.

12.3.1 Port B Data Register

The port B data register (PTB) contains a data latch for each of the eight port B pins.

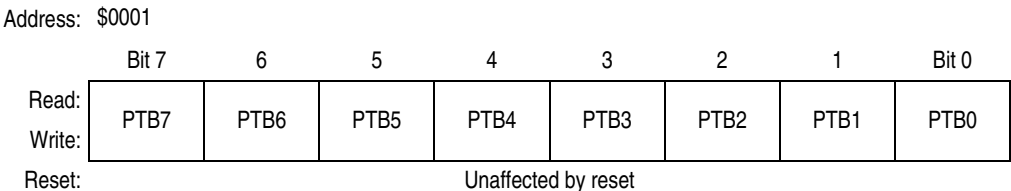
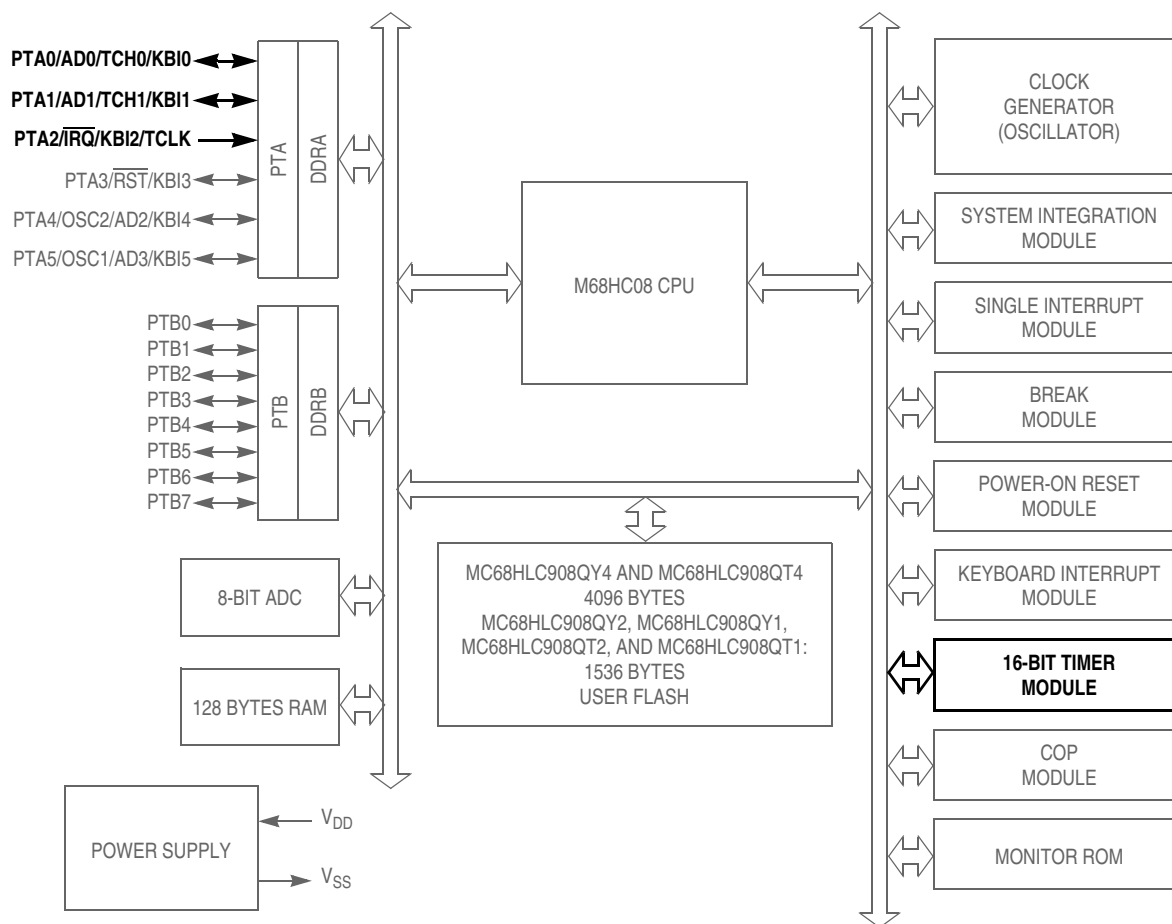


Figure 12-5. Port B Data Register (PTB)

PTB[7:0] — Port B Data Bits

These read/write bits are software programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

Timer Interface Module (TIM)



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30K Ohms) pull up

PTA[0:5]: High current sink and source capability

PTA[0:5]: Pins have programmable keyboard interrupt and pull up

PTB[0:7]: Not available on 8-pin devices – MC68HLC908QT1, MC68HLC908QT2, and MC68HLC908QT4 (see note in [12.1 Introduction](#))

ADC: Not available on the MC68HLC908QY1 and MC68HLC908QT1

Figure 14-1. Block Diagram Highlighting TIM Block and Pins

Figure 14-2 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The diagram illustrates the internal architecture of the TMR16B16 module. It features an **INTERNAL BUS** at the bottom, which connects to various components:

- PRESCALER**: Receives the **INTERNAL BUS CLOCK** and **TSTOP** (input) and **TRST** (input/output). It outputs to the **PRESCALER SELECT** block.
- PRESCALER SELECT**: Receives inputs from **PS2**, **PS1**, and **PS0**. It outputs to the **16-BIT COUNTER** and the **TOF** (Time-Out Flag) block.
- 16-BIT COUNTER**: Receives the prescaled clock and outputs to the **16-BIT COMPARATOR** and **TMODH:TMODL** (Time Modulus High/Low) block.
- 16-BIT COMPARATOR**: Outputs to the **16-BIT LATCH** and the **TOF** block.
- CHANNEL 0**: Consists of a **16-BIT COMPARATOR**, **TCH0H:TCH0L** (Time Counter High/Low), and **16-BIT LATCH**. It receives the **INTERNAL BUS** clock and outputs to the **ELS0B** and **ELS0A** (Event Source Latch Status) blocks.
- CHANNEL 1**: Consists of a **16-BIT COMPARATOR**, **TCH1H:TCH1L** (Time Counter High/Low), and **16-BIT LATCH**. It receives the **INTERNAL BUS** clock and outputs to the **ELS1B** and **ELS1A** blocks.
- ELS0B** and **ELS0A**: Inputs to a multiplier (\otimes) that produces the **CH0F** (Channel 0 Flag) signal.
- ELS1B** and **ELS1A**: Inputs to a multiplier (\otimes) that produces the **CH1F** (Channel 1 Flag) signal.
- CH0F** and **CH1F**: Inputs to a multiplier (\otimes) that produces the **TOV0** (Time-Out Value 0) and **CH0MAX** (Channel 0 Maximum) signals.
- TOV0** and **CH0MAX**: Inputs to the **PORT LOGIC** block, which outputs **TCH0** (Time Counter High 0).
- CH0IE** (Channel 0 Interrupt Enable): Input to the **INTERRUPT LOGIC** block, which outputs **TCH0**.
- TOV1** and **CH1MAX**: Inputs to the **PORT LOGIC** block, which outputs **TCH1** (Time Counter High 1).
- CH1IE** (Channel 1 Interrupt Enable): Input to the **INTERRUPT LOGIC** block, which outputs **TCH1**.

Figure 14-2. TIM Block Diagram

16.7 Typical 3.0-V Output Drive Characteristics

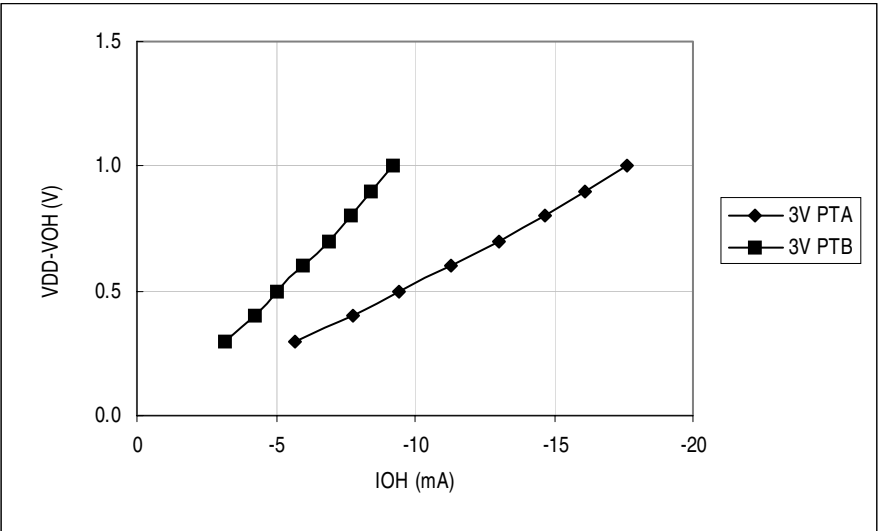


Figure 16-2. Typical 3-Volt Output High Voltage versus Output High Current (25°C)

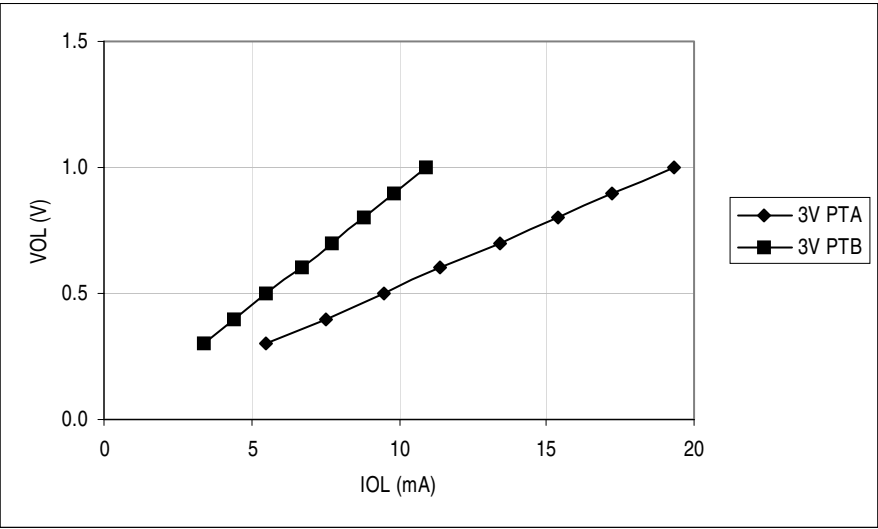


Figure 16-3. Typical 3-Volt Output Low Voltage versus Output Low Current (25°C)

16.11 Timer Interface Module Characteristics

Characteristic	Symbol	Min	Max	Unit
Timer input capture pulse width	t_{TH} , t_{TL}	2	—	t_{cyc}
Timer input capture period	t_{TLTL}	Note ⁽¹⁾	—	t_{cyc}
Timer input clock pulse width	t_{TCL} , t_{TCH}	$t_{cyc} + 5$	—	ns

1. The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{cyc} .

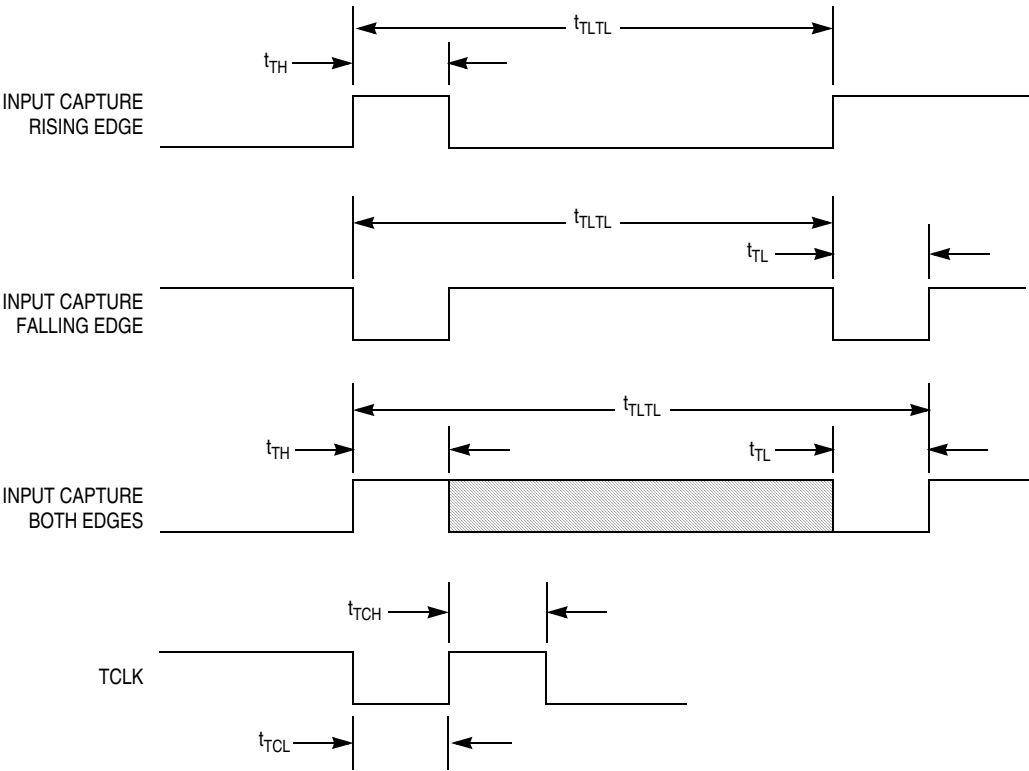


Figure 16-8. Timer Input Timing



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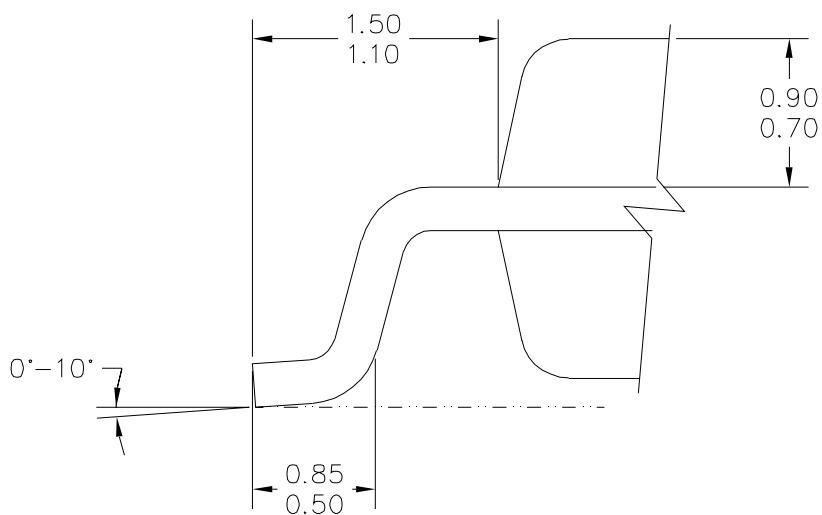
MECHANICAL OUTLINES DICTIONARY

DOCUMENT NO: 98ASH70107A

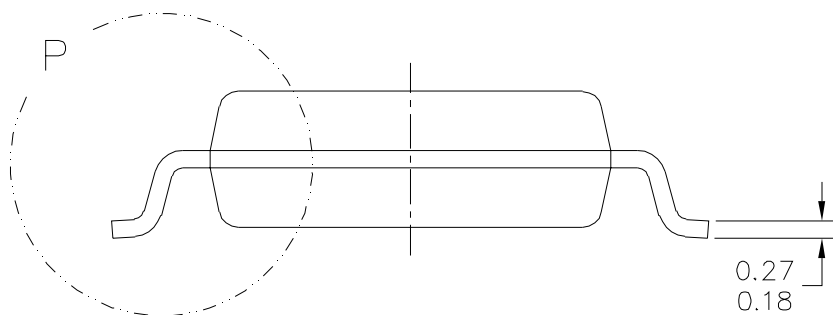
PAGE: 968

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DETAIL P



TITLE:

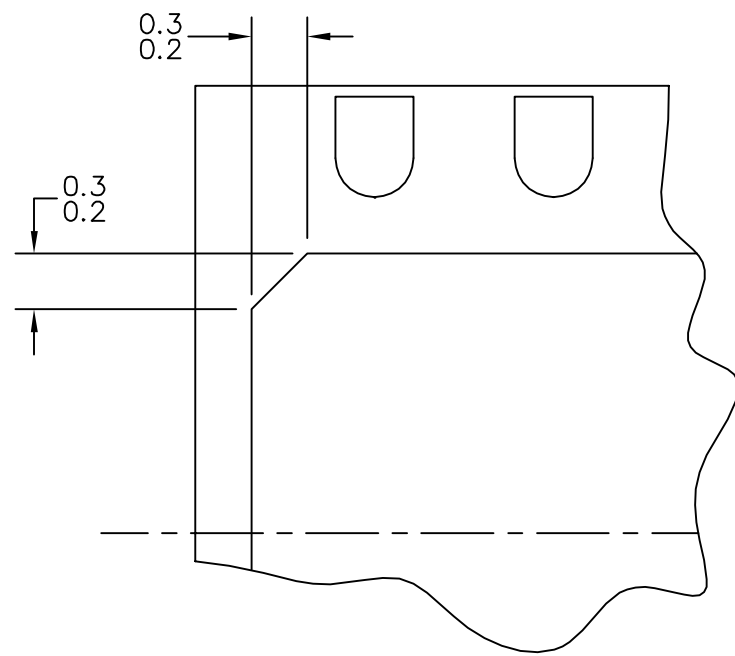
8 LEAD MFP

CASE NUMBER: 968-02

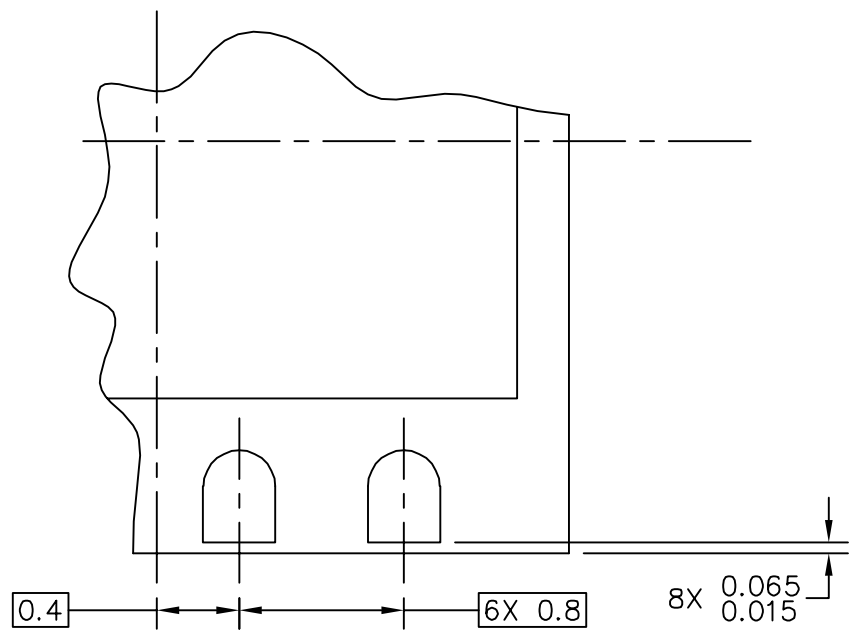
STANDARD: EIAJ

PACKAGE CODE: 6003

SHEET: 2 OF 4



DETAIL M
BACKSIDE PIN 1 INDEX



DETAIL N

TITLE: THERMALLY ENHANCED DUAL
FLAT NO LEAD PACKAGE (DFN)
8 TERMINAL, 0.8 PITCH (4 X 4 X 1)

CASE NUMBER: 1452-01

STANDARD: NON-JEDEC

PACKAGE CODE: 6165

SHEET: 3 OF 5



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MECHANICAL OUTLINES DICTIONARY

DOCUMENT NO: 98ASB42567B

PAGE: 751G

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REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

TITLE:
16LD SOIC W/B, 1.27 PITCH,
CASE OUTLINE

CASE NUMBER: 751G–05

STANDARD: JEDEC MS–013AA

PACKAGE CODE: 2003

SHEET: 2 OF 3