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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	5
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcl908qt2cdwe

Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
August, 2003	N/A	Initial release	N/A
October, 2003	1.0	Figure 2-2. Control, Status, and Data Registers Deleted unimplemented areas from \$FFB0–\$FFBD and \$FFC2–\$FFCF as they are actually available. Also corrected \$FFBF designation from unimplemented to reserved.	26
		Figure 6-1. COP Block Diagram — Reworked for clarity	57
		6.3.2 STOP Instruction — Added subsection for STOP instruction	58
		13.4.2 Active Resets from Internal Sources — Reworked notes for clarity.	115
		15.3 Monitor Module (MON) — Clarified seventh bullet.	154
		16.5 DC Electrical Characteristics — Corrected notes 4 and 5.	169
		16.6 Control Timing — Updated values for $\overline{\text{RST}}$ input pulse width low and $\overline{\text{IRQ}}$ interrupt pulse width low	170
January, 2004	2.0	Figure 2-2. Control, Status, and Data Registers — Corrected reset state for the FLASH Block Protect Register at address location \$FFBE and the Internal Oscillator Trim Value at \$FFC0.	30
		Figure 2-5. FLASH Block Protect Register (FLBPR) — Restated reset state for clarity.	37
July, 2005	3.0	Reformatted to meet current documentation standards	Throughout
		Chapter 7 Central Processor Unit (CPU) — In 7.7 Instruction Set Summary : Reworked definitions for STOP instruction Added WAIT instruction	70 71
		13.8.1 SIM Reset Status Register — Clarified SRSR flag setting.	117
		14.9.1 TIM Status and Control Register — Added information to TSTOP note.	127
		17.3 Package Dimensions — Updated package information.	163



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Chapter 2

Memory

2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in [Figure 2-1](#), includes:

- 4096 bytes of user FLASH for MC68HLC908QT4 and MC68HLC908QY4
- 1536 bytes of user FLASH for MC68HLC908QT2, MC68HLC908QT1, MC68HLC908QY2, and MC68HLC908QY1
- 128 bytes of random access memory (RAM)
- 48 bytes of user-defined vectors, located in FLASH
- 416 bytes of monitor read-only memory (ROM)
- 1536 bytes of FLASH program and erase routines, located in ROM

2.2 Unimplemented Memory Locations

Accessing an unimplemented location can have unpredictable effects on MCU operation. In [Figure 2-1](#) and in register figures in this document, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In [Figure 2-1](#) and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.

Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
<div> <div>Lowest</div> <div>↑</div> <div>↓</div> <div>Highest</div> </div>	IF15	\$FFDE	ADC conversion complete vector (high)
		\$FFDF	ADC conversion complete vector (low)
	IF14	\$FFE0	Keyboard vector (high)
		\$FFE1	Keyboard vector (low)
	IF13 ↓ IF6	—	Not used
	IF5	\$FFF2	TIM overflow vector (high)
		\$FFF3	TIM overflow vector (low)
	IF4	\$FFF4	TIM Channel 1 vector (high)
		\$FFF5	TIM Channel 1 vector (low)
	IF3	\$FFF6	TIM Channel 0 vector (high)
		\$FFF7	TIM Channel 0 vector (low)
	IF2	—	Not used
	IF1	\$FFFA	$\overline{\text{IRQ}}$ vector (high)
		\$FFFB	$\overline{\text{IRQ}}$ vector (low)
	—	\$FFFC	SWI vector (high)
		\$FFFD	SWI vector (low)
	—	\$FFFE	Reset vector (high)
		\$FFFF	Reset vector (low)

2.5 Random-Access Memory (RAM)

The 128 bytes of random-access memory (RAM) are located at addresses \$0080–\$00FF. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64-Kbyte memory space.

NOTE

For correct operation, the stack pointer must point only to RAM locations.

Before processing an interrupt, the central processor unit (CPU) uses five bytes of the stack to save the contents of the CPU registers.

NOTE

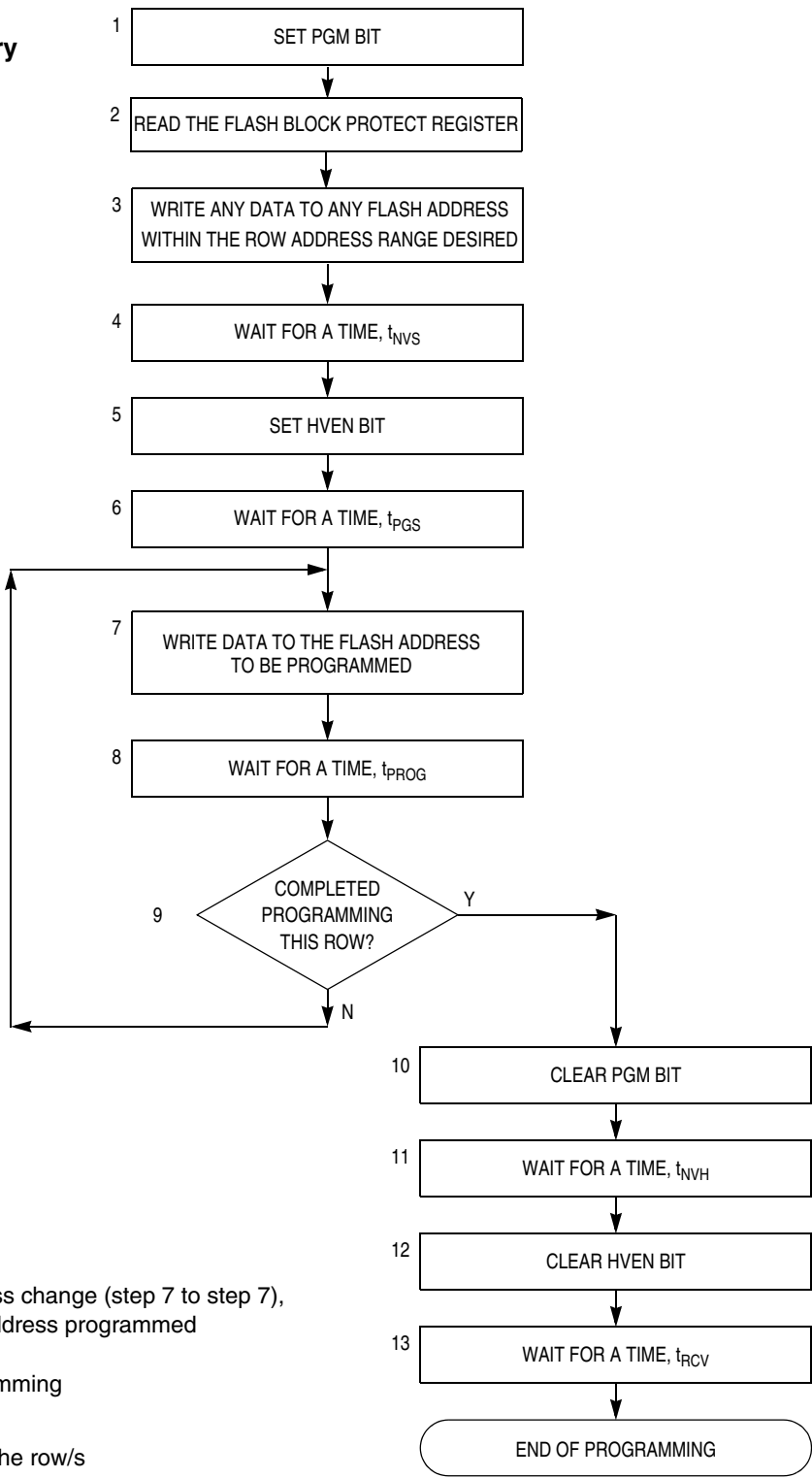
For M6805, M146805, and M68HC05 compatibility, the H register is not stacked.

During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

NOTE

Be careful when using nested subroutines. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.

**Algorithm for Programming
a Row (32 Bytes) of FLASH Memory**



NOTES:

The time between each FLASH address change (step 7 to step 7), or the time between the last FLASH address programmed to clearing PGM bit (step 7 to step 10) must not exceed the maximum programming time, $t_{\text{PROG max}}$.

This row program algorithm assumes the row/s to be programmed are initially erased.

Figure 2-4. FLASH Programming Flowchart

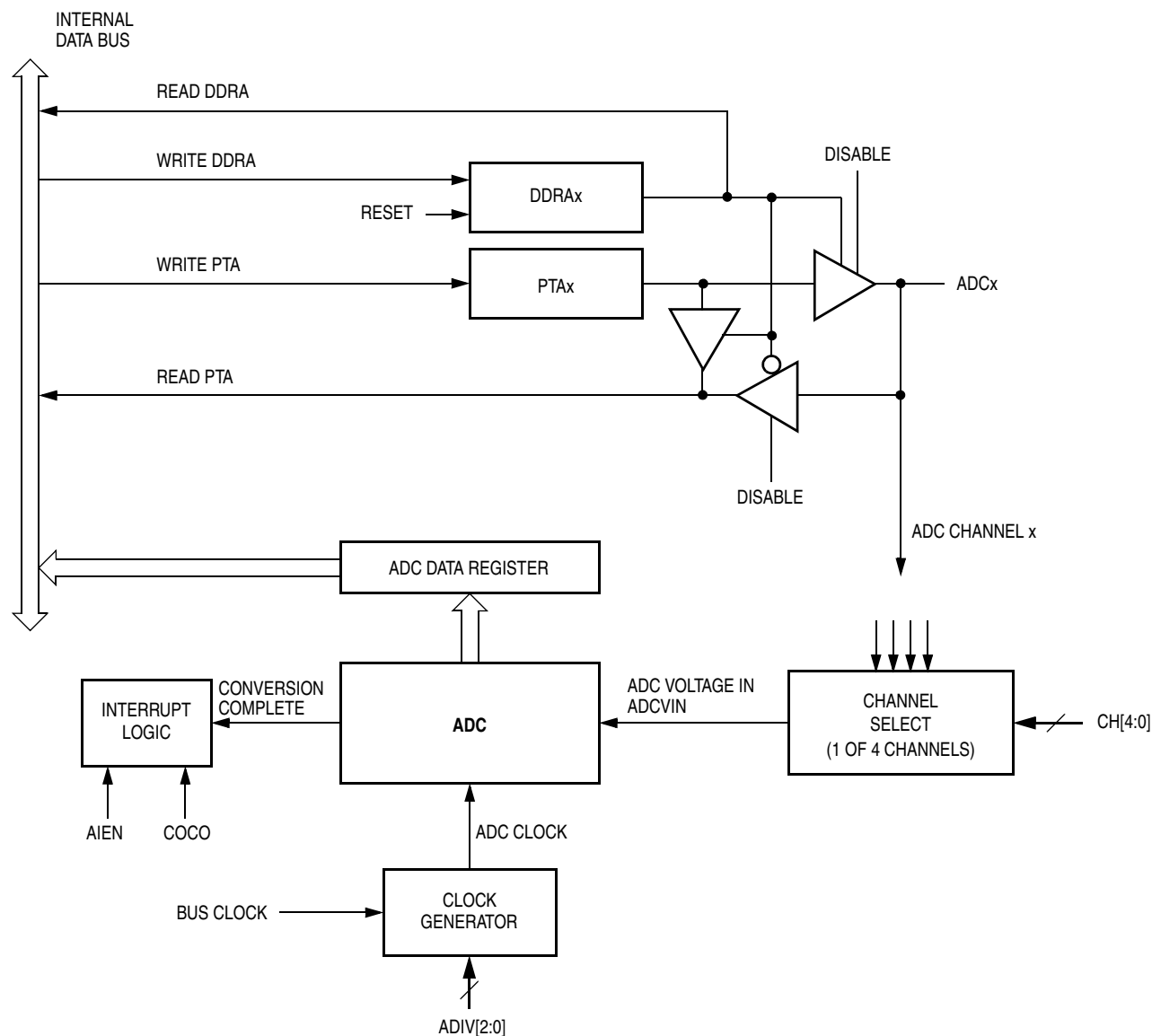


Figure 3-2. ADC Block Diagram

3.3.2 Voltage Conversion

When the input voltage to the ADC equals V_{DD} , the ADC converts the signal to \$FF (full scale). If the input voltage equals V_{SS} , the ADC converts it to \$00. Input voltages between V_{DD} and V_{SS} are a straight-line linear conversion. All other input voltages will result in \$FF if greater than V_{DD} and \$00 if less than V_{SS} .

NOTE

Input voltage should not exceed the analog supply voltages.

Chapter 4

Auto Wakeup Module (AWU)

4.1 Introduction

This section describes the auto wakeup module (AWU). The AWU generates a periodic interrupt during stop mode to wake the part up without requiring an external signal. [Figure 4-1](#) is a block diagram of the AWU.

4.2 Features

Features of the auto wakeup module include:

- One internal interrupt with separate interrupt enable bit, sharing the same keyboard interrupt vector and keyboard interrupt mask bit
- Exit from low-power stop mode without external signals
- Selectable timeout periods
- Dedicated low power internal oscillator separate from the main system clock sources

4.3 Functional Description

The function of the auto wakeup logic is to generate periodic wakeup requests to bring the microcontroller unit (MCU) out of stop mode. The wakeup requests are treated as regular keyboard interrupt requests, with the difference that instead of a pin, the interrupt signal is generated by an internal logic.

Writing the AWUIE bit in the keyboard interrupt enable register enables or disables the auto wakeup interrupt input (see [Figure 4-1](#)). A logic 1 applied to the AWUIREQ input with auto wakeup interrupt request enabled, latches an auto wakeup interrupt request.

Auto wakeup latch, AWUL, can be read directly from the bit 6 position of port A data register (PTA). This is a read-only bit which is occupying an empty bit position on PTA. No PTA associated registers, such as PTA6 data direction or PTA6 pullup exist for this bit.

Entering stop mode will enable the auto wakeup generation logic. An internal RC oscillator (exclusive for the auto wakeup feature) drives the wakeup request generator. Once the overflow count is reached in the generator counter, a wakeup request, AWUIREQ, is latched and sent to the KBI logic. See [Figure 4-1](#).

Wakeup interrupt requests will only be serviced if the associated interrupt enable bit, AWUIE, in KBIER is set. The AWU shares the keyboard interrupt vector.



- COPRS = 0: 875 ms @ 3.0 V, 1.1 s @ 2.3 V
- COPRS = 1: 22 ms @ 3.0 V, 27 ms @ 2.3 V

The wakeup request is latched to allow the interrupt source identification. The latched value, AWUL, can be read directly from the bit 6 position of PTA data register. This is a read-only bit which is occupying an empty bit position on PTA. No PTA associated registers, such as PTA6 data, PTA6 direction, and PTA6 pullup exist for this bit. The latch can be cleared by writing to the ACKK bit in the KBSCR register. Reset also clears the latch. AWUIE bit in KBI interrupt enable register (see [Figure 4-1](#)) has no effect on AWUL reading.

The AWU oscillator and counters are inactive in normal operating mode and become active only upon entering stop mode.



Configuration Register (CONFIG)

IRQPUD — $\overline{\text{IRQ}}$ Pin Pullup Control Bit

- 1 = Internal pullup is disconnected
- 0 = Internal pullup is connected between $\overline{\text{IRQ}}$ pin and V_{DD}

IRQEN — $\overline{\text{IRQ}}$ Pin Function Selection Bit

- 1 = Interrupt request function active in pin
- 0 = Interrupt request function inactive in pin

OSCOPT1 and OSCOPT0 — Selection Bits for Oscillator Option

- (0, 0) Internal oscillator
- (0, 1) External oscillator
- (1, 0) External RC oscillator
- (1, 1) External XTAL oscillator

RSTEN — $\overline{\text{RST}}$ Pin Function Selection

- 1 = Reset function active in pin
- 0 = Reset function inactive in pin

NOTE

The RSTEN bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.

Address: \$001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVDLVR	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	U	0	0	0
POR:	0	0	0	0	0	0	0	0

U = Unaffected

Figure 5-2. Configuration Register 1 (CONFIG1)

COPRS (Out of STOP Mode) — COP Reset Period Selection Bit

- 1 = COP reset short cycle = $8176 \times \text{BUSCLKX4}$
- 0 = COP reset long cycle = $262,128 \times \text{BUSCLKX4}$

COPRS (In STOP Mode) — Auto Wakeup Period Selection Bit

- 1 = Auto wakeup short cycle = $512 \times \text{INTRCOSC}$
- 0 = Auto wakeup long cycle = $16,384 \times \text{INTRCOSC}$

LVISTOP — LVI Enable in Stop Mode Bit

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

- 1 = LVI enabled during stop mode
- 0 = LVI disabled during stop mode

LVIRSTD — LVI Reset Disable Bit

LVIRSTD disables the reset signal from the LVI module. Unlike other configuration bits, the LVIRSTD can be written at any time.

- 1 = LVI module resets disabled
- 0 = LVI module resets enabled

Chapter 6

Computer Operating Properly (COP)

6.1 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the configuration 1 (CONFIG1) register.

6.2 Functional Description

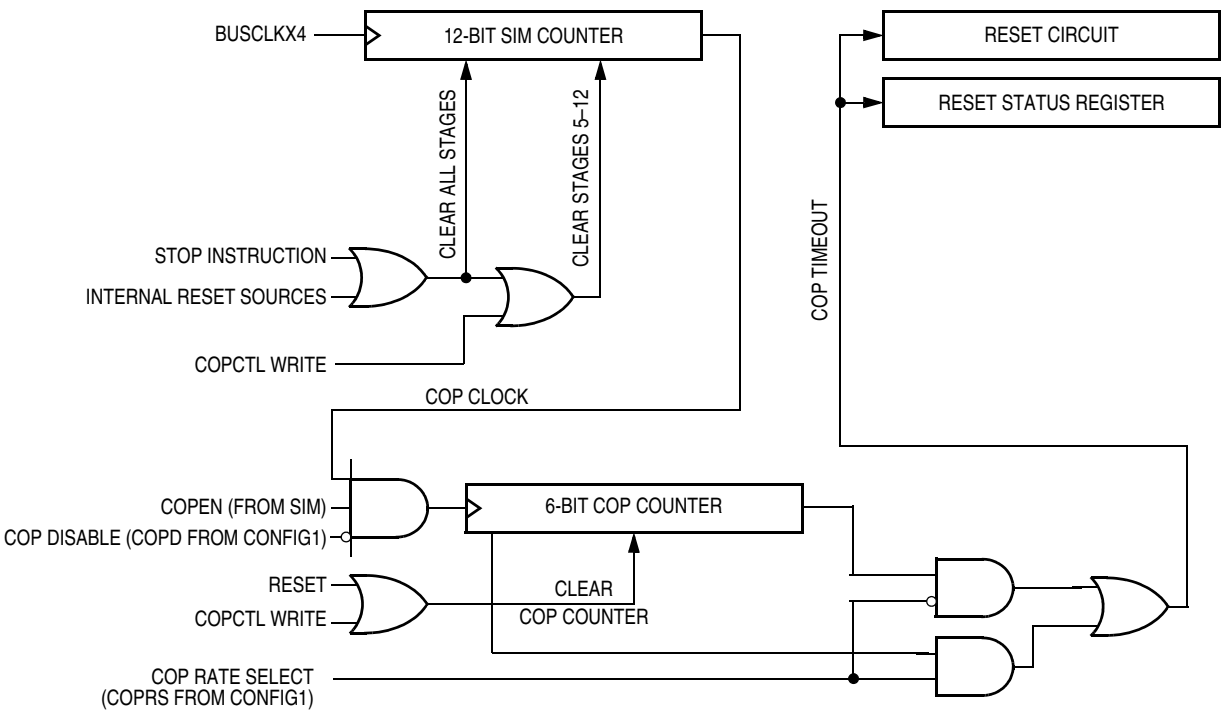


Figure 6-1. COP Block Diagram

Central Processor Unit (CPU)

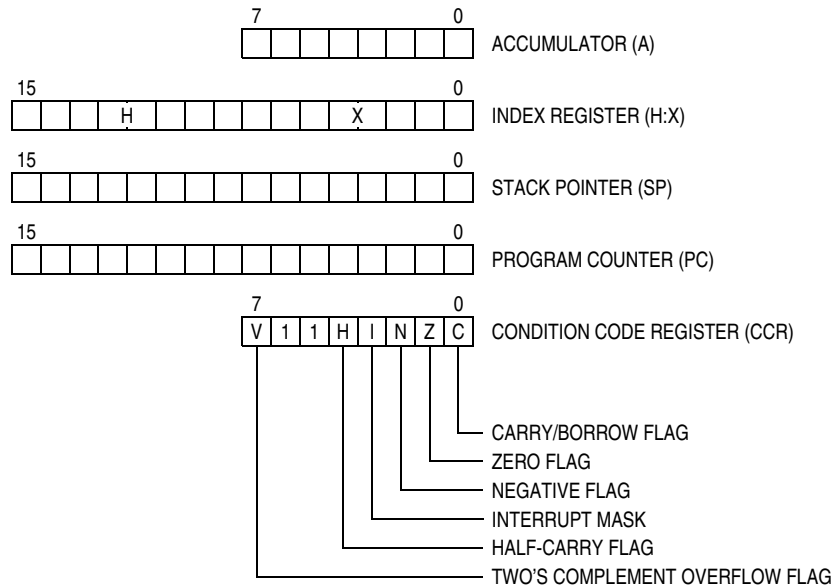


Figure 7-1. CPU Registers

7.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

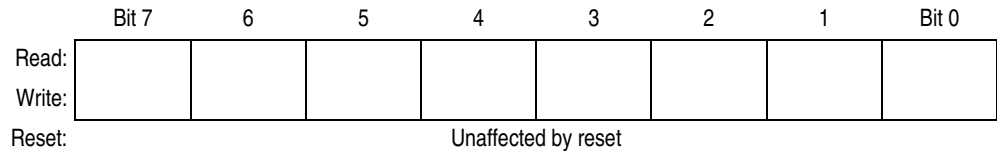


Figure 7-2. Accumulator (A)

7.3.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.

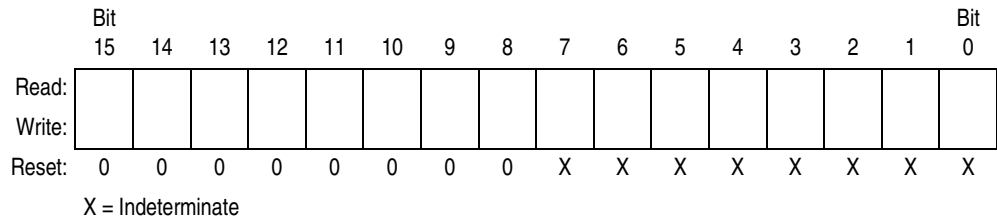


Figure 7-3. Index Register (H:X)

Chapter 8

External Interrupt (IRQ)

8.1 Introduction

The $\overline{\text{IRQ}}$ pin (external interrupt), shared with PTA2 (general purpose input) and keyboard interrupt (KBI), provides a maskable interrupt input.

8.2 Features

Features of the IRQ module include the following:

- External interrupt pin, $\overline{\text{IRQ}}$
- $\overline{\text{IRQ}}$ interrupt control bits
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Selectable internal pullup resistor

8.3 Functional Description

$\overline{\text{IRQ}}$ pin functionality is enabled by setting configuration register 2 (CONFIG2) IRQEN bit accordingly. A zero disables the IRQ function and PTA2 will assume the other shared functionalities. A one enables the IRQ function.

A low level applied to the external interrupt request ($\overline{\text{IRQ}}$) pin can latch a CPU interrupt request.

[Figure 8-2](#) shows the structure of the IRQ module.

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ latch. The IRQ latch remains set until one of the following actions occurs:

- IRQ vector fetch — An IRQ vector fetch automatically generates an interrupt acknowledge signal that clears the IRQ latch.
- Software clear — Software can clear the IRQ latch by writing a 1 to the ACK bit in the interrupt status and control register (INTSCR).
- Reset — A reset automatically clears the IRQ latch.

The external interrupt pin is falling-edge-triggered out of reset and is software-configurable to be either falling-edge or falling-edge and low-level triggered. The MODE bit in INTSCR controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

13.3.1 Bus Timing

In user mode, the internal bus frequency is the oscillator frequency (BUSCLKX4) divided by four.

13.3.2 Clock Start-Up from POR

When the power-on reset module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 BUSCLKX4 cycle POR time out has completed. The IBUS clocks start upon completion of the time out.

13.3.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt or reset, the SIM allows BUSCLKX4 to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay time out. This time out is selectable as 4096 or 32 BUSCLKX4 cycles. See [13.7.2 Stop Mode](#).

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

13.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector \$FFFE–FFFF (\$FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see [13.5 SIM Counter](#)), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See [13.8 SIM Registers](#).

13.4.1 External Pin Reset

The $\overline{\text{RST}}$ pin circuits include an internal pullup device. Pulling the asynchronous $\overline{\text{RST}}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{\text{RST}}$ is held low for at least the minimum t_{RL} time. [Figure 13-3](#) shows the relative timing. The $\overline{\text{RST}}$ pin function is only available if the RSTEN bit is set in the CONFIG2 register.

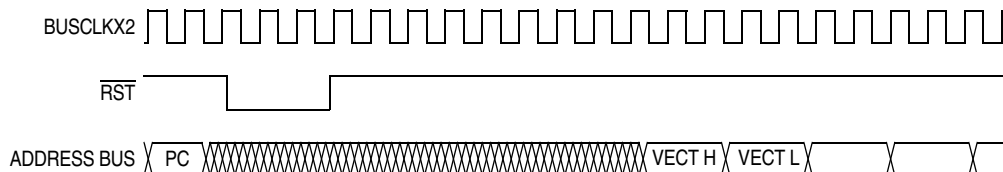


Figure 13-3. External Reset Timing

control the output are the ones written to last. TSC0 controls and monitors the buffered output compare function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

NOTE

In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.

14.4.4 Pulse Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM can generate a PWM signal. The value in the TIM counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM counter modulo registers. The time between overflows is the period of the PWM signal.

As [Figure 14-3](#) shows, the output compare value in the TIM channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM to clear the channel pin on output compare if the state of the PWM pulse is logic 1 (ELSxA = 0). Program the TIM to set the pin if the state of the PWM pulse is logic 0 (ELSxA = 1).

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing \$00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is 000. See [14.9.1 TIM Status and Control Register](#).

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing \$0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50%.

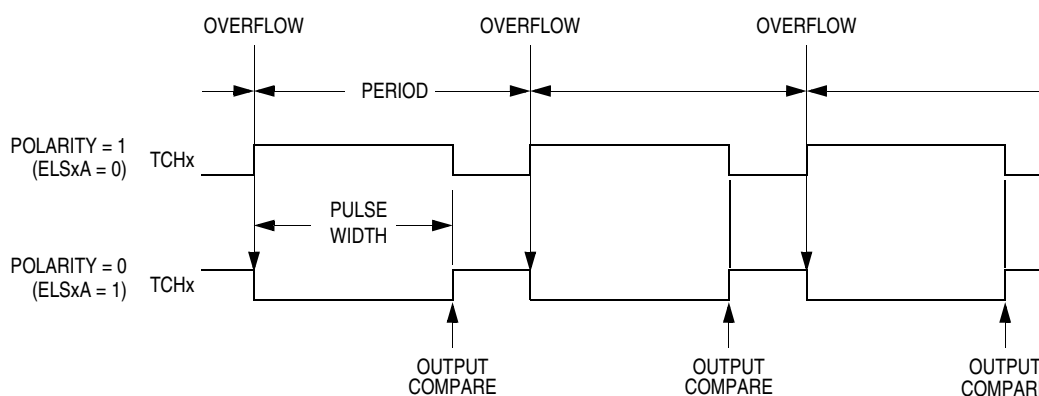


Figure 14-3. PWM Period and Pulse Width

14.6 Wait Mode

The WAIT instruction puts the MCU in low power-consumption standby mode.

The TIM remains active after the execution of a WAIT instruction. In wait mode the TIM registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

14.7 TIM During Break Interrupts

A break interrupt stops the TIM counter.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See [13.8.2 Break Flag Control Register](#).

To allow software to clear status bits during a break interrupt, write a 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at 0. After the break, doing the second step clears the status bit.

14.8 Input/Output Signals

Port A shares three of its pins with the TIM. Two TIM channel I/O pins are PTA0/TCH0 and PTA1/TCH1 and an alternate clock source is PTA2/TCLK.

14.8.1 TIM Clock Pin (PTA2/TCLK)

PTA2/TCLK is an external clock input that can be the clock source for the TIM counter instead of the prescaled internal bus clock. Select the PTA2/TCLK input by writing 1s to the three prescaler select bits, PS[2–0]. (See [14.9.1 TIM Status and Control Register](#).) When the PTA2/TCLK pin is the TIM clock input, it is an input regardless of port pin initialization.

14.8.2 TIM Channel I/O Pins (PTA0/TCH0 and PTA1/TCH1)

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. PTA0/TCH0 can be configured as a buffered output compare or buffered PWM pin.

14.9 Input/Output Registers

The following I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM counter registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0 and TSC1)
- TIM channel registers (TCH0H:TCH0L and TCH1H:TCH1L)

15.2.2.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.

Address: \$FE0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BRKE	BRKA	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0


 = Unimplemented

Figure 15-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a 0 to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match

0 = Breaks disabled

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a 1 to BRKA generates a break interrupt. Clear BRKA by writing a 0 to it before exiting the break routine. Reset clears the BRKA bit.

1 = Break address match

0 = No break address match

15.2.2.2 Break Address Registers

The break address registers (BRKH and BRKL) contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

Address: \$FE09

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 15-4. Break Address Register High (BRKH)

Address: \$FE0A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 15-5. Break Address Register Low (BRKL)



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5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF
THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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