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#### Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mcl908qy2cdwe">https://www.e-xfl.com/product-detail/nxp-semiconductors/mcl908qy2cdwe</a>

## Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

## Revision History

Date	Revision Level	Description	Page Number(s)
August, 2003	N/A	Initial release	N/A
October, 2003	1.0	Figure 2-2. Control, Status, and Data Registers Deleted unimplemented areas from \$FFB0–\$FFBD and \$FFC2–\$FFCF as they are actually available. Also corrected \$FFBF designation from unimplemented to reserved.	26
		Figure 6-1. COP Block Diagram — Reworked for clarity	57
		6.3.2 STOP Instruction — Added subsection for STOP instruction	58
		13.4.2 Active Resets from Internal Sources — Reworked notes for clarity.	115
		15.3 Monitor Module (MON) — Clarified seventh bullet.	154
		16.5 DC Electrical Characteristics — Corrected notes 4 and 5.	169
		16.6 Control Timing — Updated values for $\overline{\text{RST}}$ input pulse width low and $\overline{\text{IRQ}}$ interrupt pulse width low	170
January, 2004	2.0	Figure 2-2. Control, Status, and Data Registers — Corrected reset state for the FLASH Block Protect Register at address location \$FFBE and the Internal Oscillator Trim Value at \$FFC0.	30
		Figure 2-5. FLASH Block Protect Register (FLBPR) — Restated reset state for clarity.	37
July, 2005	3.0	Reformatted to meet current documentation standards	Throughout
		<a href="#">Chapter 7 Central Processor Unit (CPU)</a> — In <a href="#">7.7 Instruction Set Summary</a> : Reworked definitions for STOP instruction Added WAIT instruction	<a href="#">70</a> <a href="#">71</a>
		<a href="#">13.8.1 SIM Reset Status Register</a> — Clarified SRSR flag setting.	<a href="#">117</a>
		<a href="#">14.9.1 TIM Status and Control Register</a> — Added information to TSTOP note.	<a href="#">127</a>
		<a href="#">17.3 Package Dimensions</a> — Updated package information.	<a href="#">163</a>



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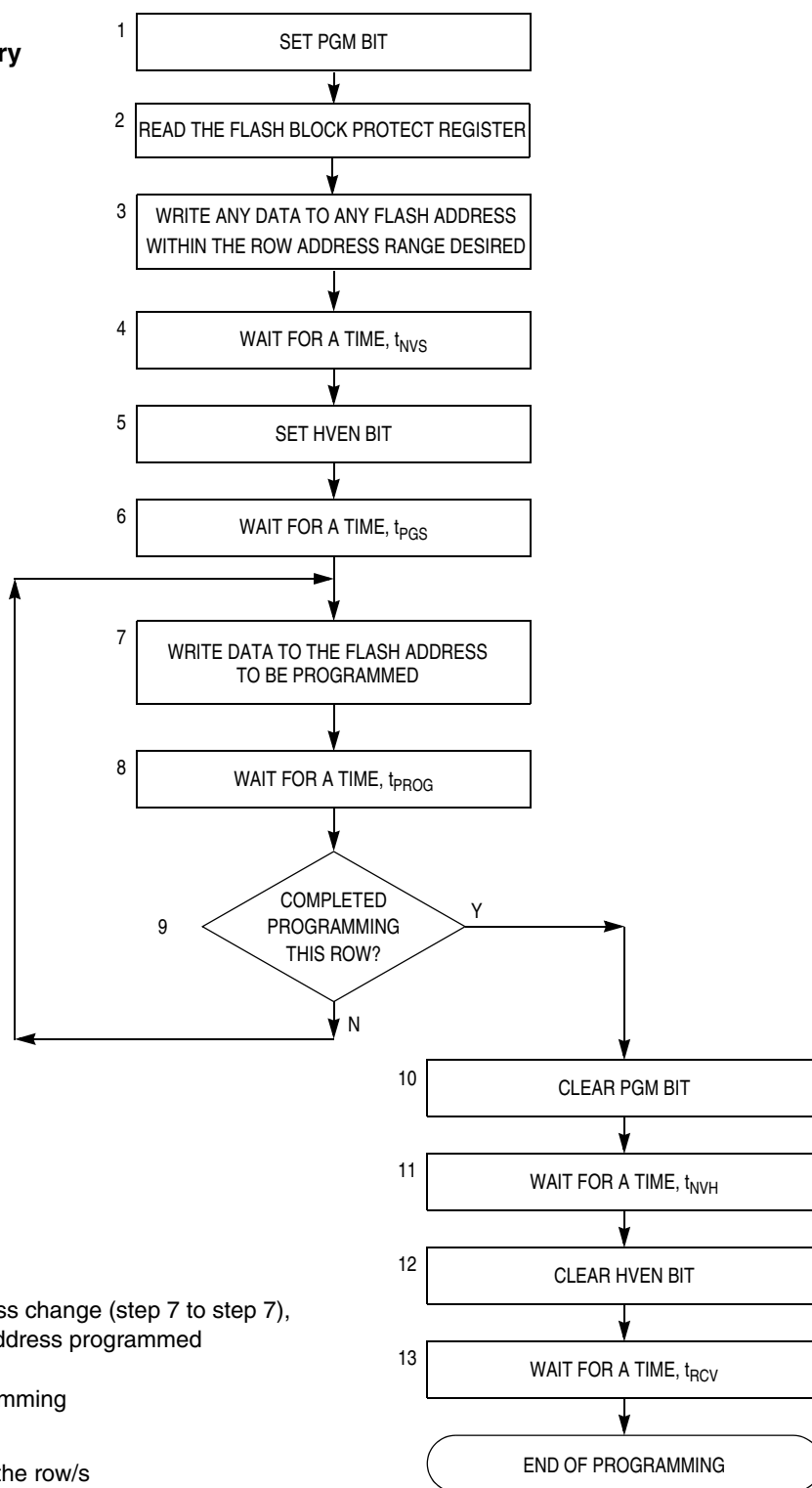
## Memory

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$0029	TIM Channel 1 Register High (TCH1H) <a href="#">See page 133.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9
		Write:	Bit 8						
		Reset:	Indeterminate after reset						
\$002A	TIM Channel 1 Register Low (TCH1L) <a href="#">See page 133.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
		Write:	Bit 0						
		Reset:	Indeterminate after reset						
\$002B ↓ \$0035	Unimplemented								
\$0036	Oscillator Status Register (OSCSTAT) <a href="#">See page 95.</a>	Read:	R	R	R	R	R	ECGON	ECGST
		Write:							
		Reset:	0	0	0	0	0	0	0
\$0037	Unimplemented	Read:							
\$0038	Oscillator Trim Register (OSCTRIM) <a href="#">See page 96.</a>	Read:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1
		Write:	TRIM0						
		Reset:	1	0	0	0	0	0	0
\$0039 ↓ \$003B	Unimplemented								
\$003C	ADC Status and Control Register (ADSCR) <a href="#">See page 43.</a>	Read:	COCO	AIEN	ADCO	CH4	CH3	CH2	CH1
		Write:	R						
		Reset:	0	0	0	1	1	1	1
\$003D	Unimplemented								
\$003E	ADC Data Register (ADR) <a href="#">See page 44.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
		Write:	Bit 0						
		Reset:	Indeterminate after reset						
\$003F	ADC Input Clock Register (ADICLK) <a href="#">See page 45.</a>	Read:	ADIV2	ADIV1	ADIV0	0	0	0	0
		Write:							
		Reset:	0	0	0	0	0	0	0

  = Unimplemented    
 R = Reserved    
 U = Unaffected

**Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 6)**

# Algorithm for Programming a Row (32 Bytes) of FLASH Memory



## NOTES:

The time between each FLASH address change (step 7 to step 7), or the time between the last FLASH address programmed to clearing PGM bit (step 7 to step 10) must not exceed the maximum programming time,  $t_{PROG}$  max.

This row program algorithm assumes the row/s to be programmed are initially erased.

**Figure 2-4. FLASH Programming Flowchart**

# Chapter 5

## Configuration Register (CONFIG)

### 5.1 Introduction

This section describes the configuration registers (CONFIG1 and CONFIG2). The configuration registers enable or disable the following options:

- Stop mode recovery time ( $32 \times \text{BUSCLKX4}$  cycles or  $4096 \times \text{BUSCLKX4}$  cycles)
- STOP instruction
- Computer operating properly module (COP)
- COP reset period (COPRS):  $8176 \times \text{BUSCLKX4}$  or  $262,128 \times \text{BUSCLKX4}$
- Low-voltage inhibit (LVI) enable and trip voltage selection
- OSC option selection
- $\overline{\text{IRQ}}$  pin
- $\overline{\text{RST}}$  pin
- Auto wakeup timeout period

### 5.2 Functional Description

The configuration registers are used in the initialization of various options. The configuration registers can be written once after each reset. Exceptions are bits LVDLVR and LVIRSTD which may be written at any time. Most of the configuration register bits are cleared during reset. Since the various options affect the operation of the microcontroller unit (MCU) it is recommended that this register be written immediately after reset. The configuration registers are located at \$001E and \$001F, and may be read at anytime.

Address: \$001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	IRQEN	R	OSCOPT1	OSCOPT0	R	R	RSTEN
Write:								
Reset:	0	0	0	0	0	0	0	U
POR:	0	0	0	0	0	0	0	0

R = Reserved      U = Unaffected

**Figure 5-1. Configuration Register 2 (CONFIG2)**





### Z — Zero Flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of \$00.

1 = Zero result

0 = Non-zero result

### C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

1 = Carry out of bit 7

0 = No carry out of bit 7

## 7.4 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

## 7.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

### 7.5.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

### 7.5.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

## 7.6 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with \$FFFC:\$FFFD or with \$FEFC:\$FEFD in monitor mode

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

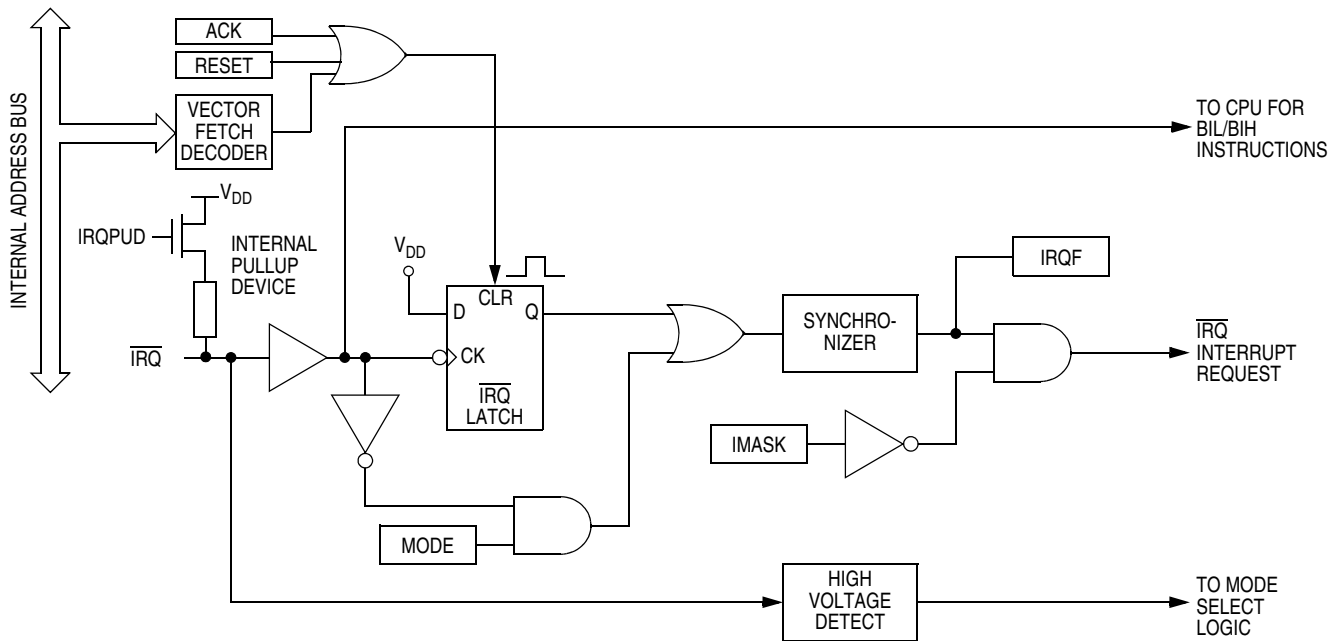


Figure 8-2. IRQ Module Block Diagram

### 8.3.1 MODE = 1

If the MODE bit is set, the  $\overline{\text{IRQ}}$  pin is both falling edge sensitive and low level sensitive. With MODE set, both of the following actions must occur to clear the  $\overline{\text{IRQ}}$  interrupt request:

- Return of the  $\overline{\text{IRQ}}$  pin to a high level. As long as the  $\overline{\text{IRQ}}$  pin is low, the IRQ request remains active.
- IRQ vector fetch or software clear. An IRQ vector fetch generates an interrupt acknowledge signal to clear the IRQ latch. Software generates the interrupt acknowledge signal by writing a 1 to ACK in INTSCR. The ACK bit is useful in applications that poll the  $\overline{\text{IRQ}}$  pin and require software to clear the IRQ latch. Writing to ACK prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACK does not affect subsequent transitions on the  $\overline{\text{IRQ}}$  pin. A falling edge that occurs after writing to ACK latches another interrupt request. If the IRQ mask bit, IMASK, is clear, the CPU loads the program counter with the IRQ vector address.

The IRQ vector fetch or software clear and the return of the  $\overline{\text{IRQ}}$  pin to a high level may occur in any order. The interrupt request remains pending as long as the  $\overline{\text{IRQ}}$  pin is low. A reset will clear the IRQ latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

Use the BIH or BIL instruction to read the logic level on the  $\overline{\text{IRQ}}$  pin.

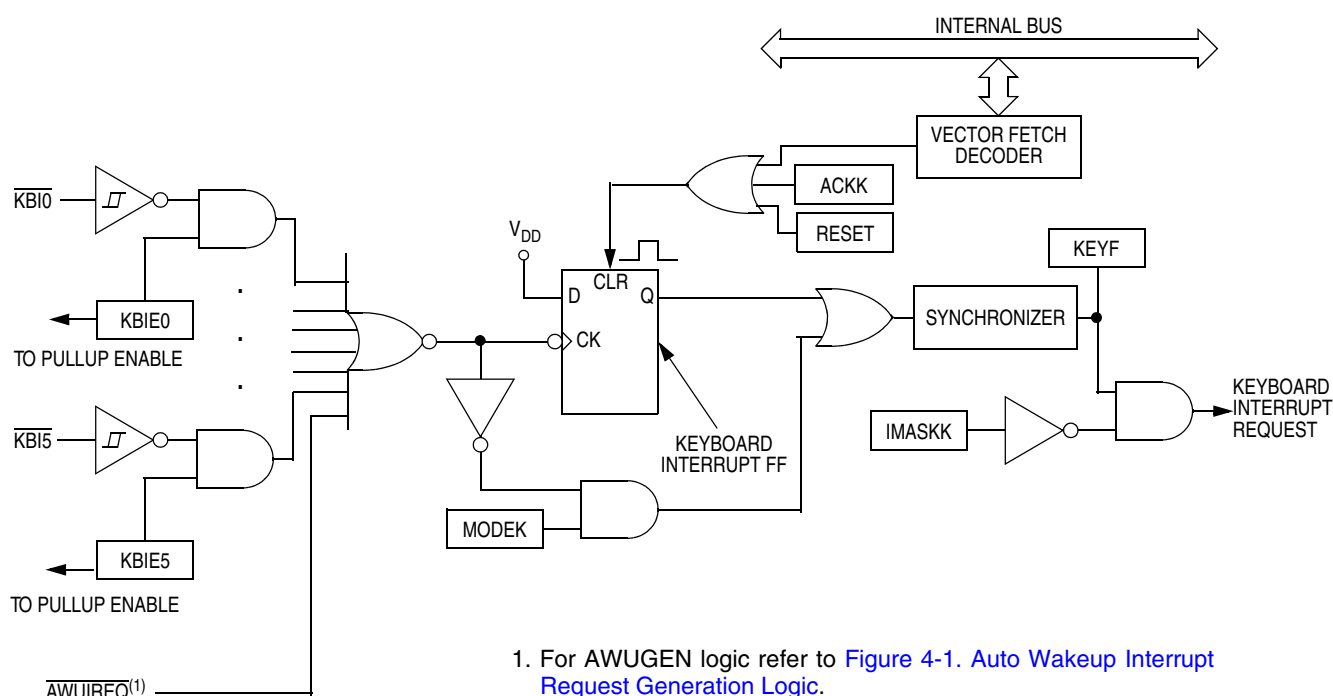
### 8.3.2 MODE = 0

If the MODE bit is clear, the  $\overline{\text{IRQ}}$  pin is falling edge sensitive only. With MODE clear, an IRQ vector fetch or software clear immediately clears the IRQ latch.

The IRQF bit in INTSCR can be read to check for pending interrupts. The IRQF bit is not affected by IMASK, which makes it useful in applications where polling is preferred.

#### NOTE

*When using the level-sensitive interrupt trigger, avoid false IRQ interrupts by masking interrupt requests in the interrupt routine.*



**Figure 9-2. Keyboard Interrupt Block Diagram**

If the MODEK bit is set, the keyboard interrupt inputs are both falling edge and low-level sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt inputs and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt inputs. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the central processor unit (CPU) loads the program counter with the vector address at locations \$FFE0 and \$FFE1.
- Return of all enabled keyboard interrupt inputs to logic 1 — As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set. The auto wakeup interrupt input, AWUIREQ, will be cleared only by writing to ACKK bit in KBSCR or reset.

The vector fetch or software clear and the return of all enabled keyboard interrupt pins to logic 1 may occur in any order.

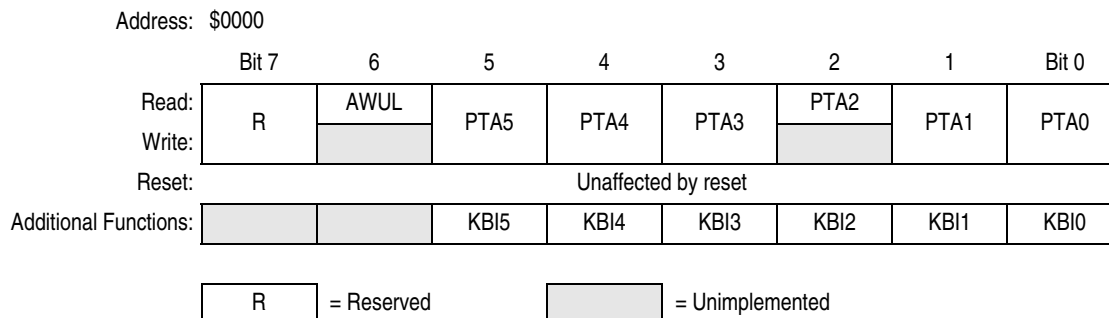
If the MODEK bit is clear, the keyboard interrupt pin is falling-edge sensitive only. With MODEK clear, a vector fetch or software clear immediately clears the keyboard interrupt request.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt input stays at logic 0.

The keyboard flag bit (KEYF) in the keyboard status and control register can be used to see if a pending interrupt exists. The KEYF bit is not affected by the keyboard interrupt mask bit (IMASKK) which makes it useful in applications where polling is preferred.

## 12.2.1 Port A Data Register

The port A data register (PTA) contains a data latch for each of the six port A pins.



**Figure 12-1. Port A Data Register (PTA)**

### PTA[5:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

### AWUL — Auto Wakeup Latch Data Bit

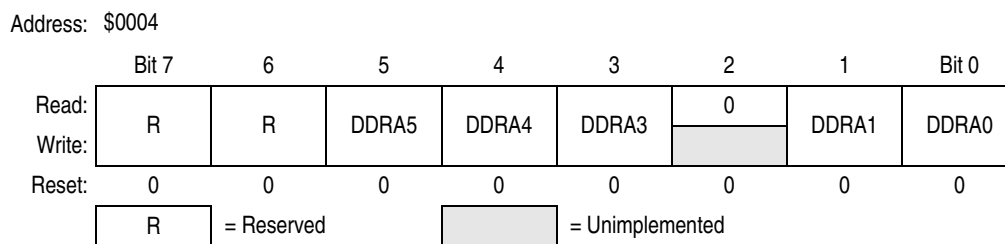
This is a read-only bit which has the value of the auto wakeup interrupt request latch. The wakeup request signal is generated internally (see [Chapter 4 Auto Wakeup Module \(AWU\)](#)). There is no PTA6 port nor any of the associated bits such as PTA6 data register, pullup enable or direction.

### KBI[5:0] — Port A Keyboard Interrupts

The keyboard interrupt enable bits, KBIE5–KBIE0, in the keyboard interrupt control enable register (KBIER) enable the port A pins as external interrupt pins (see [Chapter 9 Keyboard Interrupt Module \(KBI\)](#)).

## 12.2.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output. Writing a 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a 0 disables the output buffer.



**Figure 12-2. Data Direction Register A (DDRA)**

### DDRA[5:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[5:0], configuring all port A pins as inputs.

- 1 = Corresponding port A pin configured as output
- 0 = Corresponding port A pin configured as input

#### NOTE

*Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.*

Figure 12-3 shows the port A I/O logic.

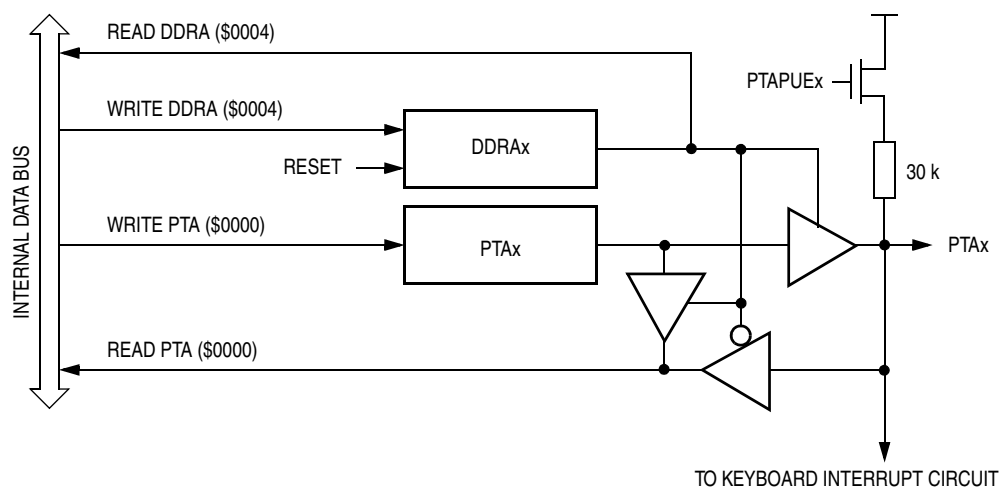


Figure 12-3. Port A I/O Circuit

**NOTE**

Figure 12-3 does not apply to PTA2

When DDRAx is a 1, reading address \$0000 reads the PTAx data latch. When DDRAx is a 0, reading address \$0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

### 12.2.3 Port A Input Pullup Enable Register

The port A input pullup enable register (PTAPUE) contains a software configurable pullup device for each of the six port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx, to be configured as input. Each pullup device is automatically and dynamically disabled when its corresponding DDRAx bit is configured as output.

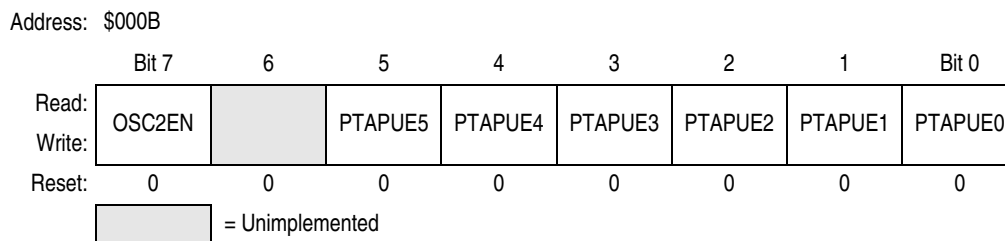


Figure 12-4. Port A Input Pullup Enable Register (PTAPUE)

#### OSC2EN — Enable PTA4 on OSC2 Pin

This read/write bit configures the OSC2 pin function when internal oscillator or RC oscillator option is selected. This bit has no effect for the XTAL or external oscillator options.

1 = OSC2 pin outputs the internal or RC oscillator clock (BUSCLKX4)

0 = OSC2 pin configured for PTA4 I/O, having all the interrupt and pullup functions

### 12.3.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output. Writing a 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a 0 disables the output buffer.

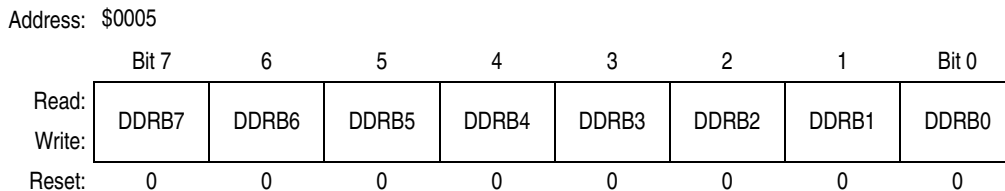


Figure 12-6. Data Direction Register B (DDRB)

#### DDRB[7:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[7:0], configuring all port B pins as inputs.

- 1 = Corresponding port B pin configured as output
- 0 = Corresponding port B pin configured as input

#### NOTE

Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1. Figure 12-7 shows the port B I/O logic.

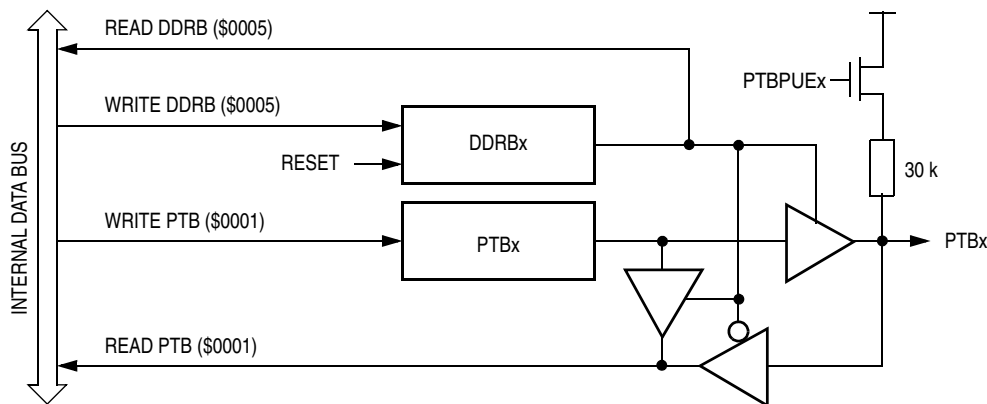


Figure 12-7. Port B I/O Circuit

When DDRBx is a 1, reading address \$0001 reads the PTBx data latch. When DDRBx is a 0, reading address \$0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 12-2 summarizes the operation of the port B pins.

Table 12-2. Port B Pin Functions

DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
			Read/Write	Read	Write
0	X <sup>(1)</sup>	Input, Hi-Z <sup>(2)</sup>	DDRB7–DDRB0	Pin	PTB7–PTB0 <sup>(3)</sup>
1	X	Output	DDRB7–DDRB0	Pin	PTB7–PTB0

1. X = don't care

2. Hi-Z = high impedance

3. Writing affects data register, but does not affect the input.

### IF1 and IF3–IF5 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

### Bit 0, 1, 3, and 7 — Always read 0

#### 13.6.2.2 Interrupt Status Register 2

Address: \$FE05

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IF14	0	0	0	0	0	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 13-12. Interrupt Status Register 2 (INT2)**

### IF14 — Interrupt Flags

This flag indicates the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

### Bit 0–6 — Always read 0

#### 13.6.2.3 Interrupt Status Register 3

Address: \$FE06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	IF15
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 13-13. Interrupt Status Register 3 (INT3)**

### IF15 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

### Bit 1–7 — Always read 0

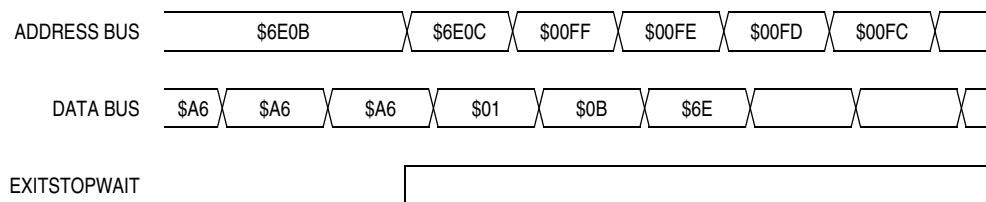
## 13.6.3 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

## 13.6.4 Break Interrupts

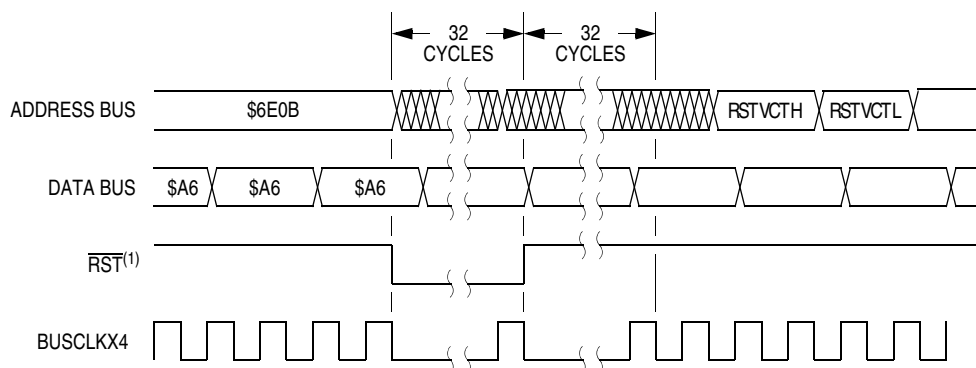
The break module can stop normal program flow at a software programmable break point by asserting its break interrupt output. (See [Chapter 15 Development Support](#).) The SIM puts the CPU into the break

Figure 13-15 and Figure 13-16 show the timing for wait recovery.



NOTE: EXITSTOPWAIT =  $\overline{\text{RST}}$  pin OR CPU interrupt

**Figure 13-15. Wait Recovery from Interrupt**



1.  $\overline{\text{RST}}$  is only available if the RSTEN bit in the CONFIG1 register is set.

**Figure 13-16. Wait Recovery from Internal Reset**

### 13.7.2 Stop Mode

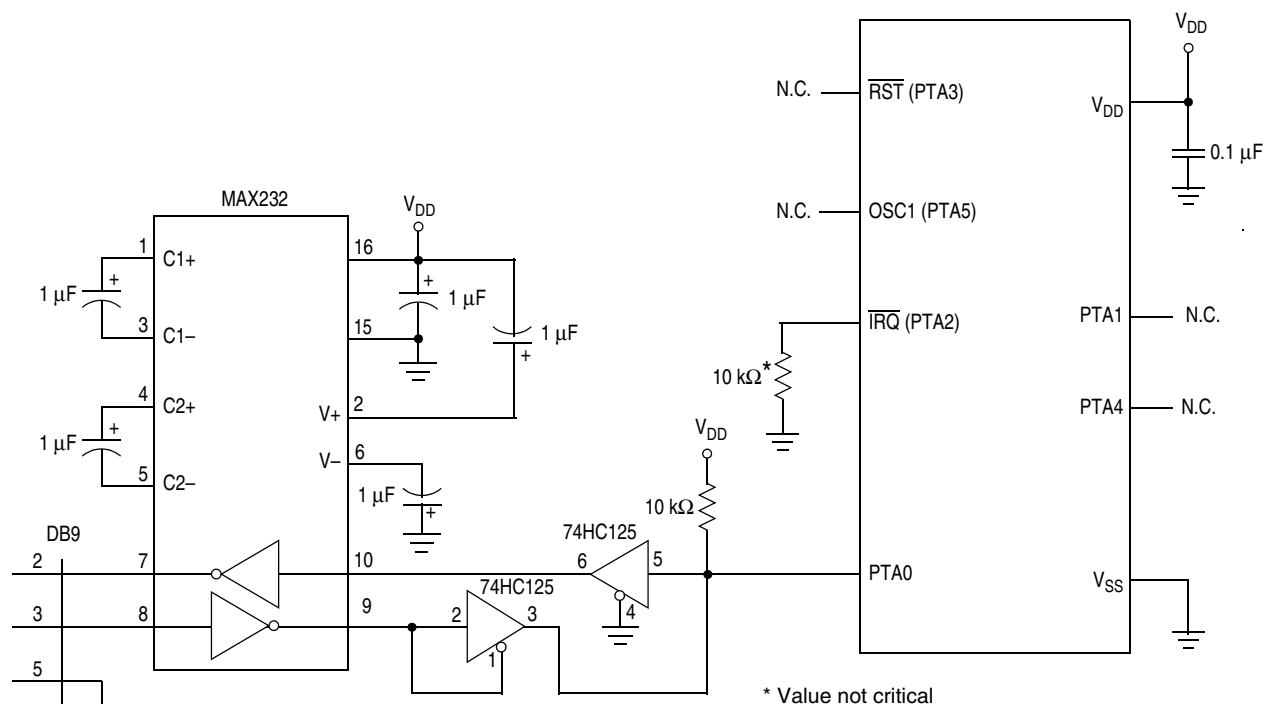
In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

The SIM disables the oscillator signals (BUSCLKX2 and BUSCLKX4) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register 1 (CONFIG1). If SSREC is set, stop recovery is reduced from the normal delay of 4096 BUSCLKX4 cycles down to 32. This is ideal for the internal oscillator, RC oscillator, and external oscillator options which do not require long start-up times from stop mode.

#### NOTE

*External crystal applications should use the full stop recovery time by clearing the SSREC bit.*





**Figure 15-12. Monitor Mode Circuit (Internal Clock, No High Voltage)**

The monitor code has been updated from previous versions of the monitor code to allow enabling the internal oscillator to generate the internal clock. This addition, which is enabled when  $\overline{\text{IRQ}}$  is held low out of reset, is intended to support serial communication/programming at 4800 baud in monitor mode by using the internal oscillator, and the internal oscillator user trim value  $\text{OSCTRIM}$  (FLASH location \$FFC0, if programmed) to generate the desired internal frequency (1.0 MHz). Since this feature is enabled only when  $\overline{\text{IRQ}}$  is held low out of reset, it cannot be used when the reset vector is programmed (i.e., the value is not \$FFFF) because entry into monitor mode in this case requires  $V_{\text{TST}}$  on  $\overline{\text{IRQ}}$ . The  $\overline{\text{IRQ}}$  pin must remain low during this monitor session in order to maintain communication.

Table 15-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a power-on reset (POR) and will allow communication at 9600 baud provided one of the following sets of conditions is met:

- If \$FFFE and \$FFFF do not contain \$FF (programmed state):
  - The external clock is 9.8304 MHz
  - $\overline{\text{IRQ}} = V_{\text{TST}}$
- If \$FFFE and \$FFFF contain \$FF (erased state):
  - The external clock is 9.8304 MHz
  - $\overline{\text{IRQ}} = V_{\text{DD}}$  (this can be implemented through the internal  $\overline{\text{IRQ}}$  pullup)
- If \$FFFE and \$FFFF contain \$FF (erased state):
  - $\overline{\text{IRQ}} = V_{\text{SS}}$  (internal oscillator is selected, no external clock required)

The rising edge of the internal  $\overline{\text{RST}}$  signal latches the monitor mode. Once monitor mode is latched, the values on PTA1 and PTA4 pins can be changed.

## 16.3 Functional Operating Range

Characteristic	Symbol	Value	Unit	Temp Code
Operating temperature range ( $T_L$ to $T_H$ )	$T_A$	−40 to 85 0 to 70	°C	C —
Operating voltage range <sup>(1)</sup> ( $V_{DDMIN}$ to $V_{DDMAX}$ ) −40 to 85°C 0 to 70°C	$V_{DD}$	2.4 to 3.6 2.2 to 3.6	V	C —

1.  $V_{DD}$  must be above  $V_{TRIPR}$  upon power on.

## 16.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 8-pin PDIP 8-pin SOIC 8-pin DFN 16-pin PDIP 16-pin SOIC 16-pin TSSOP	$\theta_{JA}$	105 142 173 76 90 133	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation <sup>(1)</sup>	$P_D$	$P_D = (I_{DD} \times V_{DD})$ $+ P_{I/O} = K/(T_J + 273^\circ\text{C})$	W
Constant <sup>(2)</sup>	K	$P_D \times (T_A + 273^\circ\text{C})$ $+ P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	$T_J$	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	$T_{JM}$	150	°C

1. Power dissipation is a function of temperature.

2. K constant unique to the device. K can be determined for a known  $T_A$  and measured  $P_D$ . With this value of K,  $P_D$  and  $T_J$  can be determined for any value of  $T_A$ .





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MECHANICAL OUTLINES  
DICTIONARY

DOCUMENT NO: 98ASB42431B

PAGE: 648

DO NOT SCALE THIS DRAWING

REV: T

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

DIM	MILLIMETERS		INCHES		DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770					
B	6.35	6.85	0.250	0.270					
C	3.69	4.44	0.145	0.175					
D	0.39	0.53	0.015	0.021					
F	1.02	1.77	0.040	0.070					
G	2.54 BSC		0.100 BSC						
H	1.27 BSC		0.050 BSC						
J	0.21	0.38	0.008	0.015					
K	2.80	3.30	0.110	0.130					
L	7.50	7.74	0.295	0.305					
M	0°	10°	0°	10°					
S	0.51	1.01	0.020	0.040					
TITLE:  16 LD PDIP					CASE NUMBER: 648-08				
					STANDARD: NON-JEDEC				
					PACKAGE CODE: 0006		SHEET: 2 OF 4		



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## MECHANICAL OUTLINES DICTIONARY

DOCUMENT NO: 98ASB42567B

PAGE: 751G

DO NOT SCALE THIS DRAWING

REV: E

### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

TITLE:  
16LD SOIC W/B, 1.27 PITCH,  
CASE OUTLINE

CASE NUMBER: 751G–05

STANDARD: JEDEC MS–013AA

PACKAGE CODE: 2003

SHEET: 2 OF 3