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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2292fbd144-01-5

Table 1. Ordering information *…continued*

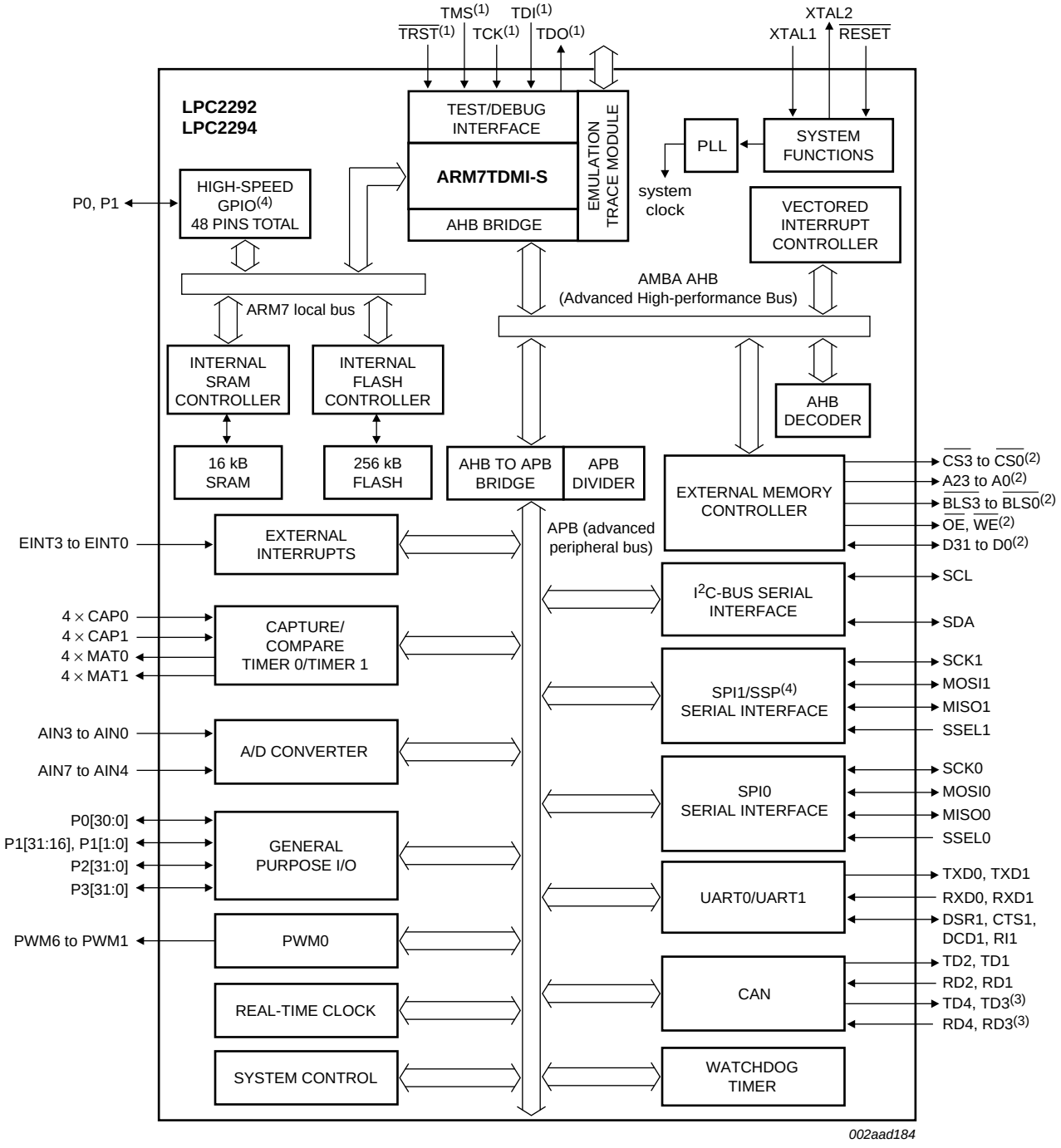
Type number	Package		
	Name	Description	Version
LPC2294HBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/00	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	CAN	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2292FBD144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/00	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2292FET144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/G	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2294HBD144	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/00	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/01	256 kB	16 kB	4 channels	yes	−40 °C to +125 °C

4. Block diagram



(1) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(2) Pins shared with GPIO.

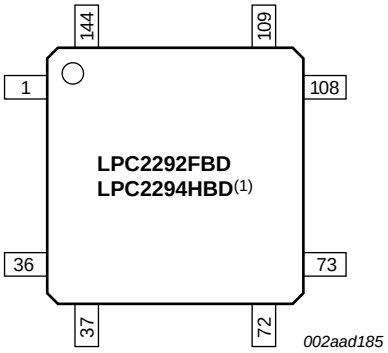
(3) Available in LPC2294 only.

(4) SSP interface and high-speed GPIO are available on LPC2292/2294/01 only.

Fig 1. Block diagram

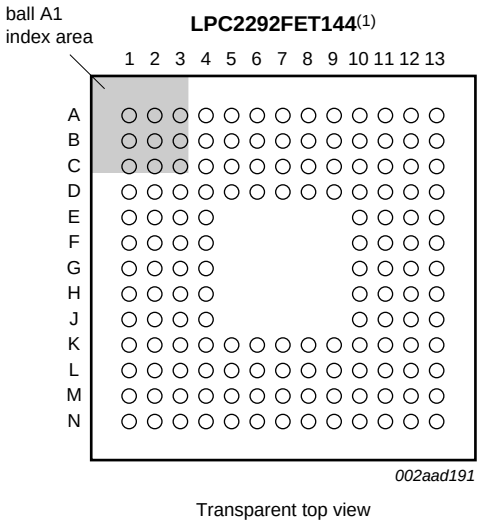
5. Pinning information

5.1 Pinning



(1) Pin configuration is identical for devices with and without /00 and /01 suffixes.

Fig 2. LQFP144 pinning



(1) Pin configuration is identical for devices with and without /00 and /01 suffixes.

Fig 3. TFBGA144 pinning

5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/ PWM1	42[2]	L4[2]	O	**TXD0 —** Transmitter output for UART0.
			O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	49[4]	K6[4]	I	**RXD0 —** Receiver input for UART0.
			O	**PWM3 —** Pulse Width Modulator output 3.
			I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/ CAP0[0]	50[5]	L6[5]	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	58[5]	M8[5]	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
			I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	59[2]	L8[2]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	61[2]	N9[2]	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	68[2]	N11[2]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	69[4]	M11[4]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**PWM2 —** Pulse Width Modulator output 2.
			I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4	75[2]	L12[2]	O	**TXD1 —** Transmitter output for UART1.
			O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	76[4]	L13[4]	I	**RXD1 —** Receiver input for UART1.
			O	**PWM6 —** Pulse Width Modulator output 6.
			I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	78[2]	K11[2]	O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	83[2]	J12[2]	I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[12]/DSR1/ MAT1[0]/RD4	84[2]	J13[2]	I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
			I	**RD4 —** CAN4 receiver input (LPC2294 only).
P0[13]/DTR1/ MAT1[1]/TD4	85[2]	H10[2]	O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
			O	**TD4 —** CAN4 transmitter output (LPC2294 only).
P0[14]/DCD1/ EINT1	92[4]	G10[4]	I	**DCD1 —** Data Carrier Detect input for UART1.
			I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/ EINT2	99[4]	E11[4]	I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0[16]/EINT0/ MAT0[2]/ CAP0[2]	100[4]	E10[4]	I	**EINT0 —** External interrupt 0 input.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	101[2]	D13[2]	I	**CAP1[2] —** Capture input for Timer 1, channel 2.
			I/O	**SCK1 —** Serial Clock for SPI1/SSP[3]. SPI clock output from master or input to slave.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	121[2]	D8[2]	I	**CAP1[3] —** Capture input for Timer 1, channel 3.
			I/O	**MISO1 —** Master In Slave Out for SPI1/SSP[3]. Data input to SPI master or data output from SPI slave.
			O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	122[2]	C8[2]	O	**MAT1[2] —** Match output for Timer 1, channel 2.
			I/O	**MOSI1 —** Master Out Slave In for SPI1/SSP[3]. Data output from SPI master or data input to SPI slave.
			I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	123[4]	B8[4]	O	**MAT1[3] —** Match output for Timer 1, channel 3.
			I	**SSEL1 —** Slave Select for SPI1/SSP[3]. Selects the SPI interface as a slave.
			I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ RD3/CAP1[3]	4[2]	C1[2]	O	**PWM5 —** Pulse Width Modulator output 5.
			I	**RD3 —** CAN3 receiver input (LPC2294 only).
			I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/TD3/ CAP0[0]/ MAT0[0]	5[2]	D4[2]	O	**TD3 —** CAN3 transmitter output (LPC2294 only).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]/RD2	6[2]	D3[2]	I	**RD2 —** CAN2 receiver input.
P0[24]/TD2	8[2]	D1[2]	O	**TD2 —** CAN2 transmitter output.
P0[25]/RD1	21[2]	H1[2]	I	**RD1 —** CAN1 receiver input.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P2[24]/D24	11[7]	E2[7]	I/O	**D24 —** External memory data line 24.
P2[25]/D25	12[7]	E1[7]	I/O	**D25 —** External memory data line 25.
P2[26]/D26/ BOOT0	13[7]	F4[7]	I/O	**D26 —** External memory data line 26.
			I	**BOOT0 —** While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected.
P2[27]/D27/ BOOT1	16[7]	F1[7]	I/O	**D27 —** External memory data line 27.
			I	**BOOT1 —** While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. BOOT1:0 = 00 selects 8-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 01 selects 16-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 10 selects 32-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 11 selects internal flash memory.
P2[28]/D28	17[7]	G2[7]	I/O	**D28 —** External memory data line 28.
P2[29]/D29	18[7]	G1[7]	I/O	**D29 —** External memory data line 29.
P2[30]/D30/ AIN4	19[6]	G3[6]	I/O	**D30 —** External memory data line 30.
			I	**AIN4 —** ADC, input 4. This analog input is always connected to its pin.
P2[31]/D31/ AIN5	20[6]	G4[6]	I/O	**D31 —** External memory data line 31.
			I	**AIN5 —** ADC, input 5. This analog input is always connected to its pin.
P3[0] to P3[31]			I/O	**Port 3 —** Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3[0]/A0	89[7]	G12[7]	O	**A0 —** External memory address line 0.
P3[1]/A1	88[7]	H13[7]	O	**A1 —** External memory address line 1.
P3[2]/A2	87[7]	H12[7]	O	**A2 —** External memory address line 2.
P3[3]/A3	81[7]	J10[7]	O	**A3 —** External memory address line 3.
P3[4]/A4	80[7]	K13[7]	O	**A4 —** External memory address line 4.
P3[5]/A5	74[7]	M13[7]	O	**A5 —** External memory address line 5.
P3[6]/A6	73[7]	N13[7]	O	**A6 —** External memory address line 6.
P3[7]/A7	72[7]	M12[7]	O	**A7 —** External memory address line 7.
P3[8]/A8	71[7]	N12[7]	O	**A8 —** External memory address line 8.
P3[9]/A9	66[7]	M10[7]	O	**A9 —** External memory address line 9.
P3[10]/A10	65[7]	N10[7]	O	**A10 —** External memory address line 10.
P3[11]/A11	64[7]	K9[7]	O	**A11 —** External memory address line 11.
P3[12]/A12	63[7]	L9[7]	O	**A12 —** External memory address line 12.
P3[13]/A13	62[7]	M9[7]	O	**A13 —** External memory address line 13.
P3[14]/A14	56[7]	K7[7]	O	**A14 —** External memory address line 14.
P3[15]/A15	55[7]	L7[7]	O	**A15 —** External memory address line 15.
P3[16]/A16	53[7]	M7[7]	O	**A16 —** External memory address line 16.

Table 5. Interrupt sources *…continued*

Block	Flag(s)	VIC channel #
UART1	RX Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	RX Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI)	
	Auto-baud time-out (ABTO)[1]End of auto-baud (ABEO)[1]	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I2C	SI (state change)	9
SPI0	SPIF, MODF	10
SPI1 and SSP[1]	SPIF, MODF and TXRIS, RXRIS, RTRIS, RORRIS	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
ADC	ADC	18
CAN	1 ORed CAN Acceptance Filter	19
	CAN1/2 Tx	20, 21
	CAN2/3 Tx (LPC2294 only)	22, 23
	reserved	24, 25
	CAN1/2 Rx	26, 27
	CAN3/4 Rx (LPC2294 only)	28,29

[1] SSP interface and UART0/1 auto-baud control are available on LPC2292/2294/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 External memory controller

The external Static Memory Controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8-bit, 16-bit, or 32-bit wide.

6.15.2 Features available in LPC2292/2294/01 only

The LPC2292/2294/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to PCLK / 4. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than 1 / (2PCLK).

6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.18 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2292/2294. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.19 System control

6.19.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2292/2294: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

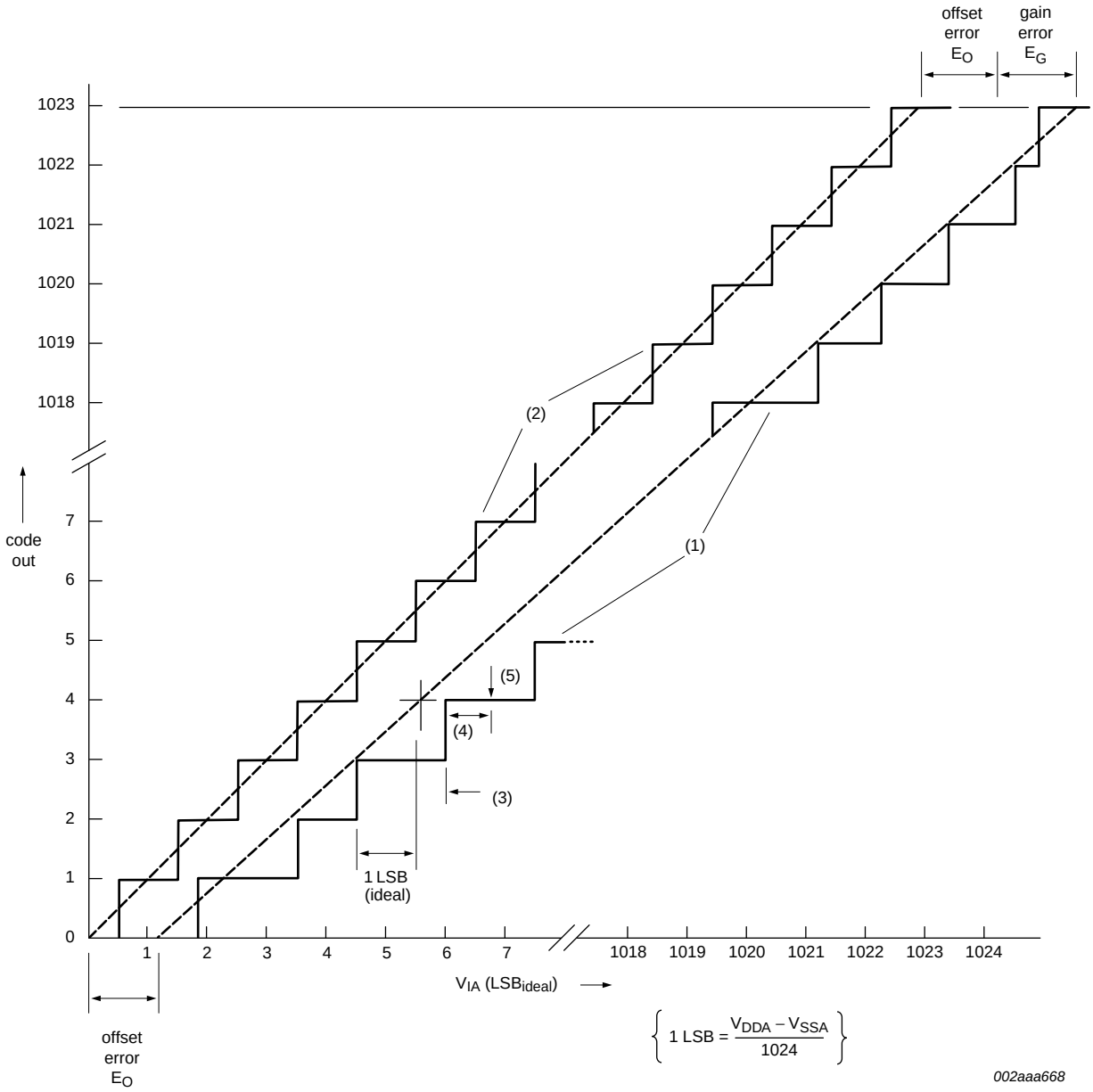
The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

8. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V	[9]	0	0	0	μA



(1) Example of an actual transfer curve.

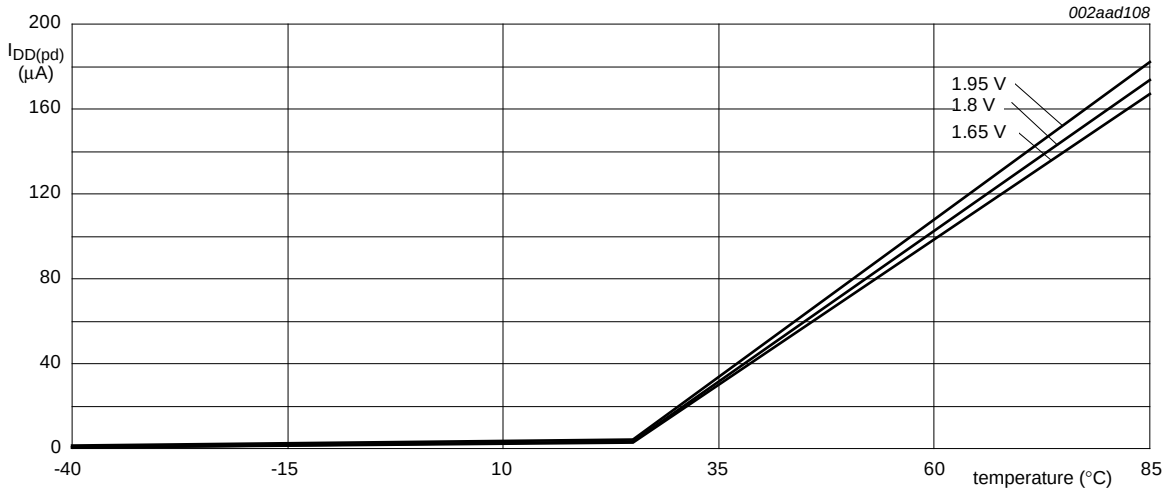
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

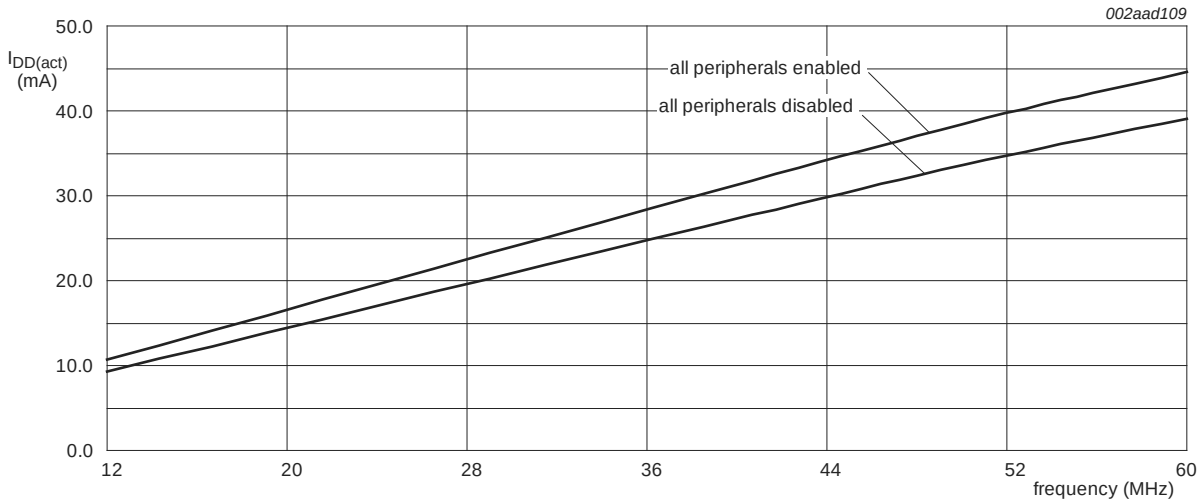
(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics



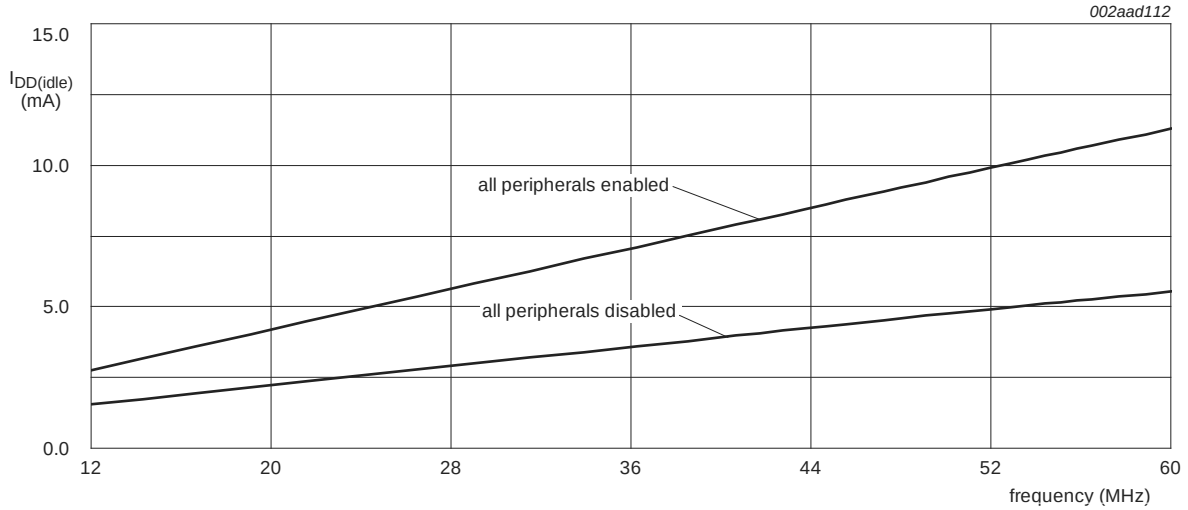
Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 12. Typical LPC2292/01 core power-down current $I_{DD(pd)}$ measured at different temperatures



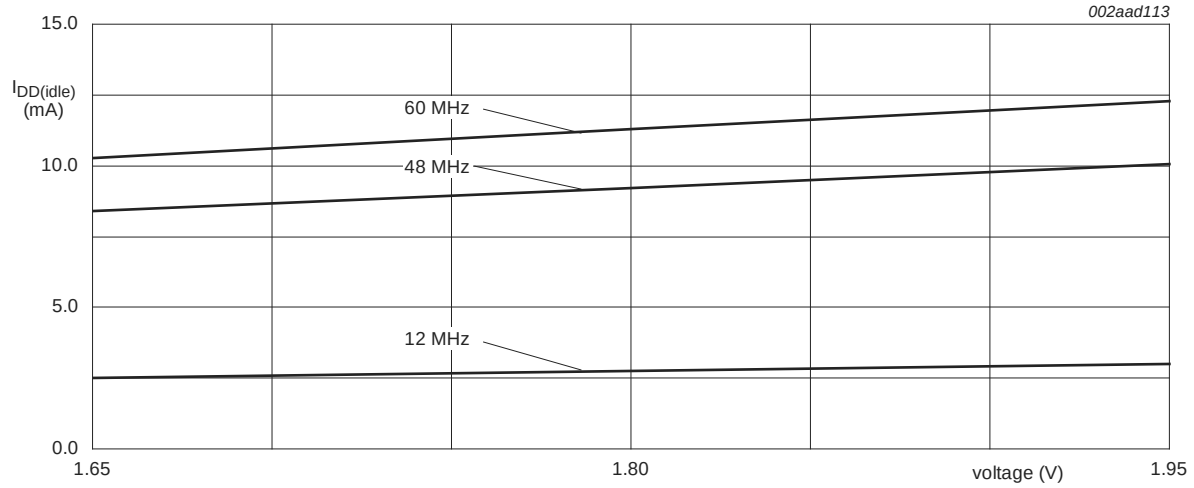
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 13. Typical LPC2294/01 $I_{DD(act)}$ measured at different frequencies



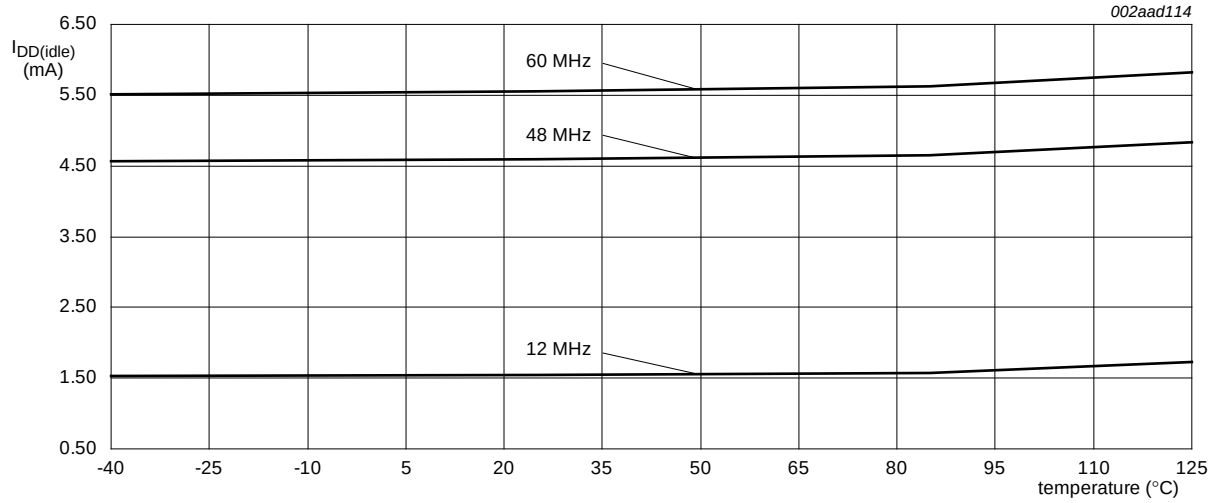
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 16. Typical LPC2294/01 $I_{DD(idle)}$ measured at different frequencies



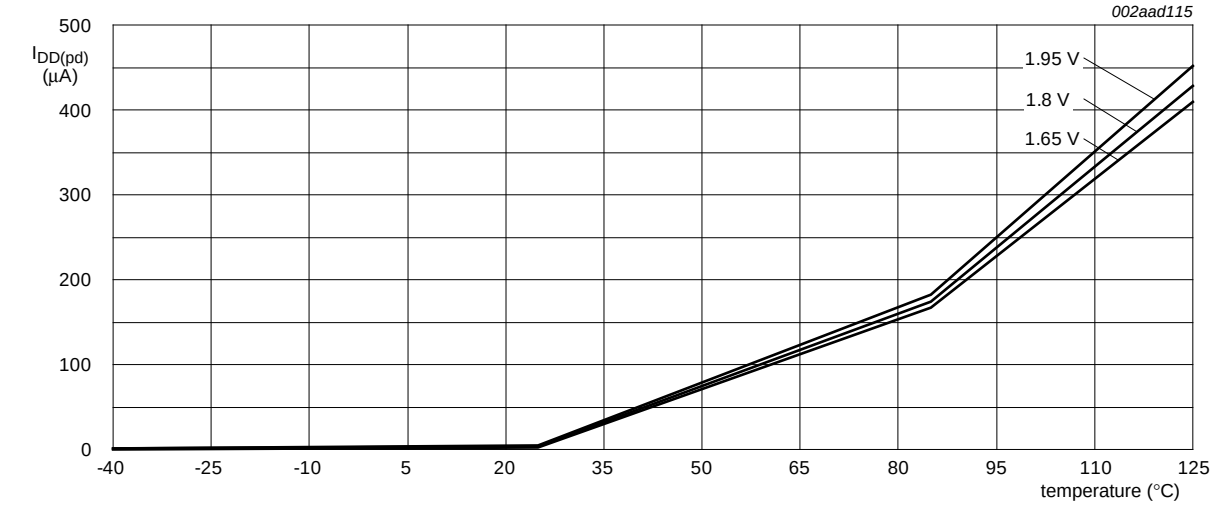
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 17. Typical LPC2294/01 $I_{DD(idle)}$ measured at different core voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 18. Typical LPC2294/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 19. Typical LPC2294/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 9. Typical LPC2292/01 peripheral power consumption in active mode *...continued*
Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
PWM0	103	341	407
I^2C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
PCEMC	306	994	1205
ADC	33	128	167
CAN1/2	229	771	914

Table 10. Typical LPC2294/01 peripheral power consumption in active mode
Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421
PWM0	103	341	407
I^2C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
PCEMC	306	994	1205
ADC	33	128	167
CAN1/2/3/4	230	769	912

9. Dynamic characteristics

Table 11. Dynamic characteristics
T_{amb} = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

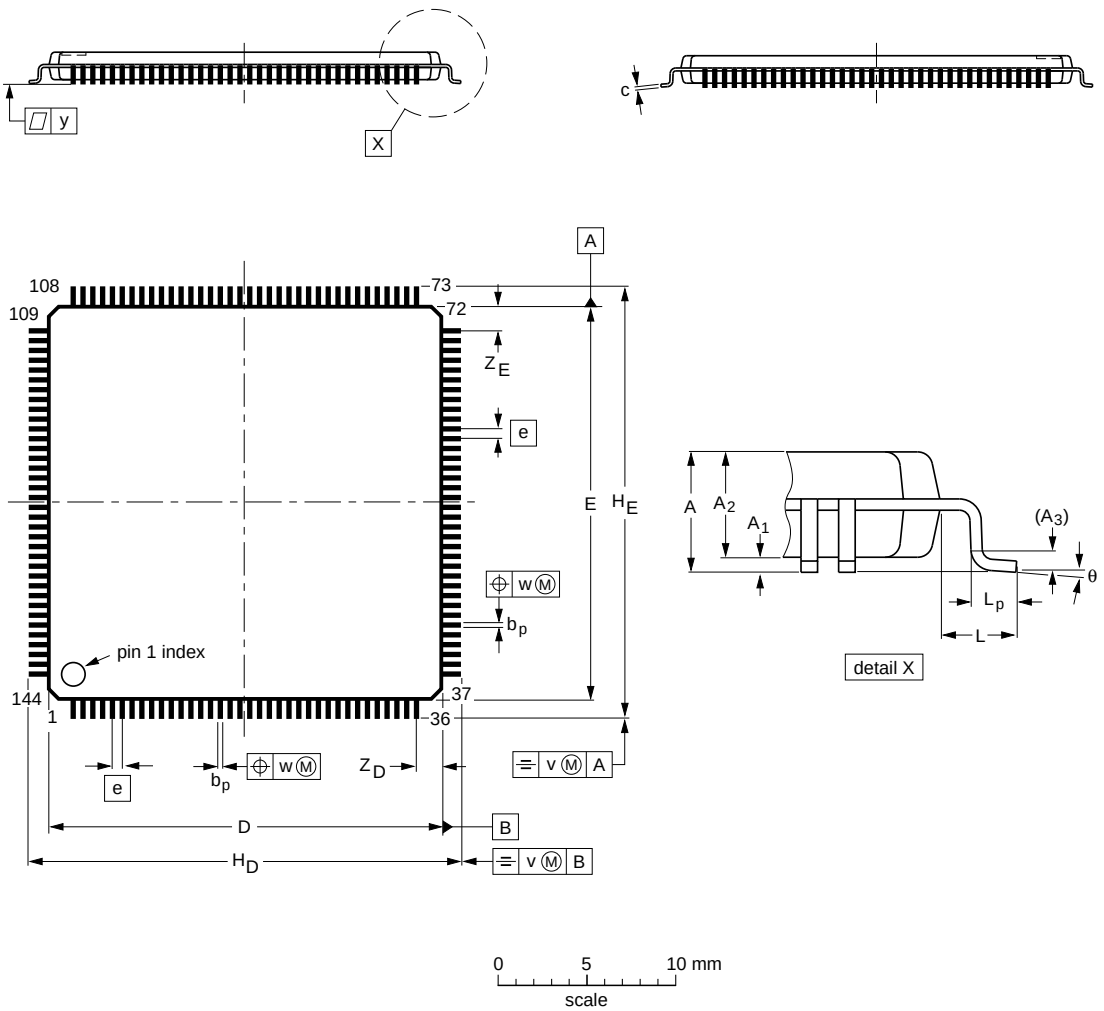
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns

Table 12. External memory interface dynamic characteristics
C_L = 25 pF; T_{amb} = 40 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles						
t_{CHAV}	XCLK HIGH to address valid time		-	-	10	ns
t_{CHCSL}	XCLK HIGH to $\overline{CS}$ LOW time		-	-	10	ns
t_{CHCSH}	XCLK HIGH to $\overline{CS}$ HIGH time		-	-	10	ns
t_{CHANV}	XCLK HIGH to address invalid time		-	-	10	ns
Read cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	[1]	−5	-	+10	ns
t_{OELAV}	$\overline{OE}$ LOW to address valid time	[1]	−5	-	+10	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		−5	-	+5	ns
t_{am}	memory access time	[2][3]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(ibr)}$	memory access time (initial burst-ROM)	[2][3]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(sbr)}$	memory access time (subsequent burst-ROM)	[2][4]	$T_{cy(CCLK)} + (-20)$	-	-	ns
$t_{h(D)}$	data input hold time	[5]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		−5	-	+5	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		−5	-	+5	ns
t_{CHOEL}	XCLK HIGH to $\overline{OE}$ LOW time		−5	-	+5	ns
t_{CHOEH}	XCLK HIGH to $\overline{OE}$ HIGH time		−5	-	+5	ns
Write cycle parameters						
t_{AVCSL}	address valid to $\overline{CS}$ LOW time	[1]	$T_{cy(CCLK)} - 10$	-	-	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		−5	-	+5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		−5	-	+5	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		−5	-	+5	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		−5	-	+5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		−5	-	+5	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[2]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[2]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns

10. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

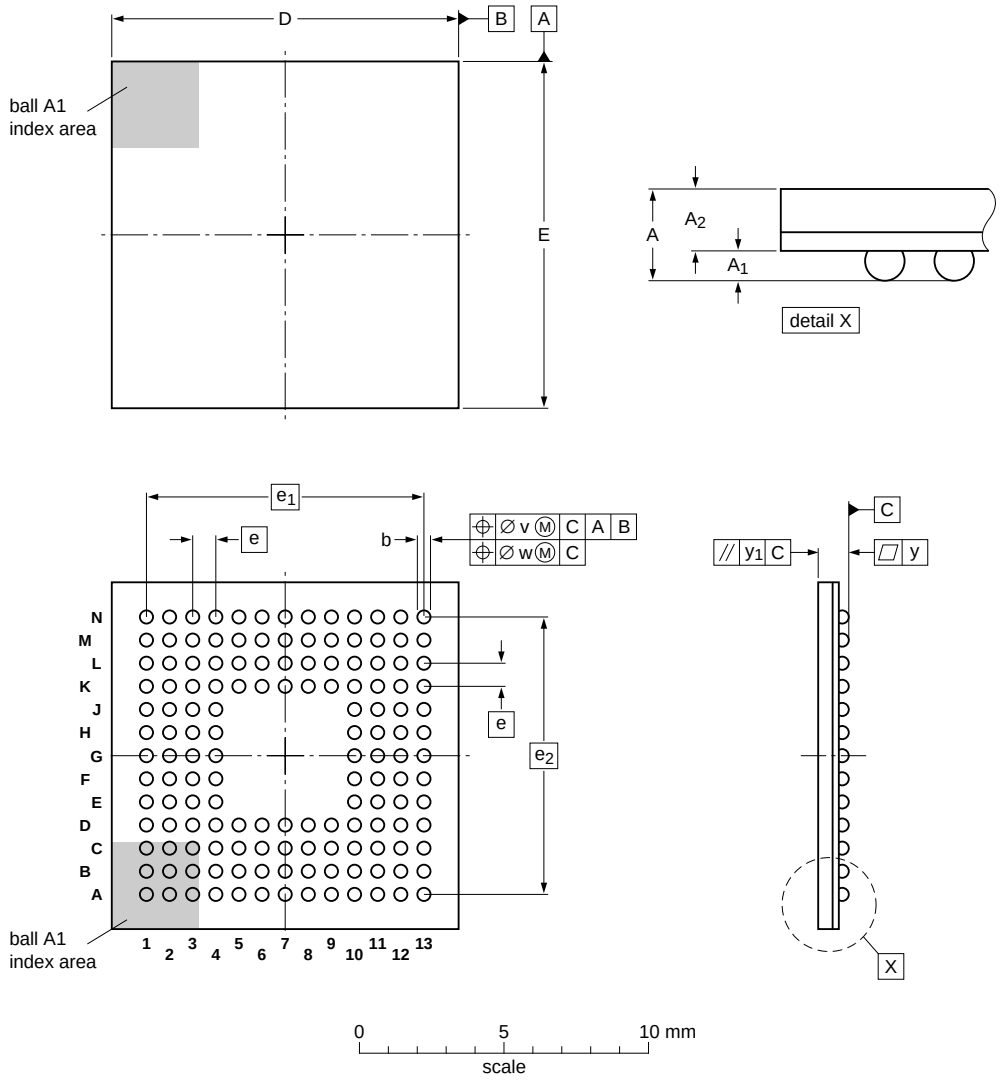
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 25. Package outline SOT486-1 (LQFP144)

TFBGA144: plastic thin fine-pitch ball grid array package; 144 balls **SOT569-2**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	9.6	9.6	0.15	0.05	0.1	0.08
	nom	1.05	0.35	0.70	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT569-2						~~08-01-29~~ 08-03-14

Fig 26. Package outline SOT569-2 (TFBGA144)

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