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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2292fbd144-551

- 16 kB on-chip static RAM and 256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip bootloader software. Single flash sector or full chip erase in 400 ms and programming of 256 B in 1 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software as well as high-speed real-time tracing of instruction execution.
- Two/four (LPC2292/2294) interconnected CAN interfaces with advanced acceptance filters. Additional serial interfaces include two UARTs (16C550), Fast I^2C-bus (400 kbit/s) and two SPIs.
- Eight channel 10-bit ADC with conversion time as low as 2.44 μs.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC), and watchdog.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 112 general purpose I/O pins (5 V tolerant). Up to nine edge/level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2292FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2292FET144/00	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/01	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC2294HBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/00	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

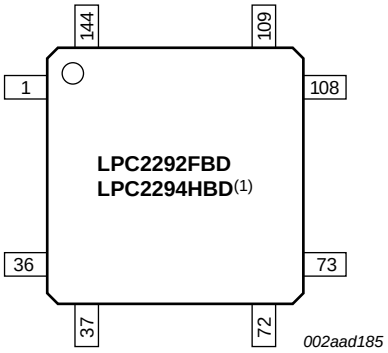
3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	CAN	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2292FBD144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/00	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2292FET144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/G	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2294HBD144	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/00	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/01	256 kB	16 kB	4 channels	yes	−40 °C to +125 °C

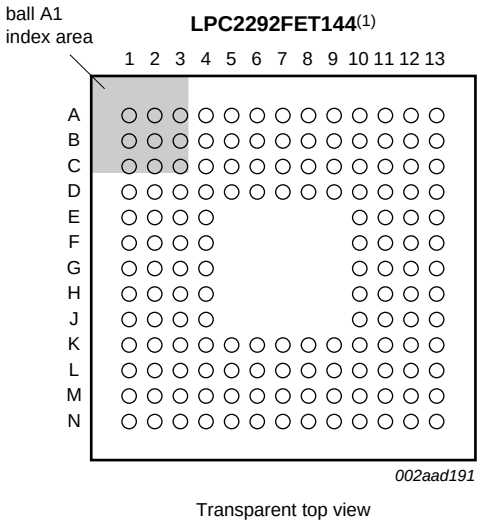
5. Pinning information

5.1 Pinning



(1) Pin configuration is identical for devices with and without /00 and /01 suffixes.

Fig 2. LQFP144 pinning



(1) Pin configuration is identical for devices with and without /00 and /01 suffixes.

Fig 3. TFBGA144 pinning

Table 3. Ball allocation

Row	Column												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2[22]/ D22	$V_{DDA(1V8)}$	P1[28]/ TDI	P2[21]/ D21	P2[18]/ D18	P2[14]/ D14	P1[29]/ TCK	P2[11]/ D11	P2[10]/ D10	P2[7]/D7	$V_{DD(3V3)}$	$V_{DD(1V8)}$	P2[4]/D4
B	$V_{DD(3V3)}$	P1[27]/ TDO	XTAL2	$V_{SSA(PLL)}$	P2[19]/ D19	P2[15]/ D15	P2[12]/ D12	P0[20]/ MAT1[3]/ SSEL1/ EINT3	$V_{DD(3V3)}$	P2[6]/D6	V_{SS}	P2[3]/D3	V_{SS}
C	P0[21]/ PWM5/ CAP1[3]	V_{SS}	XTAL1	V_{SSA}	$\overline{\text{RESET}}$	P2[16]/ D16	P2[13]/ D13	P0[19]/ MAT1[2]/ MOSI1/ CAP1[2]	P2[9]/D9	P2[5]/D5	P2[2]/D2	P2[1]/D1	$V_{DD(3V3)}$
D	P0[24]/ TD2	P1[19]/ TRACE PKT3	P0[23]/ RD2	P0[22]/ CAP0[0]/ MAT0[0]	P2[20]/ D20	P2[17]/ D17	V_{SS}	P0[18]/ CAP1[3]/ MISO1/ MAT1[3]	P2[8]/D8	P1[30]/ TMS	V_{SS}	P1[20]/ TRACE SYNC	P0[17]/ CAP1[2]/ SCK1/ MAT1[2]
E	P2[25]/ D25	P2[24]/ D24	P2[23]	V_{SS}						P0[16]/ EINT0/ MAT0[2]/ CAP0[2]	P0[15]/ RI1/ EINT2	P2[0]/D0	P3[30]/ BLS1
F	P2[27]/ D27/ BOOT1	P1[18]/ TRACE PKT2	$V_{DDA(3V3)}$	P2[26]/ D26/ BOOT0						P3[31]/ BLS0	P1[21]/ PIPE STAT0	$V_{DD(3V3)}$	V_{SS}
G	P2[29]/ D29	P2[28]/ D28	P2[30]/ D30/AIN4	P2[31]/ D31/AIN5						P0[14]/ DCD1/ EINT1	P1[0]/$\overline{\text{CS0}}$	P3[0]/A0	P1[1]/$\overline{\text{OE}}$
H	P0[25]/ RD1	TD1	P0[27]/ AIN0/ CAP0[1]/ MAT0[1]	P1[17]/ TRACE PKT1						P0[13]/ DTR1/ MAT1[1]	P1[22]/ PIPE STAT1	P3[2]/A2	P3[1]/A1
J	P0[28]/ AIN1/ CAP0[2]/ MAT0[2]	V_{SS}	P3[29]/ BLS2/ AIN6	P3[28]/ BLS3/ AIN7						P3[3]/A3	P1[23]/ PIPE STAT2	P0[11]/ CTS1/ CAP1[1]	P0[12]/ DSR1/ MAT1[0]
K	P3[27]/ WE	P3[26]/ CS1	$V_{DD(3V3)}$	P3[22]/ A22	P3[20]/ A20	P0[1]/ RXD0/ PWM3/ EINT0	P3[14]/ A14	P1[25]/ EXTIN0	P3[11]/ A11	$V_{DD(3V3)}$	P0[10]/ RTS1/ CAP1[0]	V_{SS}	P3[4]/A4

Table 3. Ball allocation *…continued*

Row	Column												
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
L	P0[29]/ AIN2/ CAP0[3]/ MAT0[3]	P0[30]/ AIN3/ EINT3/ CAP0[0]	P1[16]/ TRACE PKT0	P0[0]/ TXD0/ PWM1	P3[19]/ A19	P0[2]/ SCL/ CAP0[0]	P3[15]/ A15	P0[4]/ SCK0/ CAP0[1]	P3[12]/ A12	V_{SS}	P1[24]/ TRACE CLK	P0[8]/ TXD1/ PWM4	P0[9]/ RXD1/ PWM6/ EINT3
M	P3[25]/ CS2	P3[24]/ CS3	$V_{DD(3V3)}$	P1[31]/ TRST	P3[18]/ A18	$V_{DD(3V3)}$	P3[16]/ A16	P0[3]/ SDA/ MAT0[0]/ EINT1	P3[13]/ A13	P3[9]/A9	P0[7]/ SSEL0/ PWM2/ EINT2	P3[7]/A7	P3[5]/A5
N	$V_{DD(1V8)}$	V_{SS}	P3[23]/ A23/ XCLK	P3[21]/ A21	P3[17]/ A17	P1[26]/ RTCK	V_{SS}	$V_{DD(3V3)}$	P0[5]/ MISO0/ MAT0[1]	P3[10]/ A10	P0[6]/ MOSI0/ CAP0[2]	P3[8]/A8	P3[6]/A6

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[12]/DSR1/ MAT1[0]/RD4	84[2]	J13[2]	I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
			I	**RD4 —** CAN4 receiver input (LPC2294 only).
P0[13]/DTR1/ MAT1[1]/TD4	85[2]	H10[2]	O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
			O	**TD4 —** CAN4 transmitter output (LPC2294 only).
P0[14]/DCD1/ EINT1	92[4]	G10[4]	I	**DCD1 —** Data Carrier Detect input for UART1.
			I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/ EINT2	99[4]	E11[4]	I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0[16]/EINT0/ MAT0[2]/ CAP0[2]	100[4]	E10[4]	I	**EINT0 —** External interrupt 0 input.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	101[2]	D13[2]	I	**CAP1[2] —** Capture input for Timer 1, channel 2.
			I/O	**SCK1 —** Serial Clock for SPI1/SSP[3]. SPI clock output from master or input to slave.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	121[2]	D8[2]	I	**CAP1[3] —** Capture input for Timer 1, channel 3.
			I/O	**MISO1 —** Master In Slave Out for SPI1/SSP[3]. Data input to SPI master or data output from SPI slave.
			O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	122[2]	C8[2]	O	**MAT1[2] —** Match output for Timer 1, channel 2.
			I/O	**MOSI1 —** Master Out Slave In for SPI1/SSP[3]. Data output from SPI master or data input to SPI slave.
			I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	123[4]	B8[4]	O	**MAT1[3] —** Match output for Timer 1, channel 3.
			I	**SSEL1 —** Slave Select for SPI1/SSP[3]. Selects the SPI interface as a slave.
			I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ RD3/CAP1[3]	4[2]	C1[2]	O	**PWM5 —** Pulse Width Modulator output 5.
			I	**RD3 —** CAN3 receiver input (LPC2294 only).
			I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/TD3/ CAP0[0]/ MAT0[0]	5[2]	D4[2]	O	**TD3 —** CAN3 transmitter output (LPC2294 only).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]/RD2	6[2]	D3[2]	I	**RD2 —** CAN2 receiver input.
P0[24]/TD2	8[2]	D1[2]	O	**TD2 —** CAN2 transmitter output.
P0[25]/RD1	21[2]	H1[2]	I	**RD1 —** CAN1 receiver input.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[27]/AIN0/ CAP0[1]/ MAT0[1]	23[6]	H3[6]	I	**AIN0 —** ADC, input 0. This analog input is always connected to its pin.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[28]/AIN1/ CAP0[2]/ MAT0[2]	25[6]	J1[6]	I	**AIN1 —** ADC, input 1. This analog input is always connected to its pin.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AIN2/ CAP0[3]/ MAT0[3]	32[6]	L1[6]	I	**AIN2 —** ADC, input 2. This analog input is always connected to its pin.
			I	**CAP0[3] —** Capture input for Timer 0, Channel 3.
			O	**MAT0[3] —** Match output for Timer 0, channel 3.
P0[30]/AIN3/ EINT3/CAP0[0]	33[6]	L2[6]	I	**AIN3 —** ADC, input 3. This analog input is always connected to its pin.
			I	**EINT3 —** External interrupt 3 input.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available.
P1[0]/$\overline{\text{CS0}}$	91[7]	G11[7]	O	**$\overline{\text{CS0}}$ —** LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1[1]/$\overline{\text{OE}}$	90[7]	G13[7]	O	**$\overline{\text{OE}}$ —** LOW-active Output Enable signal.
P1[16]/ TRACEPKT0	34[7]	L3[7]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/ TRACEPKT1	24[7]	H4[7]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/ TRACEPKT2	15[7]	F2[7]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/ TRACEPKT3	7[7]	D2[7]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/ TRACESYNC	102[7]	D12[7]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/ PIPESTAT0	95[7]	F11[7]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/ PIPESTAT1	86[7]	H11[7]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/ PIPESTAT2	82[7]	J11[7]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/ TRACECLK	70[7]	L11[7]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P1[25]/EXTIN0	60[7]	K8[7]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	52[7]	N6[7]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	144[7]	B2[7]	O	**TDO —** Test Data out for JTAG interface.
P1[28]/TDI	140[7]	A3[7]	I	**TDI —** Test Data in for JTAG interface.
P1[29]/TCK	126[7]	A7[7]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	113[7]	D10[7]	I	**TMS —** Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	43[7]	M4[7]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
P2[0] to P2[31]			I/O	**Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2[0]/D0	98[7]	E12[7]	I/O	**D0 —** External memory data line 0.
P2[1]/D1	105[7]	C12[7]	I/O	**D1 —** External memory data line 1.
P2[2]/D2	106[7]	C11[7]	I/O	**D2 —** External memory data line 2.
P2[3]/D3	108[7]	B12[7]	I/O	**D3 —** External memory data line 3.
P2[4]/D4	109[7]	A13[7]	I/O	**D4 —** External memory data line 4.
P2[5]/D5	114[7]	C10[7]	I/O	**D5 —** External memory data line 5.
P2[6]/D6	115[7]	B10[7]	I/O	**D6 —** External memory data line 6.
P2[7]/D7	116[7]	A10[7]	I/O	**D7 —** External memory data line 7.
P2[8]/D8	117[7]	D9[7]	I/O	**D8 —** External memory data line 8.
P2[9]/D9	118[7]	C9[7]	I/O	**D9 —** External memory data line 9.
P2[10]/D10	120[7]	A9[7]	I/O	**D10 —** External memory data line 10.
P2[11]/D11	124[7]	A8[7]	I/O	**D11 —** External memory data line 11.
P2[12]/D12	125[7]	B7[7]	I/O	**D12 —** External memory data line 12.
P2[13]/D13	127[7]	C7[7]	I/O	**D13 —** External memory data line 13.
P2[14]/D14	129[7]	A6[7]	I/O	**D14 —** External memory data line 14.
P2[15]/D15	130[7]	B6[7]	I/O	**D15 —** External memory data line 15.
P2[16]/D16	131[7]	C6[7]	I/O	**D16 —** External memory data line 16.
P2[17]/D17	132[7]	D6[7]	I/O	**D17 —** External memory data line 17.
P2[18]/D18	133[7]	A5[7]	I/O	**D18 —** External memory data line 18.
P2[19]/D19	134[7]	B5[7]	I/O	**D19 —** External memory data line 19.
P2[20]/D20	136[7]	D5[7]	I/O	**D20 —** External memory data line 20.
P2[21]/D21	137[7]	A4[7]	I/O	**D21 —** External memory data line 21.
P2[22]/D22	1[7]	A1[7]	I/O	**D22 —** External memory data line 22.
P2[23]/D23	10[7]	E3[7]	I/O	**D23 —** External memory data line 23.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P2[24]/D24	11[7]	E2[7]	I/O	**D24 —** External memory data line 24.
P2[25]/D25	12[7]	E1[7]	I/O	**D25 —** External memory data line 25.
P2[26]/D26/ BOOT0	13[7]	F4[7]	I/O	**D26 —** External memory data line 26.
			I	**BOOT0 —** While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected.
P2[27]/D27/ BOOT1	16[7]	F1[7]	I/O	**D27 —** External memory data line 27.
			I	**BOOT1 —** While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. BOOT1:0 = 00 selects 8-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 01 selects 16-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 10 selects 32-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 11 selects internal flash memory.
P2[28]/D28	17[7]	G2[7]	I/O	**D28 —** External memory data line 28.
P2[29]/D29	18[7]	G1[7]	I/O	**D29 —** External memory data line 29.
P2[30]/D30/ AIN4	19[6]	G3[6]	I/O	**D30 —** External memory data line 30.
			I	**AIN4 —** ADC, input 4. This analog input is always connected to its pin.
P2[31]/D31/ AIN5	20[6]	G4[6]	I/O	**D31 —** External memory data line 31.
			I	**AIN5 —** ADC, input 5. This analog input is always connected to its pin.
P3[0] to P3[31]			I/O	**Port 3 —** Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3[0]/A0	89[7]	G12[7]	O	**A0 —** External memory address line 0.
P3[1]/A1	88[7]	H13[7]	O	**A1 —** External memory address line 1.
P3[2]/A2	87[7]	H12[7]	O	**A2 —** External memory address line 2.
P3[3]/A3	81[7]	J10[7]	O	**A3 —** External memory address line 3.
P3[4]/A4	80[7]	K13[7]	O	**A4 —** External memory address line 4.
P3[5]/A5	74[7]	M13[7]	O	**A5 —** External memory address line 5.
P3[6]/A6	73[7]	N13[7]	O	**A6 —** External memory address line 6.
P3[7]/A7	72[7]	M12[7]	O	**A7 —** External memory address line 7.
P3[8]/A8	71[7]	N12[7]	O	**A8 —** External memory address line 8.
P3[9]/A9	66[7]	M10[7]	O	**A9 —** External memory address line 9.
P3[10]/A10	65[7]	N10[7]	O	**A10 —** External memory address line 10.
P3[11]/A11	64[7]	K9[7]	O	**A11 —** External memory address line 11.
P3[12]/A12	63[7]	L9[7]	O	**A12 —** External memory address line 12.
P3[13]/A13	62[7]	M9[7]	O	**A13 —** External memory address line 13.
P3[14]/A14	56[7]	K7[7]	O	**A14 —** External memory address line 14.
P3[15]/A15	55[7]	L7[7]	O	**A15 —** External memory address line 15.
P3[16]/A16	53[7]	M7[7]	O	**A16 —** External memory address line 16.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set
- A 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2292/2294 incorporate a 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the on-chip bootloader is used, 248 kB of flash memory is available for user code.

The LPC2292/2294 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.64) provides Code Read Protection (CRP) for the LPC2292/2294 on-chip flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip RAM or flash memory are disabled. However, the ISP flash erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

6.10 CAN controllers and acceptance filter

The LPC2292/2294 each contain two/four CAN controllers. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

6.10.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit RX identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.

6.11 UARTs

The LPC2292/2294 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

6.11.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.11.2 UART features available in LPC2292/2294/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2292/2294/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.12 I^2C-bus serial I/O controller

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or

8. Static characteristics

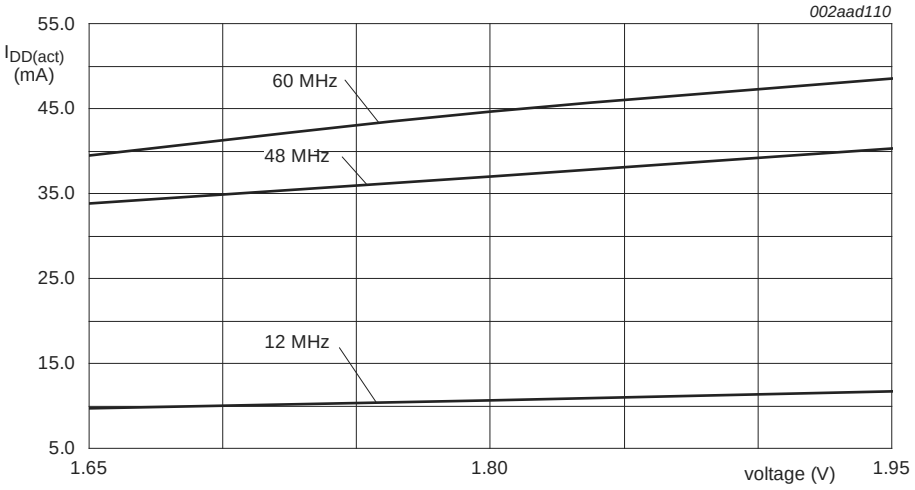
Table 7. Static characteristics

T_{amb} = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V	[9]	0	0	0	μA

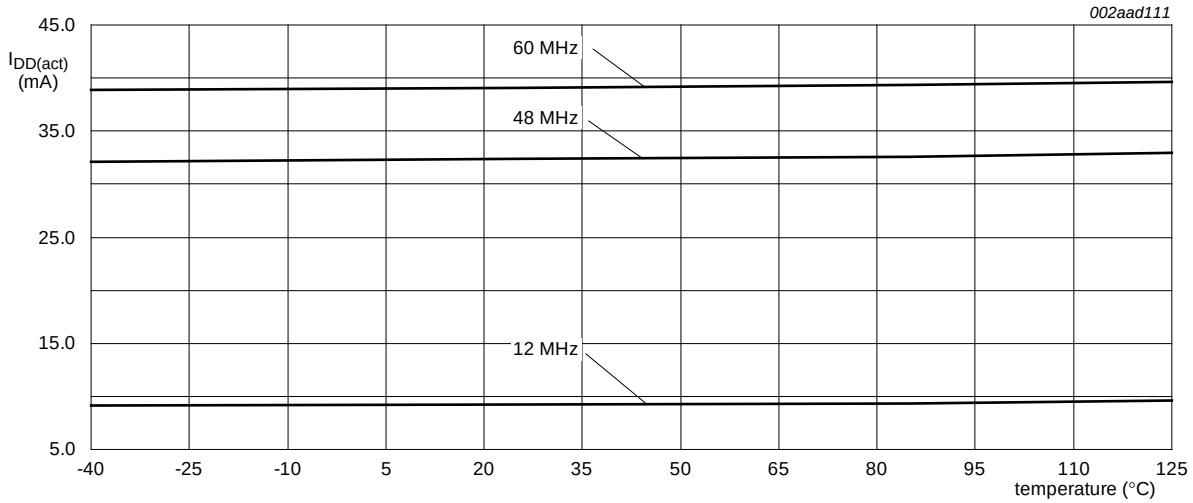
Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Power consumption LPC2292, LPC2292/00, LPC2294, LPC2294/00							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	50	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 125 °C		-	300	1000	µA
Power consumption LPC2292/01 and LPC2294/01							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	45	-	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	11.5	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 125 °C		-	300	1000	µA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	µA
		V_I = 5 V		-	10	22	µA



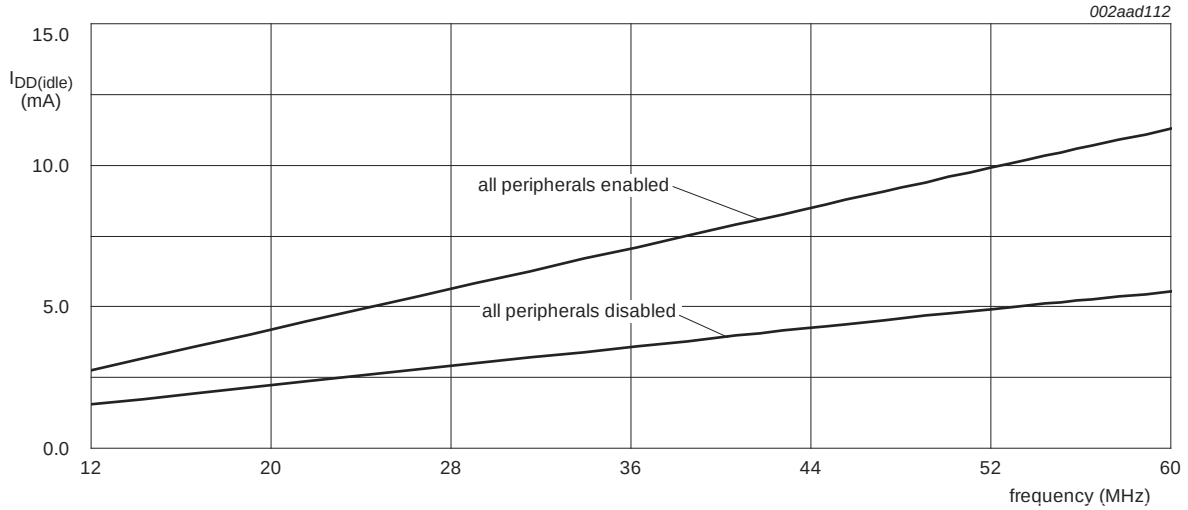
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 14. Typical LPC2294/01 $I_{DD(act)}$ measured at different core voltages



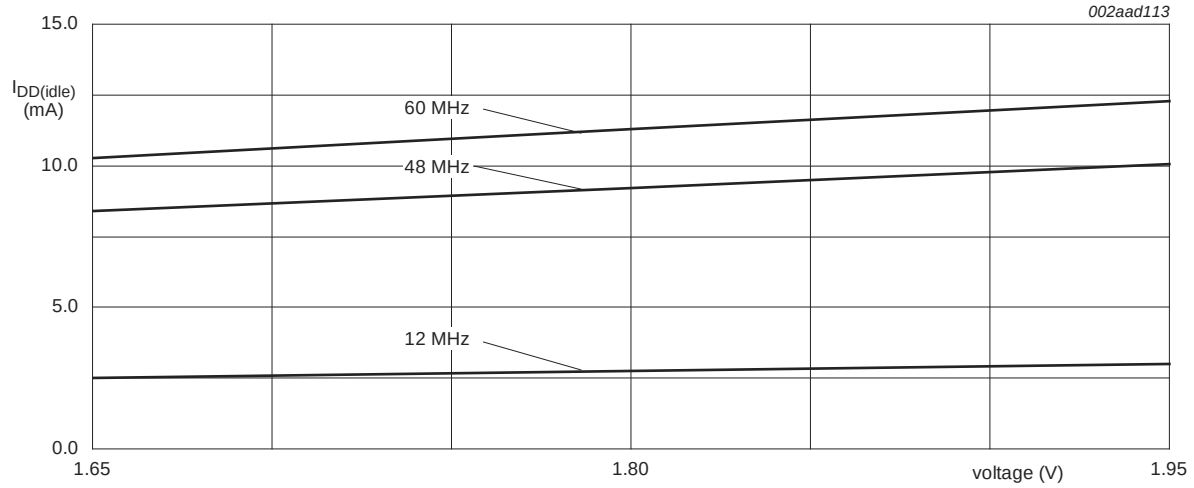
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
core voltage 1.8 V; all peripherals disabled.

Fig 15. Typical LPC2294/01 $I_{DD(act)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 16. Typical LPC2294/01 $I_{DD(idle)}$ measured at different frequencies



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 17. Typical LPC2294/01 $I_{DD(idle)}$ measured at different core voltages

Table 11. Dynamic characteristics *...continued*
T_{amb} = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

Table 12. External memory interface dynamic characteristics *…continued*
C_L = 25 pF, T_{amb} = 40 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
t_{CHDV}	XCLK HIGH to data valid time			-	-	10	ns
t_{CHWEL}	XCLK HIGH to $\overline{WE}$ LOW time			-	-	10	ns
t_{CHBLSL}	XCLK HIGH to $\overline{BLS}$ LOW time			-	-	10	ns
t_{CHWEH}	XCLK HIGH to $\overline{WE}$ HIGH time			-	-	10	ns
t_{CHBLSH}	XCLK HIGH to $\overline{BLS}$ HIGH time			-	-	10	ns
t_{CHDNV}	XCLK HIGH to data invalid time			-	-	10	ns

[1] Except on initial access, in which case the address is set up $T_{cy(CCLK)}$ earlier.

[2] $T_{cy(CCLK)} = 1/_{CCLK}$.

[3] Latest of address valid, $\overline{CS}$ LOW, $\overline{OE}$ LOW to data valid.

[4] Address valid to data valid.

[5] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

Table 13. Standard read access specifications

Access cycle	Max frequency	WST[1] setting WST ≥ 0; round up to integer	Memory access time requirement
standard read	$f_{MAX} \leq \frac{2 + WST1}{t_{RAM} + 20\ ns}$	$WST1 \geq \frac{t_{RAM} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{RAM} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
standard write	$f_{MAX} \leq \frac{1 + WST2}{t_{WRITE} + 5\ ns}$	$WST2 \geq \frac{t_{WRITE} - t_{CYC} + 5}{t_{cy(CCLK)}}$	$t_{WRITE} \leq t_{cy(CCLK)} \times (1 + WST2) - 5\ ns$
burst read - initial	$f_{MAX} \leq \frac{2 + WST1}{t_{INIT} + 20\ ns}$	$WST1 \geq \frac{t_{INIT} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{INIT} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
burst read - subsequent 3×	$f_{MAX} \leq \frac{1}{t_{ROM} + 20\ ns}$	N/A	$t_{ROM} \leq t_{cy(CCLK)} - 20\ ns$

[1] See the *LPC2119/2129/2194/2292/2294 User Manual* for a description of the WSTn bits.

9.1 Timing

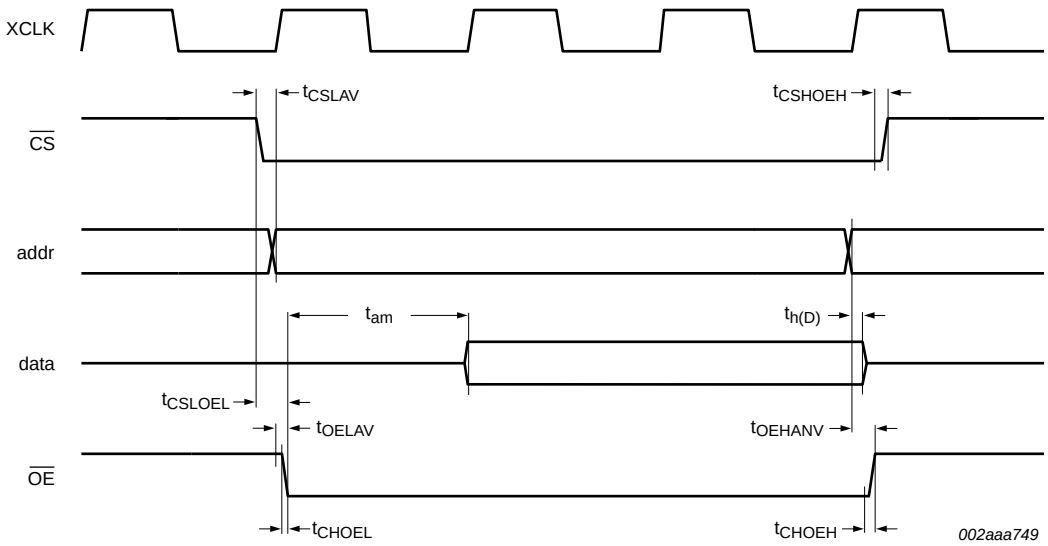


Fig 22. External memory read access

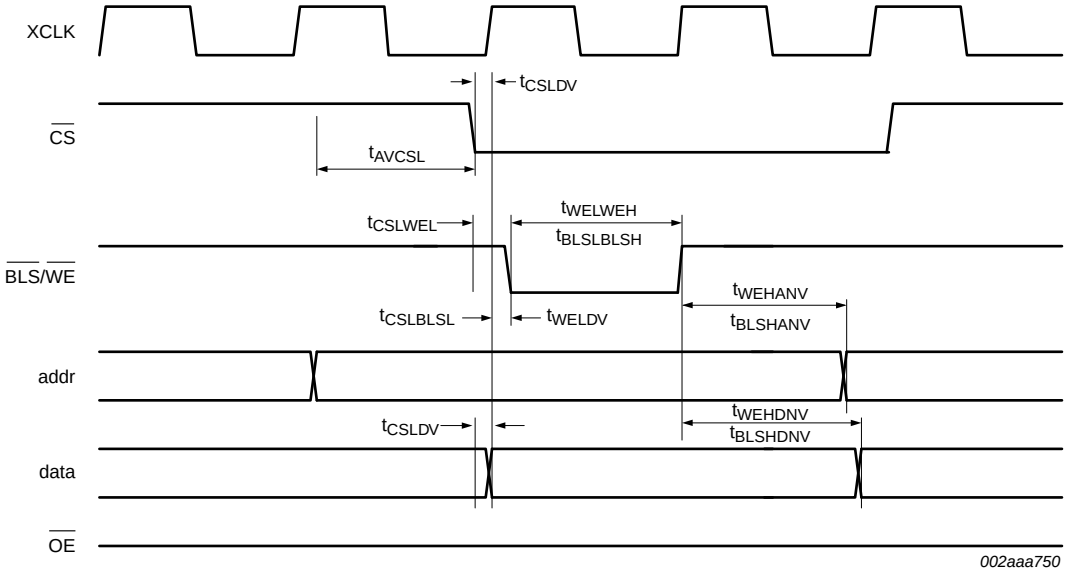
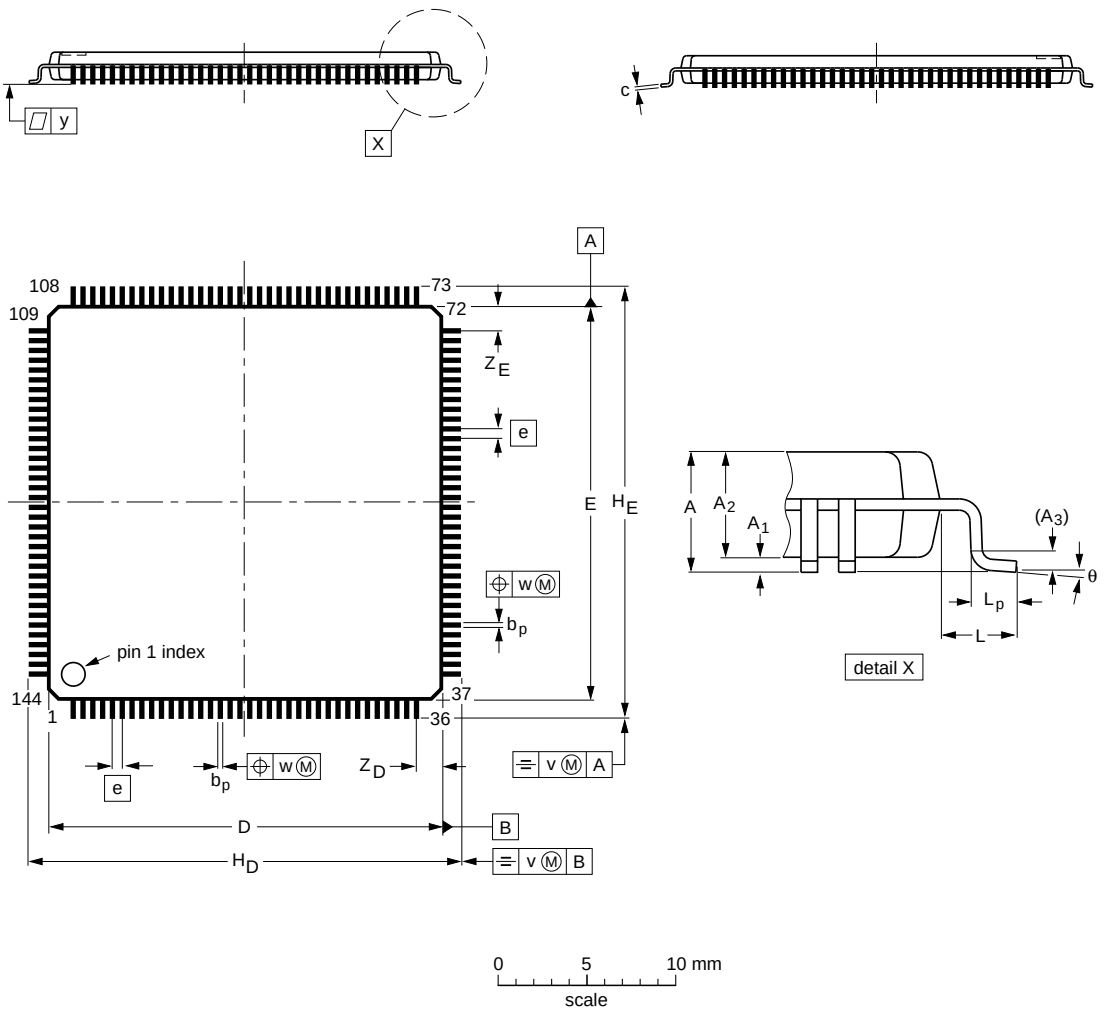


Fig 23. External memory write access

10. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 25. Package outline SOT486-1 (LQFP144)

12. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2292_2294 v.8	20110608	Product data sheet	201004021F	LPC2292_2294 v.7
Modifications:	• Table 7 “Static characteristics”; Changed /01 Power-down mode supply current ($I_{DD(pd)}$) from 180 μA to 500 μA for industrial temperature range, and 430 μA to 1000 μA for extended temperature range. • Table 7 “Static characteristics”; Changed I^2C pad hysteresis from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$.			
LPC2292_2294 v.7	20081204	Product data sheet	-	LPC2292_2294_6
Modifications:	• Figure 1 “Block diagram”: corrected high-speed GPIO ports 48 pins; P0/P1 only. • Figure 24 “External clock timing (with an amplitude of at least Vi(RMS) = 200 mV)”: removed figure note row “V_{DD} = 1.8 V”, updated graphic. • Table 4 “Pin description”: pad descriptions corrected for pins P2[30], P2[31], P3[28], P3[30], P3[31]. • Table 5 “Interrupt sources”: CAN and UART0/1 interrupt sources corrected. • Table 7 “Static characteristics”: V_{hys}, moved 0.4 from Typ to Min column. • Maximum frequency f_{osc} for external oscillator and external crystal updated. • Changed SOT569-1 to SOT569-2. • Added overbar to indicate LOW-active for $\overline{BLSn}$, $\overline{CSn}$, $\overline{OE}$, and $\overline{WE}$			
LPC2292_2294 v.6	20071210	Product data sheet	-	LPC2292_2294_5
Modifications:	• Type number LPC2292FBD144/01 has been added. • Type number LPC2292FET144/01 has been added. • Type number LPC2294HBD144/01 has been added. • Details introduced with /01 devices on new peripherals/features (Fast I/O ports, SSP, CRP) and enhancements to existing ones (UART0/1, Timers, ADC, and SPI) added. • Power consumption measurements for LPC2292/2294/01 added. • Description of JTAG pin TCK has been updated.			
LPC2292_2294 v.5	20070215	Product data sheet	-	LPC2292_2294 v.4
LPC2292_2294 v.4	20060711	Product data sheet	-	LPC2292_2294 v.3
LPC2292_2294 v.3	20051101	Product data sheet	-	LPC2292_2294 v.2
LPC2292_2294 v.2	20041223	Product data	-	LPC2292_2294 v.1
LPC2292_2294 v.1	20040205	Preliminary data	-	-