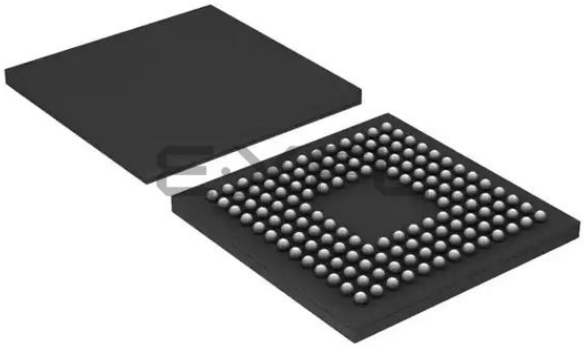


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2292fet144-01-5

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC2294HBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/00	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

3.1 Ordering options

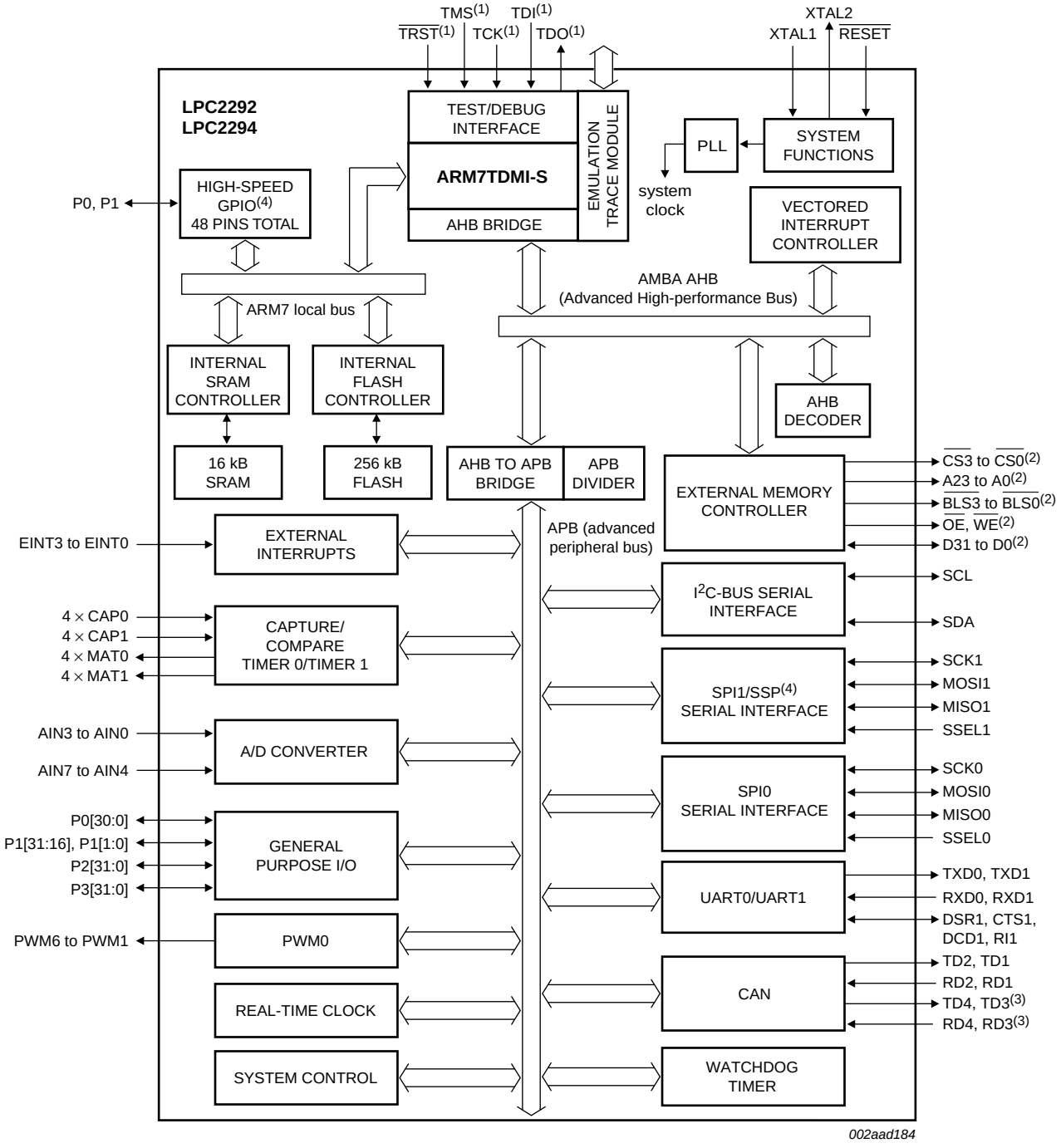
Table 2. Ordering options

Type number	Flash memory	RAM	CAN	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2292FBD144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/00	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2292FET144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/G	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2294HBD144	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/00	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/01	256 kB	16 kB	4 channels	yes	−40 °C to +125 °C

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

4. Block diagram



(1) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(2) Pins shared with GPIO.

(3) Available in LPC2294 only.

(4) SSP interface and high-speed GPIO are available on LPC2292/2294/01 only.

Fig 1. Block diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 3. Ball allocation

Row	Column												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2[22]/ D22	$V_{DDA(1V8)}$	P1[28]/ TDI	P2[21]/ D21	P2[18]/ D18	P2[14]/ D14	P1[29]/ TCK	P2[11]/ D11	P2[10]/ D10	P2[7]/D7	$V_{DD(3V3)}$	$V_{DD(1V8)}$	P2[4]/D4
B	$V_{DD(3V3)}$	P1[27]/ TDO	XTAL2	$V_{SSA(PLL)}$	P2[19]/ D19	P2[15]/ D15	P2[12]/ D12	P0[20]/ MAT1[3]/ SSEL1/ EINT3	$V_{DD(3V3)}$	P2[6]/D6	V_{SS}	P2[3]/D3	V_{SS}
C	P0[21]/ PWM5/ CAP1[3]	V_{SS}	XTAL1	V_{SSA}	$\overline{\text{RESET}}$	P2[16]/ D16	P2[13]/ D13	P0[19]/ MAT1[2]/ MOSI1/ CAP1[2]	P2[9]/D9	P2[5]/D5	P2[2]/D2	P2[1]/D1	$V_{DD(3V3)}$
D	P0[24]/ TD2	P1[19]/ TRACE PKT3	P0[23]/ RD2	P0[22]/ CAP0[0]/ MAT0[0]	P2[20]/ D20	P2[17]/ D17	V_{SS}	P0[18]/ CAP1[3]/ MISO1/ MAT1[3]	P2[8]/D8	P1[30]/ TMS	V_{SS}	P1[20]/ TRACE SYNC	P0[17]/ CAP1[2]/ SCK1/ MAT1[2]
E	P2[25]/ D25	P2[24]/ D24	P2[23]	V_{SS}						P0[16]/ EINT0/ MAT0[2]/ CAP0[2]	P0[15]/ RI1/ EINT2	P2[0]/D0	P3[30]/ BLS1
F	P2[27]/ D27/ BOOT1	P1[18]/ TRACE PKT2	$V_{DDA(3V3)}$	P2[26]/ D26/ BOOT0						P3[31]/ BLS0	P1[21]/ PIPE STAT0	$V_{DD(3V3)}$	V_{SS}
G	P2[29]/ D29	P2[28]/ D28	P2[30]/ D30/AIN4	P2[31]/ D31/AIN5						P0[14]/ DCD1/ EINT1	P1[0]/$\overline{\text{CS0}}$	P3[0]/A0	P1[1]/$\overline{\text{OE}}$
H	P0[25]/ RD1	TD1	P0[27]/ AIN0/ CAP0[1]/ MAT0[1]	P1[17]/ TRACE PKT1						P0[13]/ DTR1/ MAT1[1]	P1[22]/ PIPE STAT1	P3[2]/A2	P3[1]/A1
J	P0[28]/ AIN1/ CAP0[2]/ MAT0[2]	V_{SS}	P3[29]/ BLS2/ AIN6	P3[28]/ BLS3/ AIN7						P3[3]/A3	P1[23]/ PIPE STAT2	P0[11]/ CTS1/ CAP1[1]	P0[12]/ DSR1/ MAT1[0]
K	P3[27]/ WE	P3[26]/ CS1	$V_{DD(3V3)}$	P3[22]/ A22	P3[20]/ A20	P0[1]/ RXD0/ PWM3/ EINT0	P3[14]/ A14	P1[25]/ EXTIN0	P3[11]/ A11	$V_{DD(3V3)}$	P0[10]/ RTS1/ CAP1[0]	V_{SS}	P3[4]/A4

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 3. Ball allocation *…continued*

Row	Column												
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
L	P0[29]/ AIN2/ CAP0[3]/ MAT0[3]	P0[30]/ AIN3/ EINT3/ CAP0[0]	P1[16]/ TRACE PKT0	P0[0]/ TXD0/ PWM1	P3[19]/ A19	P0[2]/ SCL/ CAP0[0]	P3[15]/ A15	P0[4]/ SCK0/ CAP0[1]	P3[12]/ A12	V_{SS}	P1[24]/ TRACE CLK	P0[8]/ TXD1/ PWM4	P0[9]/ RXD1/ PWM6/ EINT3
M	P3[25]/ CS2	P3[24]/ CS3	$V_{DD(3V3)}$	P1[31]/ TRST	P3[18]/ A18	$V_{DD(3V3)}$	P3[16]/ A16	P0[3]/ SDA/ MAT0[0]/ EINT1	P3[13]/ A13	P3[9]/A9	P0[7]/ SSEL0/ PWM2/ EINT2	P3[7]/A7	P3[5]/A5
N	$V_{DD(1V8)}$	V_{SS}	P3[23]/ A23/ XCLK	P3[21]/ A21	P3[17]/ A17	P1[26]/ RTCK	V_{SS}	$V_{DD(3V3)}$	P0[5]/ MISO0/ MAT0[1]	P3[10]/ A10	P0[6]/ MOSI0/ CAP0[2]	P3[8]/A8	P3[6]/A6

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P2[24]/D24	11[7]	E2[7]	I/O	**D24 —** External memory data line 24.
P2[25]/D25	12[7]	E1[7]	I/O	**D25 —** External memory data line 25.
P2[26]/D26/ BOOT0	13[7]	F4[7]	I/O	**D26 —** External memory data line 26.
			I	**BOOT0 —** While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected.
P2[27]/D27/ BOOT1	16[7]	F1[7]	I/O	**D27 —** External memory data line 27.
			I	**BOOT1 —** While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. BOOT1:0 = 00 selects 8-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 01 selects 16-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 10 selects 32-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 11 selects internal flash memory.
P2[28]/D28	17[7]	G2[7]	I/O	**D28 —** External memory data line 28.
P2[29]/D29	18[7]	G1[7]	I/O	**D29 —** External memory data line 29.
P2[30]/D30/ AIN4	19[6]	G3[6]	I/O	**D30 —** External memory data line 30.
			I	**AIN4 —** ADC, input 4. This analog input is always connected to its pin.
P2[31]/D31/ AIN5	20[6]	G4[6]	I/O	**D31 —** External memory data line 31.
			I	**AIN5 —** ADC, input 5. This analog input is always connected to its pin.
P3[0] to P3[31]			I/O	**Port 3 —** Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3[0]/A0	89[7]	G12[7]	O	**A0 —** External memory address line 0.
P3[1]/A1	88[7]	H13[7]	O	**A1 —** External memory address line 1.
P3[2]/A2	87[7]	H12[7]	O	**A2 —** External memory address line 2.
P3[3]/A3	81[7]	J10[7]	O	**A3 —** External memory address line 3.
P3[4]/A4	80[7]	K13[7]	O	**A4 —** External memory address line 4.
P3[5]/A5	74[7]	M13[7]	O	**A5 —** External memory address line 5.
P3[6]/A6	73[7]	N13[7]	O	**A6 —** External memory address line 6.
P3[7]/A7	72[7]	M12[7]	O	**A7 —** External memory address line 7.
P3[8]/A8	71[7]	N12[7]	O	**A8 —** External memory address line 8.
P3[9]/A9	66[7]	M10[7]	O	**A9 —** External memory address line 9.
P3[10]/A10	65[7]	N10[7]	O	**A10 —** External memory address line 10.
P3[11]/A11	64[7]	K9[7]	O	**A11 —** External memory address line 11.
P3[12]/A12	63[7]	L9[7]	O	**A12 —** External memory address line 12.
P3[13]/A13	62[7]	M9[7]	O	**A13 —** External memory address line 13.
P3[14]/A14	56[7]	K7[7]	O	**A14 —** External memory address line 14.
P3[15]/A15	55[7]	L7[7]	O	**A15 —** External memory address line 15.
P3[16]/A16	53[7]	M7[7]	O	**A16 —** External memory address line 16.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

6.3 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2292/2294 provide 16 kB of SRAM.

6.4 Memory map

The LPC2292/2294 memory maps incorporate several distinct regions, as shown in Figure 4.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.19 “System control”.

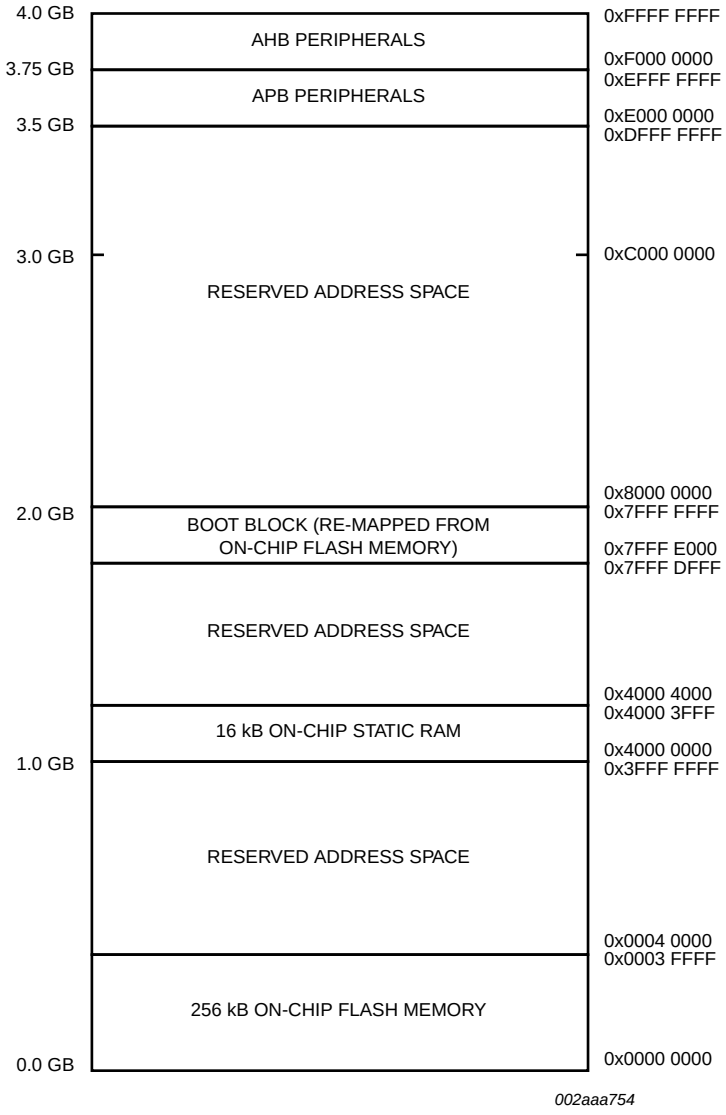


Fig 4. LPC2292/2294 memory map

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 5 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 5. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register Empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Auto-baud time-out (ABTO)[1]End of auto-baud (ABEO)[1]	6

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2292/2294 supports bit rate up to 400 kbit/s (Fast I^2C-bus).

6.12.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2292/2294 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.13.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $\frac{1}{8}$ of the input clock rate.

6.13.2 Features available in LPC2292/2294/01 only

- Eight to 16 bits per frame.
- When the SPI interface is used in Master mode, the SSELn pin is not needed (can be used for a different function).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

6.14 SSP controller (LPC2292/94/01 only)

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

While the SSP and SPI1 peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI1 to SSP and back.

6.14.1 Features

- Compatible with Motorola's SPI, Texas Instrument's 4-wire SSI, and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

6.15 General purpose timers

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

6.15.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Timer or external event counter operation
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

6.15.2 Features available in LPC2292/2294/01 only

The LPC2292/2294/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to PCLK / 4. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than 1 / (2PCLK).

6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.19 System control

6.19.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2292/2294: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power-on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC2292/2294/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

Remark: Devices without a /00 or /01 in the name have only a security level equivalent to CRP2 available.

6.19.5 External interrupt inputs

The LPC2292/2294 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.19.6 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

7. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	−0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	−0.5	+3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			−0.5	+4.6	V
V_{IA}	analog input voltage			−0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	−0.5	+6.0	V
		other I/O pins	[4][6]	−0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature		[10]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[11]			
		all pins		−2000	+2000	V

[1] The following applies to Table 6:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

8. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V	[9]	0	0	0	μA

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1[25:16].

[11] See the *LPC2119/2129/2194/2292/2294 User Manual*.

[12] To V_{SS}.

Table 8. ADC static characteristics
V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +125 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

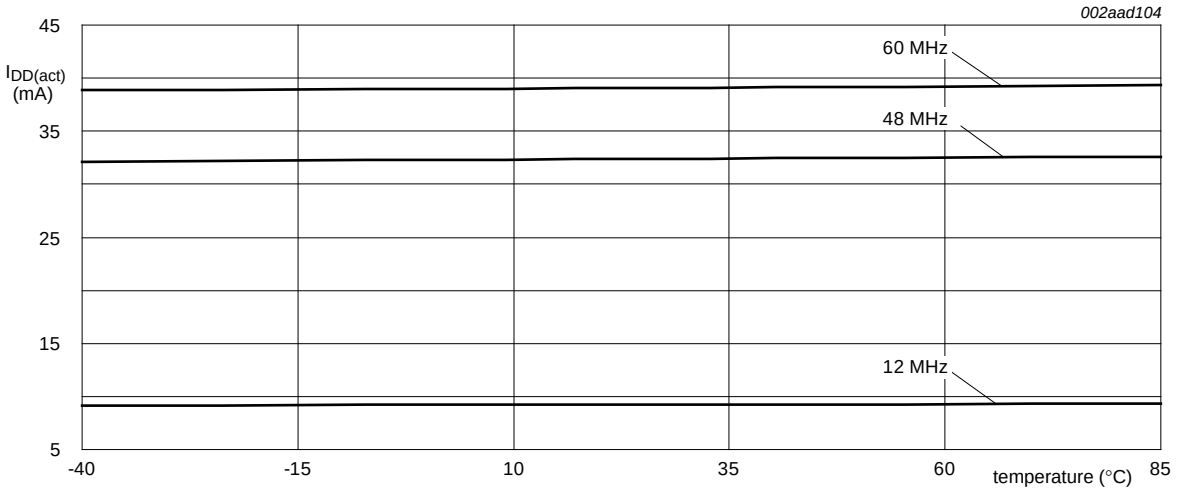
[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.

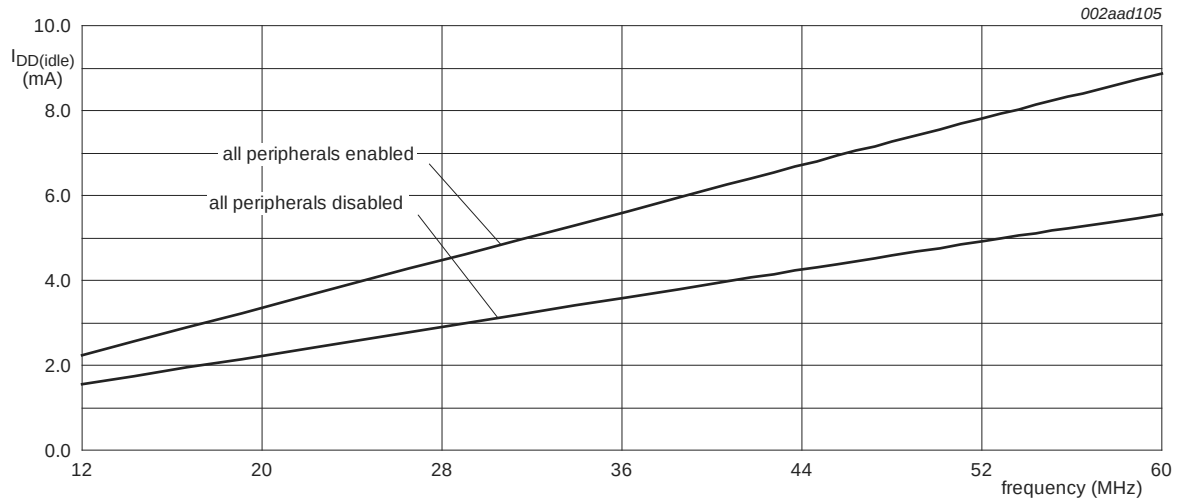
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



Test conditions: Active mode entered executing code on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 8. Typical LPC2292/01 $I_{DD(act)}$ measured at different temperatures

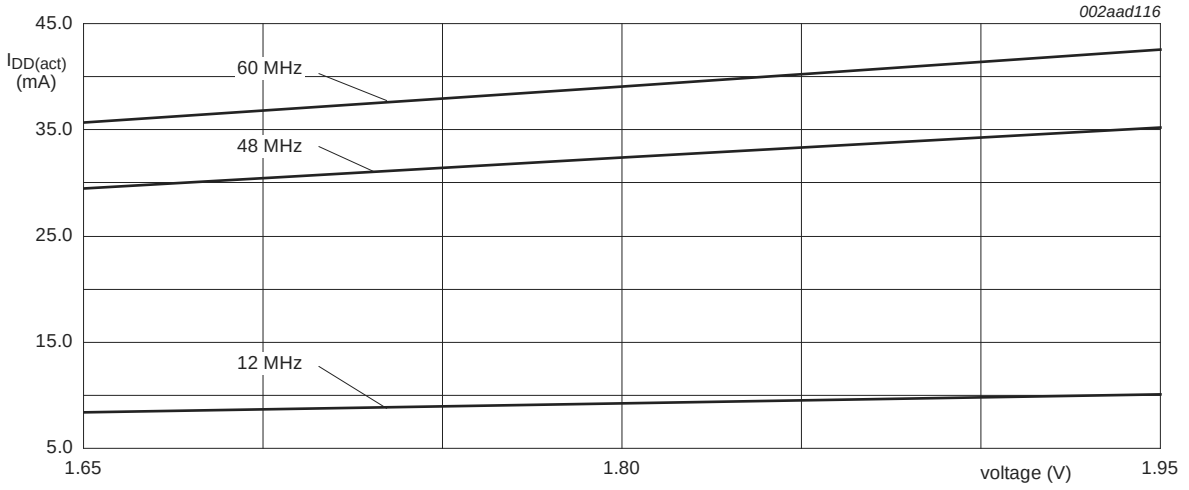


Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; core voltage 1.8 V.

Fig 9. Typical LPC2292/01 $I_{DD(idle)}$ measured at different frequencies

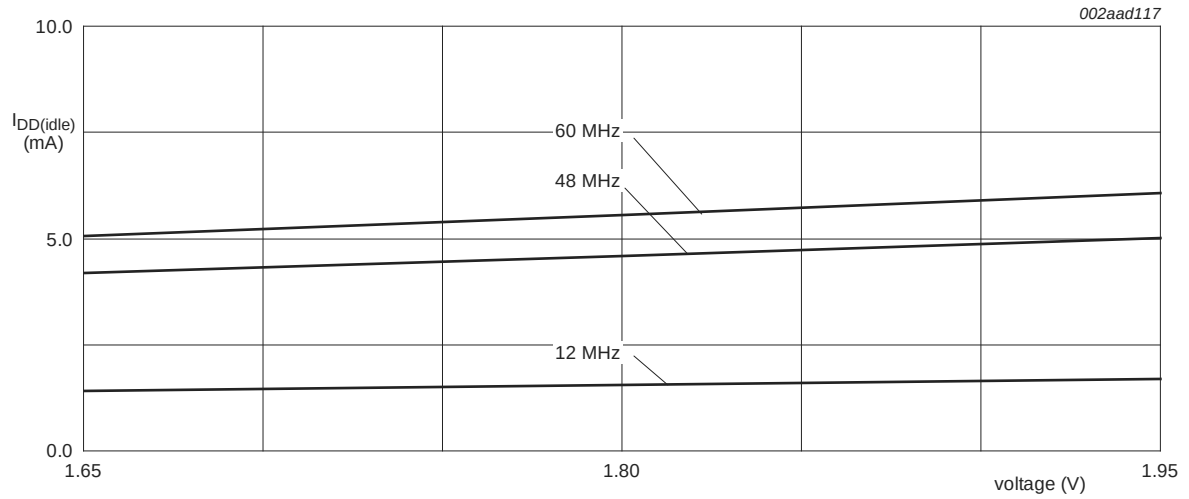
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals disabled.

Fig 20. Typical LPC2292/01 and LPC2294/01 $I_{DD(act)}$ measured at different core voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals disabled.

Fig 21. Typical LPC2292/01 and LPC2294/01 $I_{DD(idle)}$ measured at different core voltages

Table 9. Typical LPC2292/01 peripheral power consumption in active mode

Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

9.1 Timing

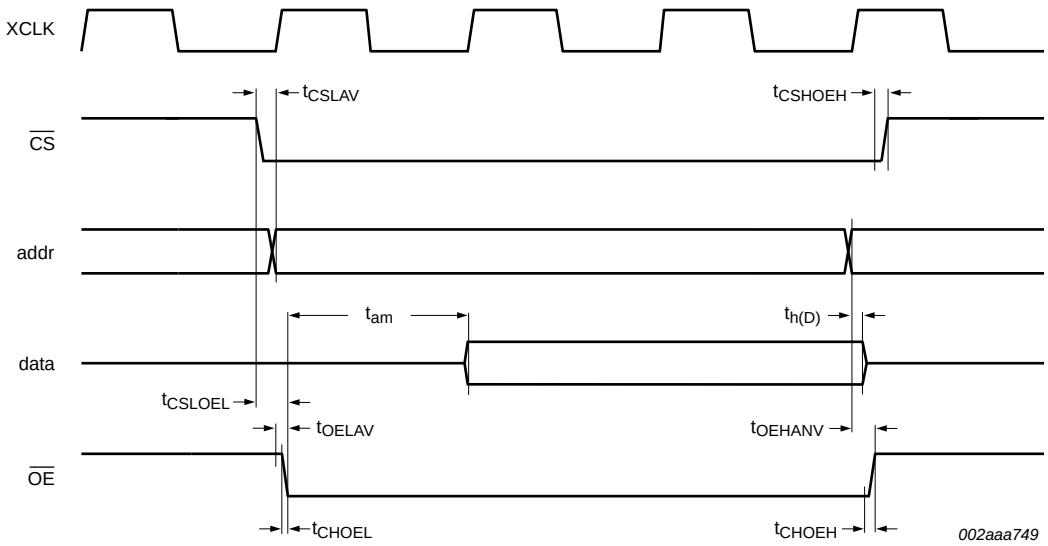


Fig 22. External memory read access

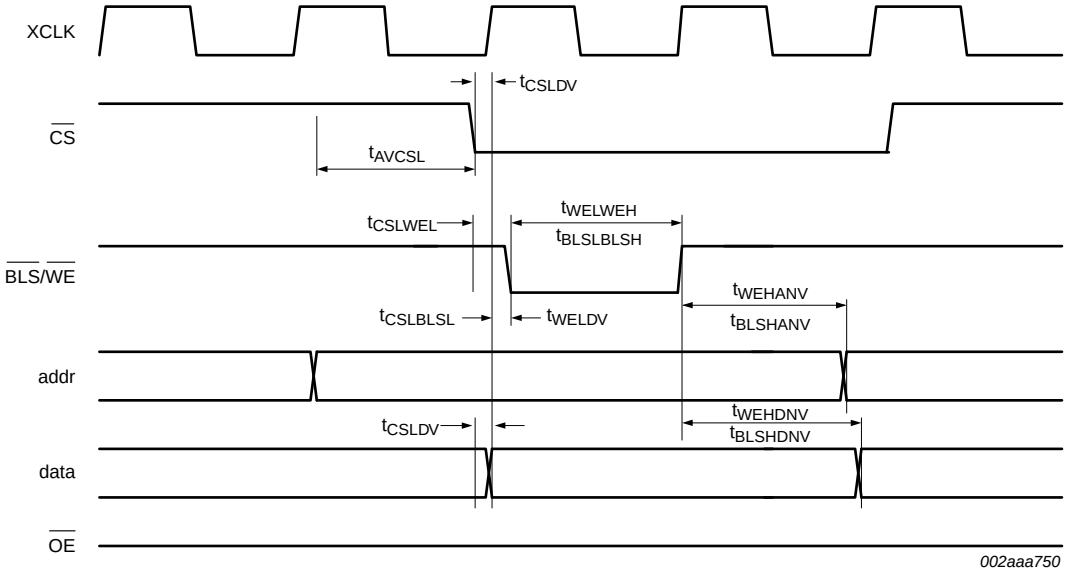


Fig 23. External memory write access

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

14. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.