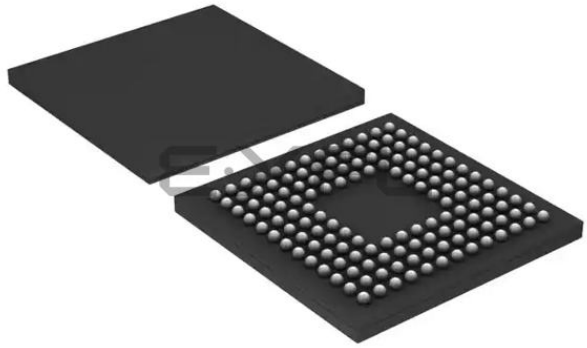

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2292fet144-551

- 16 kB on-chip static RAM and 256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip bootloader software. Single flash sector or full chip erase in 400 ms and programming of 256 B in 1 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software as well as high-speed real-time tracing of instruction execution.
- Two/four (LPC2292/2294) interconnected CAN interfaces with advanced acceptance filters. Additional serial interfaces include two UARTs (16C550), Fast I^2C-bus (400 kbit/s) and two SPIs.
- Eight channel 10-bit ADC with conversion time as low as 2.44 μs.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC), and watchdog.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 112 general purpose I/O pins (5 V tolerant). Up to nine edge/level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

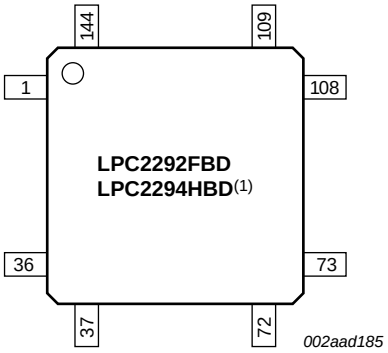
3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2292FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2292FET144/00	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/01	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2

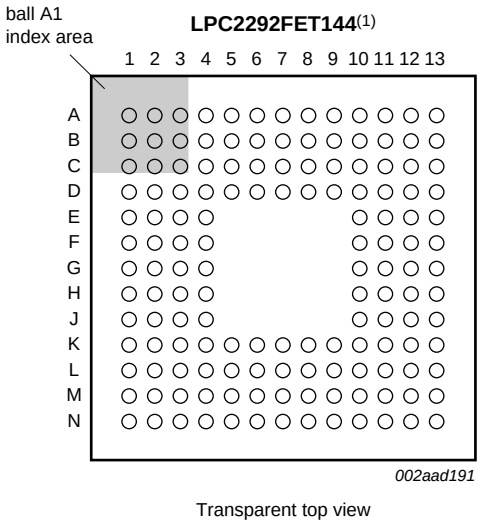
5. Pinning information

5.1 Pinning



(1) Pin configuration is identical for devices with and without /00 and /01 suffixes.

Fig 2. LQFP144 pinning



(1) Pin configuration is identical for devices with and without /00 and /01 suffixes.

Fig 3. TFBGA144 pinning

Table 3. Ball allocation

Row	Column												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2[22]/ D22	$V_{DDA(1V8)}$	P1[28]/ TDI	P2[21]/ D21	P2[18]/ D18	P2[14]/ D14	P1[29]/ TCK	P2[11]/ D11	P2[10]/ D10	P2[7]/D7	$V_{DD(3V3)}$	$V_{DD(1V8)}$	P2[4]/D4
B	$V_{DD(3V3)}$	P1[27]/ TDO	XTAL2	$V_{SSA(PLL)}$	P2[19]/ D19	P2[15]/ D15	P2[12]/ D12	P0[20]/ MAT1[3]/ SSEL1/ EINT3	$V_{DD(3V3)}$	P2[6]/D6	V_{SS}	P2[3]/D3	V_{SS}
C	P0[21]/ PWM5/ CAP1[3]	V_{SS}	XTAL1	V_{SSA}	$\overline{\text{RESET}}$	P2[16]/ D16	P2[13]/ D13	P0[19]/ MAT1[2]/ MOSI1/ CAP1[2]	P2[9]/D9	P2[5]/D5	P2[2]/D2	P2[1]/D1	$V_{DD(3V3)}$
D	P0[24]/ TD2	P1[19]/ TRACE PKT3	P0[23]/ RD2	P0[22]/ CAP0[0]/ MAT0[0]	P2[20]/ D20	P2[17]/ D17	V_{SS}	P0[18]/ CAP1[3]/ MISO1/ MAT1[3]	P2[8]/D8	P1[30]/ TMS	V_{SS}	P1[20]/ TRACE SYNC	P0[17]/ CAP1[2]/ SCK1/ MAT1[2]
E	P2[25]/ D25	P2[24]/ D24	P2[23]	V_{SS}						P0[16]/ EINT0/ MAT0[2]/ CAP0[2]	P0[15]/ RI1/ EINT2	P2[0]/D0	P3[30]/ BLS1
F	P2[27]/ D27/ BOOT1	P1[18]/ TRACE PKT2	$V_{DDA(3V3)}$	P2[26]/ D26/ BOOT0						P3[31]/ BLS0	P1[21]/ PIPE STAT0	$V_{DD(3V3)}$	V_{SS}
G	P2[29]/ D29	P2[28]/ D28	P2[30]/ D30/AIN4	P2[31]/ D31/AIN5						P0[14]/ DCD1/ EINT1	P1[0]/$\overline{\text{CS0}}$	P3[0]/A0	P1[1]/$\overline{\text{OE}}$
H	P0[25]/ RD1	TD1	P0[27]/ AIN0/ CAP0[1]/ MAT0[1]	P1[17]/ TRACE PKT1						P0[13]/ DTR1/ MAT1[1]	P1[22]/ PIPE STAT1	P3[2]/A2	P3[1]/A1
J	P0[28]/ AIN1/ CAP0[2]/ MAT0[2]	V_{SS}	P3[29]/ BLS2/ AIN6	P3[28]/ BLS3/ AIN7						P3[3]/A3	P1[23]/ PIPE STAT2	P0[11]/ CTS1/ CAP1[1]	P0[12]/ DSR1/ MAT1[0]
K	P3[27]/ WE	P3[26]/ CS1	$V_{DD(3V3)}$	P3[22]/ A22	P3[20]/ A20	P0[1]/ RXD0/ PWM3/ EINT0	P3[14]/ A14	P1[25]/ EXTIN0	P3[11]/ A11	$V_{DD(3V3)}$	P0[10]/ RTS1/ CAP1[0]	V_{SS}	P3[4]/A4

5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/ PWM1	42[2]	L4[2]	O	**TXD0 —** Transmitter output for UART0.
			O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	49[4]	K6[4]	I	**RXD0 —** Receiver input for UART0.
			O	**PWM3 —** Pulse Width Modulator output 3.
			I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/ CAP0[0]	50[5]	L6[5]	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	58[5]	M8[5]	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
			I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	59[2]	L8[2]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	61[2]	N9[2]	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	68[2]	N11[2]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	69[4]	M11[4]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**PWM2 —** Pulse Width Modulator output 2.
			I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4	75[2]	L12[2]	O	**TXD1 —** Transmitter output for UART1.
			O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	76[4]	L13[4]	I	**RXD1 —** Receiver input for UART1.
			O	**PWM6 —** Pulse Width Modulator output 6.
			I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	78[2]	K11[2]	O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	83[2]	J12[2]	I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P1[25]/EXTIN0	60[7]	K8[7]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	52[7]	N6[7]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	144[7]	B2[7]	O	**TDO —** Test Data out for JTAG interface.
P1[28]/TDI	140[7]	A3[7]	I	**TDI —** Test Data in for JTAG interface.
P1[29]/TCK	126[7]	A7[7]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	113[7]	D10[7]	I	**TMS —** Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	43[7]	M4[7]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
P2[0] to P2[31]			I/O	**Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2[0]/D0	98[7]	E12[7]	I/O	**D0 —** External memory data line 0.
P2[1]/D1	105[7]	C12[7]	I/O	**D1 —** External memory data line 1.
P2[2]/D2	106[7]	C11[7]	I/O	**D2 —** External memory data line 2.
P2[3]/D3	108[7]	B12[7]	I/O	**D3 —** External memory data line 3.
P2[4]/D4	109[7]	A13[7]	I/O	**D4 —** External memory data line 4.
P2[5]/D5	114[7]	C10[7]	I/O	**D5 —** External memory data line 5.
P2[6]/D6	115[7]	B10[7]	I/O	**D6 —** External memory data line 6.
P2[7]/D7	116[7]	A10[7]	I/O	**D7 —** External memory data line 7.
P2[8]/D8	117[7]	D9[7]	I/O	**D8 —** External memory data line 8.
P2[9]/D9	118[7]	C9[7]	I/O	**D9 —** External memory data line 9.
P2[10]/D10	120[7]	A9[7]	I/O	**D10 —** External memory data line 10.
P2[11]/D11	124[7]	A8[7]	I/O	**D11 —** External memory data line 11.
P2[12]/D12	125[7]	B7[7]	I/O	**D12 —** External memory data line 12.
P2[13]/D13	127[7]	C7[7]	I/O	**D13 —** External memory data line 13.
P2[14]/D14	129[7]	A6[7]	I/O	**D14 —** External memory data line 14.
P2[15]/D15	130[7]	B6[7]	I/O	**D15 —** External memory data line 15.
P2[16]/D16	131[7]	C6[7]	I/O	**D16 —** External memory data line 16.
P2[17]/D17	132[7]	D6[7]	I/O	**D17 —** External memory data line 17.
P2[18]/D18	133[7]	A5[7]	I/O	**D18 —** External memory data line 18.
P2[19]/D19	134[7]	B5[7]	I/O	**D19 —** External memory data line 19.
P2[20]/D20	136[7]	D5[7]	I/O	**D20 —** External memory data line 20.
P2[21]/D21	137[7]	A4[7]	I/O	**D21 —** External memory data line 21.
P2[22]/D22	1[7]	A1[7]	I/O	**D22 —** External memory data line 22.
P2[23]/D23	10[7]	E3[7]	I/O	**D23 —** External memory data line 23.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set
- A 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2292/2294 incorporate a 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the on-chip bootloader is used, 248 kB of flash memory is available for user code.

The LPC2292/2294 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.64) provides Code Read Protection (CRP) for the LPC2292/2294 on-chip flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip RAM or flash memory are disabled. However, the ISP flash erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

6.14 SSP controller (LPC2292/94/01 only)

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

While the SSP and SPI1 peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI1 to SSP and back.

6.14.1 Features

- Compatible with Motorola's SPI, Texas Instrument's 4-wire SSI, and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

6.15 General purpose timers

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

6.15.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Timer or external event counter operation
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.15.2 Features available in LPC2292/2294/01 only

The LPC2292/2294/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to PCLK / 4. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than 1 / (2PCLK).

6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.18 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2292/2294. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.19 System control

6.19.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2292/2294: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power-on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC2292/2294/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

Remark: Devices without a /00 or /01 in the name have only a security level equivalent to CRP2 available.

6.19.5 External interrupt inputs

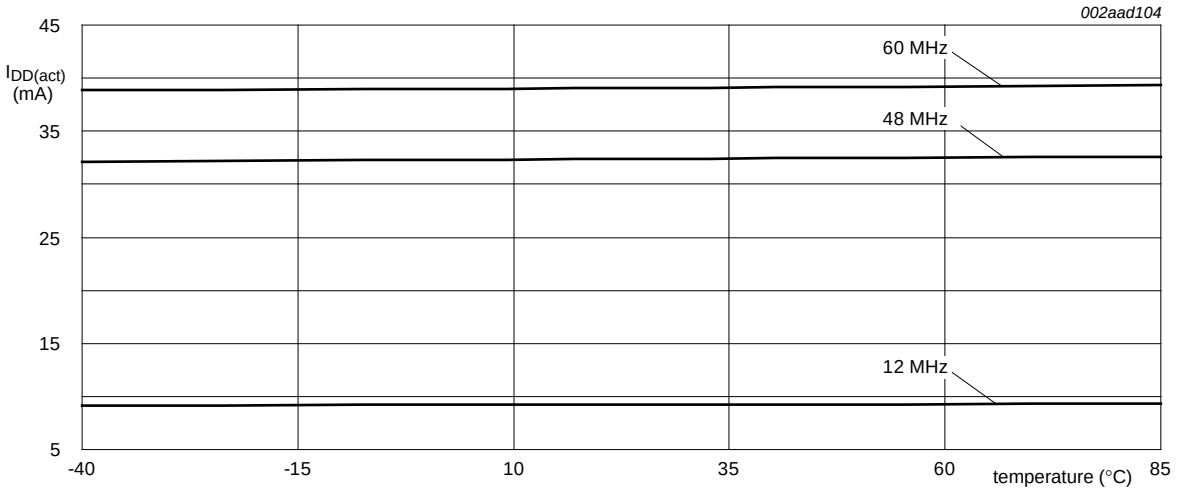
The LPC2292/2294 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.19.6 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

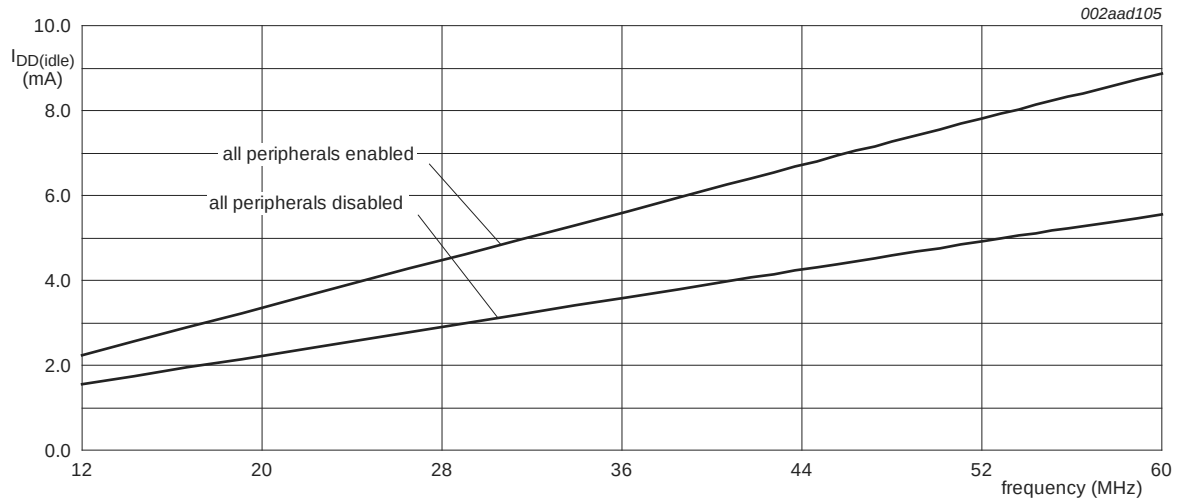
Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Power consumption LPC2292, LPC2292/00, LPC2294, LPC2294/00							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	50	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 125 °C		-	300	1000	µA
Power consumption LPC2292/01 and LPC2294/01							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	45	-	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	11.5	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 125 °C		-	300	1000	µA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	µA
		V_I = 5 V		-	10	22	µA



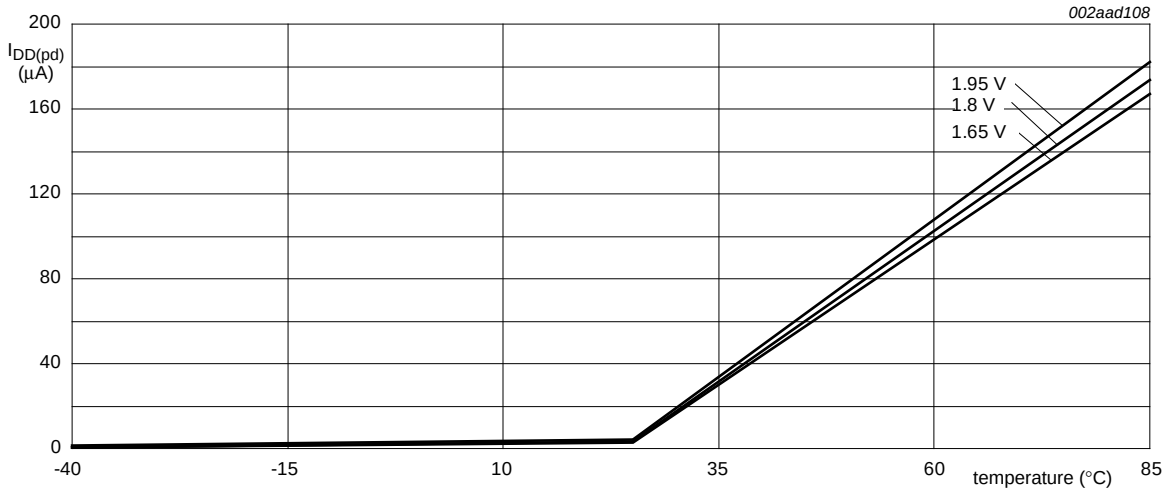
Test conditions: Active mode entered executing code on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 8. Typical LPC2292/01 $I_{DD(act)}$ measured at different temperatures



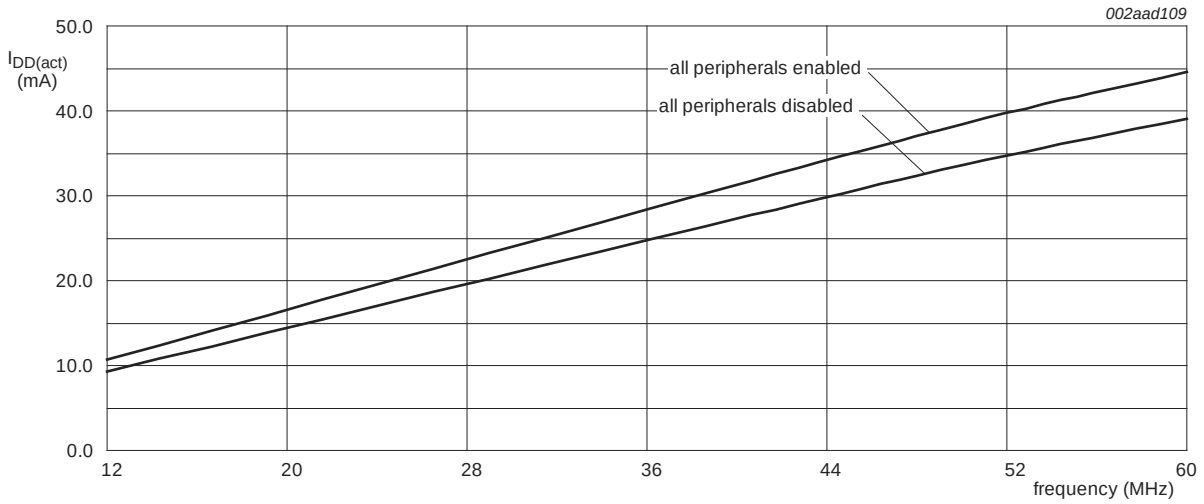
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; core voltage 1.8 V.

Fig 9. Typical LPC2292/01 $I_{DD(idle)}$ measured at different frequencies



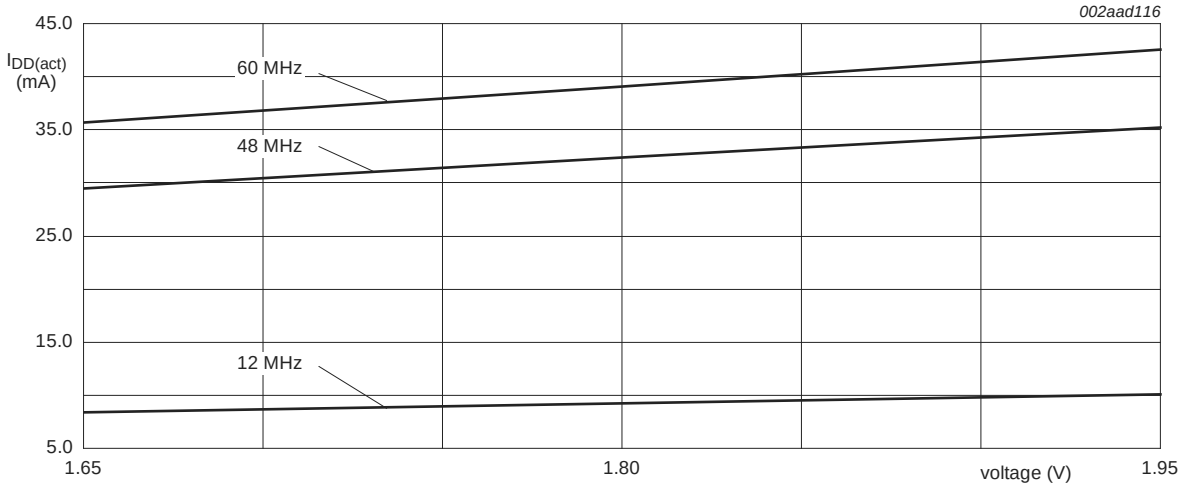
Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 12. Typical LPC2292/01 core power-down current $I_{DD(pd)}$ measured at different temperatures



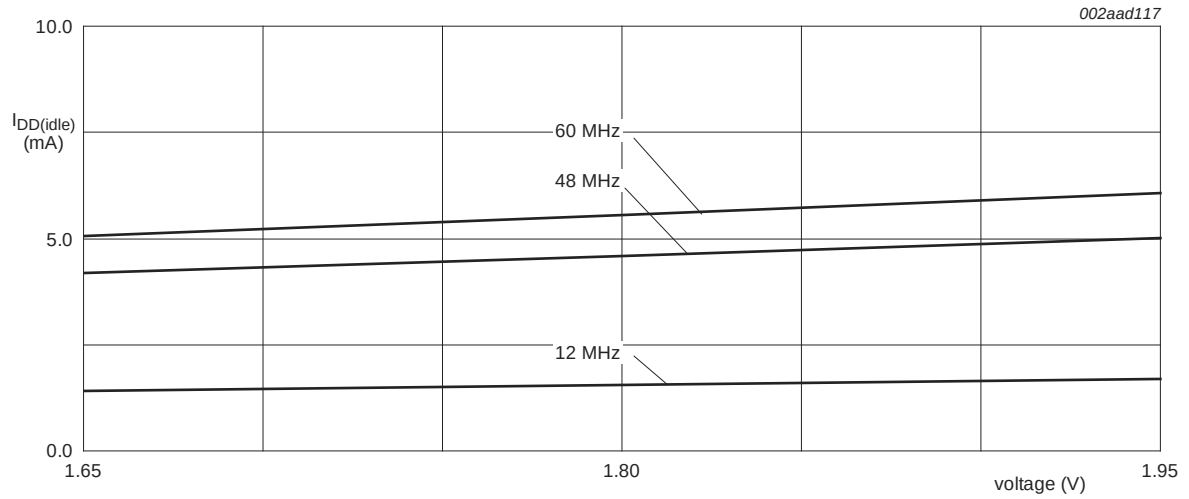
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 13. Typical LPC2294/01 $I_{DD(act)}$ measured at different frequencies



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals disabled.

Fig 20. Typical LPC2292/01 and LPC2294/01 $I_{DD(act)}$ measured at different core voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals disabled.

Fig 21. Typical LPC2292/01 and LPC2294/01 $I_{DD(idle)}$ measured at different core voltages

Table 9. Typical LPC2292/01 peripheral power consumption in active mode

Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421

Table 9. Typical LPC2292/01 peripheral power consumption in active mode *...continued*
Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
PWM0	103	341	407
I^2C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
PCEMC	306	994	1205
ADC	33	128	167
CAN1/2	229	771	914

Table 10. Typical LPC2294/01 peripheral power consumption in active mode
Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421
PWM0	103	341	407
I^2C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
PCEMC	306	994	1205
ADC	33	128	167
CAN1/2/3/4	230	769	912

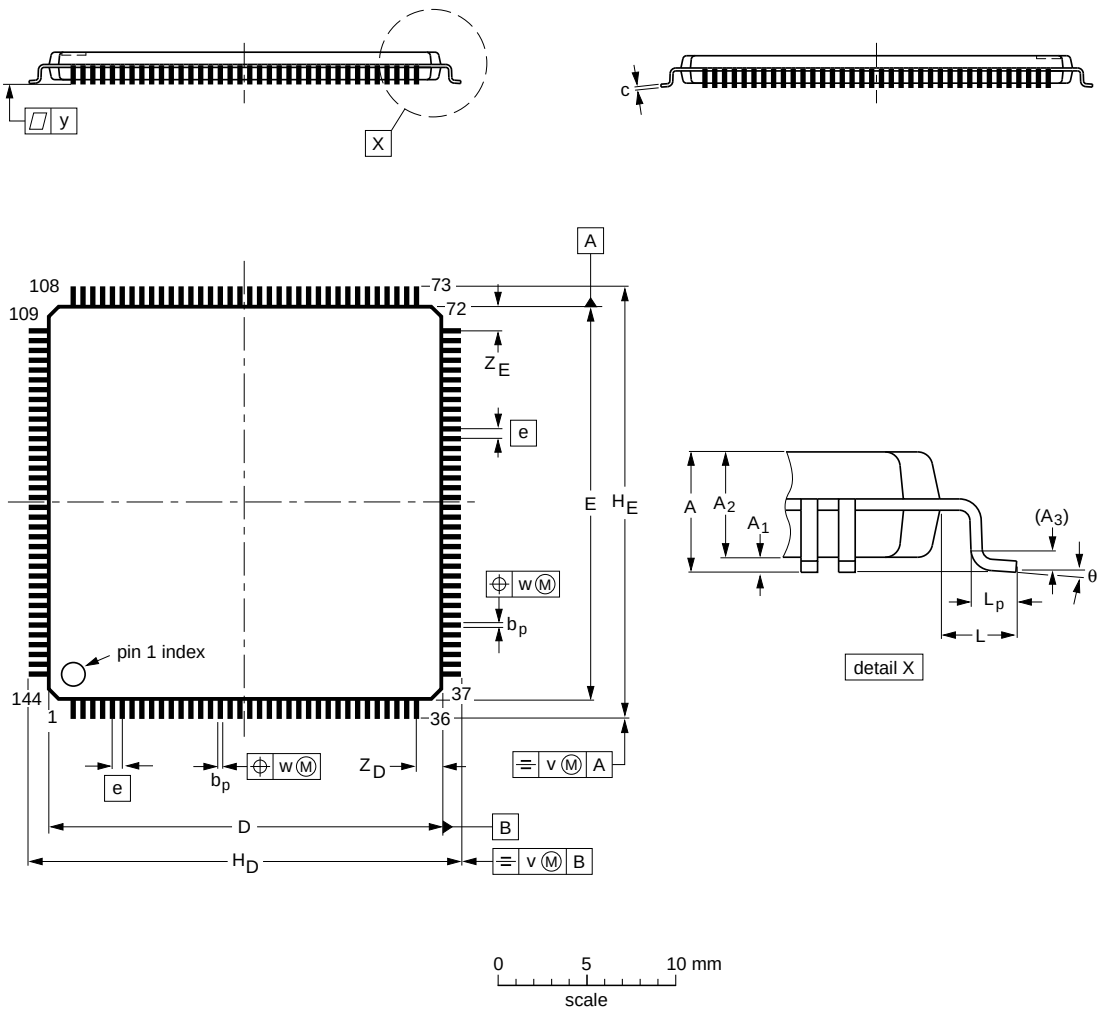
9. Dynamic characteristics

Table 11. Dynamic characteristics
T_{amb} = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns

10. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

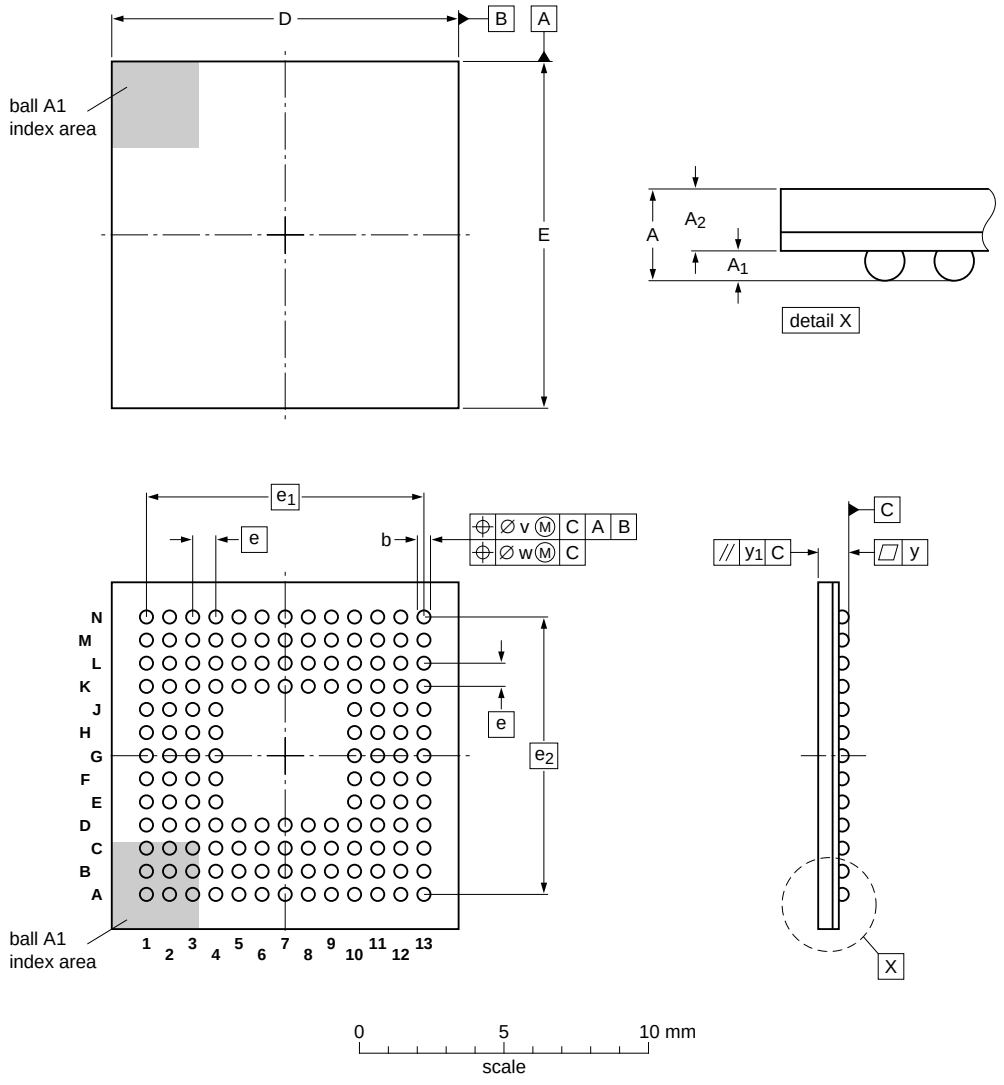
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 25. Package outline SOT486-1 (LQFP144)

TFBGA144: plastic thin fine-pitch ball grid array package; 144 balls **SOT569-2**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	9.6	9.6	0.15	0.05	0.1	0.08
	nom	1.05	0.35	0.70	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT569-2						~~08-01-29~~ 08-03-14

Fig 26. Package outline SOT569-2 (TFBGA144)

12. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2292_2294 v.8	20110608	Product data sheet	201004021F	LPC2292_2294 v.7
Modifications:	• Table 7 “Static characteristics”; Changed /01 Power-down mode supply current ($I_{DD(pd)}$) from 180 μA to 500 μA for industrial temperature range, and 430 μA to 1000 μA for extended temperature range. • Table 7 “Static characteristics”; Changed I^2C pad hysteresis from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$.			
LPC2292_2294 v.7	20081204	Product data sheet	-	LPC2292_2294_6
Modifications:	• Figure 1 “Block diagram”: corrected high-speed GPIO ports 48 pins; P0/P1 only. • Figure 24 “External clock timing (with an amplitude of at least Vi(RMS) = 200 mV)”: removed figure note row “V_{DD} = 1.8 V”, updated graphic. • Table 4 “Pin description”: pad descriptions corrected for pins P2[30], P2[31], P3[28], P3[30], P3[31]. • Table 5 “Interrupt sources”: CAN and UART0/1 interrupt sources corrected. • Table 7 “Static characteristics”: V_{hys}, moved 0.4 from Typ to Min column. • Maximum frequency f_{osc} for external oscillator and external crystal updated. • Changed SOT569-1 to SOT569-2. • Added overbar to indicate LOW-active for $\overline{BLSn}$, $\overline{CSn}$, $\overline{OE}$, and $\overline{WE}$			
LPC2292_2294 v.6	20071210	Product data sheet	-	LPC2292_2294_5
Modifications:	• Type number LPC2292FBD144/01 has been added. • Type number LPC2292FET144/01 has been added. • Type number LPC2294HBD144/01 has been added. • Details introduced with /01 devices on new peripherals/features (Fast I/O ports, SSP, CRP) and enhancements to existing ones (UART0/1, Timers, ADC, and SPI) added. • Power consumption measurements for LPC2292/2294/01 added. • Description of JTAG pin TCK has been updated.			
LPC2292_2294 v.5	20070215	Product data sheet	-	LPC2292_2294 v.4
LPC2292_2294 v.4	20060711	Product data sheet	-	LPC2292_2294 v.3
LPC2292_2294 v.3	20051101	Product data sheet	-	LPC2292_2294 v.2
LPC2292_2294 v.2	20041223	Product data	-	LPC2292_2294 v.1
LPC2292_2294 v.1	20040205	Preliminary data	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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