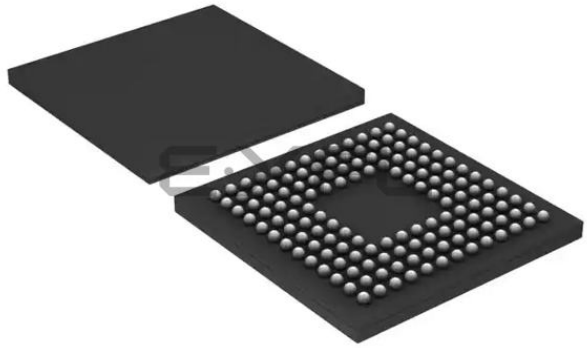

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 60MHz |
| Connectivity | CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 112 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-TFBGA |
| Supplier Device Package | 144-TFBGA (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2292fet144-g-55 |

**Table 3. Ball allocation** *…continued*

| Row | Column | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** |
| L | P0[29]/ AIN2/ CAP0[3]/ MAT0[3] | P0[30]/ AIN3/ EINT3/ CAP0[0] | P1[16]/ TRACE PKT0 | P0[0]/ TXD0/ PWM1 | P3[19]/ A19 | P0[2]/ SCL/ CAP0[0] | P3[15]/ A15 | P0[4]/ SCK0/ CAP0[1] | P3[12]/ A12 | $V_{SS}$ | P1[24]/ TRACE CLK | P0[8]/ TXD1/ PWM4 | P0[9]/ RXD1/ PWM6/ EINT3 |
| M | P3[25]/ CS2 | P3[24]/ CS3 | $V_{DD(3V3)}$ | P1[31]/ TRST | P3[18]/ A18 | $V_{DD(3V3)}$ | P3[16]/ A16 | P0[3]/ SDA/ MAT0[0]/ EINT1 | P3[13]/ A13 | P3[9]/A9 | P0[7]/ SSEL0/ PWM2/ EINT2 | P3[7]/A7 | P3[5]/A5 |
| N | $V_{DD(1V8)}$ | $V_{SS}$ | P3[23]/ A23/ XCLK | P3[21]/ A21 | P3[17]/ A17 | P1[26]/ RTCK | $V_{SS}$ | $V_{DD(3V3)}$ | P0[5]/ MISO0/ MAT0[1] | P3[10]/ A10 | P0[6]/ MOSI0/ CAP0[2] | P3[8]/A8 | P3[6]/A6 |

**Table 4. Pin description** *…continued*

| Symbol | Pin (LQFP) | Pin (TFBGA)[1] | Type | Description |
|---|---|---|---|---|
| P0[12]/DSR1/ MAT1[0]/RD4 | 84[2] | J13[2] | I | **DSR1 —** Data Set Ready input for UART1. |
| | | | O | **MAT1[0] —** Match output for Timer 1, channel 0. |
| | | | I | **RD4 —** CAN4 receiver input (LPC2294 only). |
| P0[13]/DTR1/ MAT1[1]/TD4 | 85[2] | H10[2] | O | **DTR1 —** Data Terminal Ready output for UART1. |
| | | | O | **MAT1[1] —** Match output for Timer 1, channel 1. |
| | | | O | **TD4 —** CAN4 transmitter output (LPC2294 only). |
| P0[14]/DCD1/ EINT1 | 92[4] | G10[4] | I | **DCD1 —** Data Carrier Detect input for UART1. |
| | | | I | **EINT1 —** External interrupt 1 input.<br>**Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset. |
| P0[15]/RI1/ EINT2 | 99[4] | E11[4] | I | **RI1 —** Ring Indicator input for UART1. |
| | | | I | **EINT2 —** External interrupt 2 input. |
| P0[16]/EINT0/ MAT0[2]/ CAP0[2] | 100[4] | E10[4] | I | **EINT0 —** External interrupt 0 input. |
| | | | O | **MAT0[2] —** Match output for Timer 0, channel 2. |
| | | | I | **CAP0[2] —** Capture input for Timer 0, channel 2. |
| P0[17]/CAP1[2]/ SCK1/MAT1[2] | 101[2] | D13[2] | I | **CAP1[2] —** Capture input for Timer 1, channel 2. |
| | | | I/O | **SCK1 —** Serial Clock for SPI1/SSP[3]. SPI clock output from master or input to slave. |
| | | | O | **MAT1[2] —** Match output for Timer 1, channel 2. |
| P0[18]/CAP1[3]/ MISO1/MAT1[3] | 121[2] | D8[2] | I | **CAP1[3] —** Capture input for Timer 1, channel 3. |
| | | | I/O | **MISO1 —** Master In Slave Out for SPI1/SSP[3]. Data input to SPI master or data output from SPI slave. |
| | | | O | **MAT1[3] —** Match output for Timer 1, channel 3. |
| P0[19]/MAT1[2]/ MOSI1/CAP1[2] | 122[2] | C8[2] | O | **MAT1[2] —** Match output for Timer 1, channel 2. |
| | | | I/O | **MOSI1 —** Master Out Slave In for SPI1/SSP[3]. Data output from SPI master or data input to SPI slave. |
| | | | I | **CAP1[2] —** Capture input for Timer 1, channel 2. |
| P0[20]/MAT1[3]/ SSEL1/EINT3 | 123[4] | B8[4] | O | **MAT1[3] —** Match output for Timer 1, channel 3. |
| | | | I | **SSEL1 —** Slave Select for SPI1/SSP[3]. Selects the SPI interface as a slave. |
| | | | I | **EINT3 —** External interrupt 3 input. |
| P0[21]/PWM5/ RD3/CAP1[3] | 4[2] | C1[2] | O | **PWM5 —** Pulse Width Modulator output 5. |
| | | | I | **RD3 —** CAN3 receiver input (LPC2294 only). |
| | | | I | **CAP1[3] —** Capture input for Timer 1, channel 3. |
| P0[22]/TD3/ CAP0[0]/ MAT0[0] | 5[2] | D4[2] | O | **TD3 —** CAN3 transmitter output (LPC2294 only). |
| | | | I | **CAP0[0] —** Capture input for Timer 0, channel 0. |
| | | | O | **MAT0[0] —** Match output for Timer 0, channel 0. |
| P0[23]/RD2 | 6[2] | D3[2] | I | **RD2 —** CAN2 receiver input. |
| P0[24]/TD2 | 8[2] | D1[2] | O | **TD2 —** CAN2 transmitter output. |
| P0[25]/RD1 | 21[2] | H1[2] | I | **RD1 —** CAN1 receiver input. |

**Table 4. Pin description** *…continued*

| Symbol | Pin (LQFP) | Pin (TFBGA)[1] | Type | Description |
|---|---|---|---|---|
| P1[25]/EXTIN0 | 60[7] | K8[7] | I | **EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up. |
| P1[26]/RTCK | 52[7] | N6[7] | I/O | **RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up.<br>**Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset. |
| P1[27]/TDO | 144[7] | B2[7] | O | **TDO —** Test Data out for JTAG interface. |
| P1[28]/TDI | 140[7] | A3[7] | I | **TDI —** Test Data in for JTAG interface. |
| P1[29]/TCK | 126[7] | A7[7] | I | **TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate. |
| P1[30]/TMS | 113[7] | D10[7] | I | **TMS —** Test Mode Select for JTAG interface. |
| P1[31]/$\overline{\text{TRST}}$ | 43[7] | M4[7] | I | **$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. |
| P2[0] to P2[31] | | | I/O | **Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block. |
| P2[0]/D0 | 98[7] | E12[7] | I/O | **D0 —** External memory data line 0. |
| P2[1]/D1 | 105[7] | C12[7] | I/O | **D1 —** External memory data line 1. |
| P2[2]/D2 | 106[7] | C11[7] | I/O | **D2 —** External memory data line 2. |
| P2[3]/D3 | 108[7] | B12[7] | I/O | **D3 —** External memory data line 3. |
| P2[4]/D4 | 109[7] | A13[7] | I/O | **D4 —** External memory data line 4. |
| P2[5]/D5 | 114[7] | C10[7] | I/O | **D5 —** External memory data line 5. |
| P2[6]/D6 | 115[7] | B10[7] | I/O | **D6 —** External memory data line 6. |
| P2[7]/D7 | 116[7] | A10[7] | I/O | **D7 —** External memory data line 7. |
| P2[8]/D8 | 117[7] | D9[7] | I/O | **D8 —** External memory data line 8. |
| P2[9]/D9 | 118[7] | C9[7] | I/O | **D9 —** External memory data line 9. |
| P2[10]/D10 | 120[7] | A9[7] | I/O | **D10 —** External memory data line 10. |
| P2[11]/D11 | 124[7] | A8[7] | I/O | **D11 —** External memory data line 11. |
| P2[12]/D12 | 125[7] | B7[7] | I/O | **D12 —** External memory data line 12. |
| P2[13]/D13 | 127[7] | C7[7] | I/O | **D13 —** External memory data line 13. |
| P2[14]/D14 | 129[7] | A6[7] | I/O | **D14 —** External memory data line 14. |
| P2[15]/D15 | 130[7] | B6[7] | I/O | **D15 —** External memory data line 15. |
| P2[16]/D16 | 131[7] | C6[7] | I/O | **D16 —** External memory data line 16. |
| P2[17]/D17 | 132[7] | D6[7] | I/O | **D17 —** External memory data line 17. |
| P2[18]/D18 | 133[7] | A5[7] | I/O | **D18 —** External memory data line 18. |
| P2[19]/D19 | 134[7] | B5[7] | I/O | **D19 —** External memory data line 19. |
| P2[20]/D20 | 136[7] | D5[7] | I/O | **D20 —** External memory data line 20. |
| P2[21]/D21 | 137[7] | A4[7] | I/O | **D21 —** External memory data line 21. |
| P2[22]/D22 | 1[7] | A1[7] | I/O | **D22 —** External memory data line 22. |
| P2[23]/D23 | 10[7] | E3[7] | I/O | **D23 —** External memory data line 23. |

# 6. Functional description

## 6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set
- A 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

## 6.2 On-chip flash program memory

The LPC2292/2294 incorporate a 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the on-chip bootloader is used, 248 kB of flash memory is available for user code.

The LPC2292/2294 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.64) provides Code Read Protection (CRP) for the LPC2292/2294 on-chip flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip RAM or flash memory are disabled. However, the ISP flash erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

## 6.3 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2292/2294 provide 16 kB of SRAM.

## 6.4 Memory map

The LPC2292/2294 memory maps incorporate several distinct regions, as shown in Figure 4.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.19 “System control”.

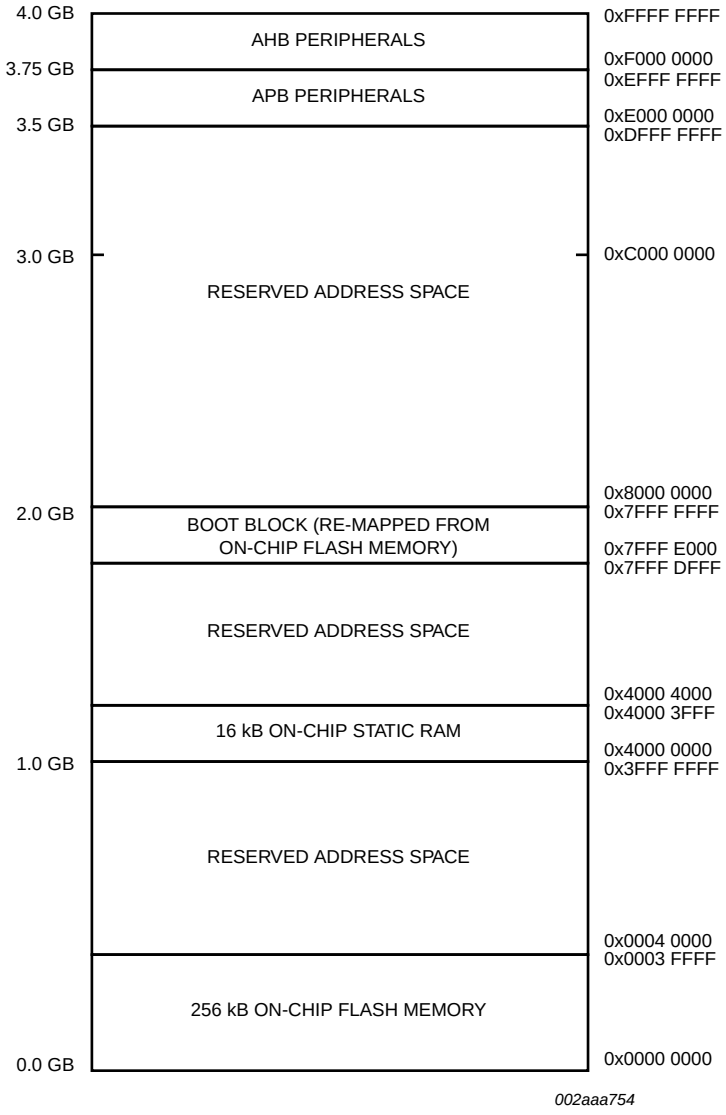



**Fig 4. LPC2292/2294 memory map**

**Table 5. Interrupt sources** *…continued*

| Block | Flag(s) | VIC channel # |
|---|---|---|
| UART1 | RX Line Status (RLS) | 7 |
| | Transmit Holding Register empty (THRE) | |
| | RX Data Available (RDA) | |
| | Character Time-out Indicator (CTI) | |
| | Modem Status Interrupt (MSI) | |
| | Auto-baud time-out (ABTO)[1]End of auto-baud (ABEO)[1] | |
| PWM0 | Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6) | 8 |
| I2C | SI (state change) | 9 |
| SPI0 | SPIF, MODF | 10 |
| SPI1 and SSP[1] | SPIF, MODF and TXRIS, RXRIS, RTRIS, RORRIS | 11 |
| PLL | PLL Lock (PLOCK) | 12 |
| RTC | RTCCIF (Counter Increment), RTCALF (Alarm) | 13 |
| System Control | External Interrupt 0 (EINT0) | 14 |
| | External Interrupt 1 (EINT1) | 15 |
| | External Interrupt 2 (EINT2) | 16 |
| | External Interrupt 3 (EINT3) | 17 |
| ADC | ADC | 18 |
| CAN | 1 ORed CAN Acceptance Filter | 19 |
| | CAN1/2 Tx | 20, 21 |
| | CAN2/3 Tx (LPC2294 only) | 22, 23 |
| | reserved | 24, 25 |
| | CAN1/2 Rx | 26, 27 |
| | CAN3/4 Rx (LPC2294 only) | 28,29 |

[1] SSP interface and UART0/1 auto-baud control are available on LPC2292/2294/01 only.

## 6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

## 6.7 External memory controller

The external Static Memory Controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8-bit, 16-bit, or 32-bit wide.

## 6.8 General purpose parallel I/O (GPIO) and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the parallel I/O registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

### 6.8.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

### 6.8.2 Features added with the Fast GPIO set of registers available on LPC2292/2294/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

## 6.9 10-bit ADC

The LPC2292/2294 each contain a single 10-bit successive approximation ADC with four multiplexed channels.

### 6.9.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

### 6.9.2 ADC features available in LPC2292/2294/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

## 6.10 CAN controllers and acceptance filter

The LPC2292/2294 each contain two/four CAN controllers. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

### 6.10.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit RX identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.

## 6.11 UARTs

The LPC2292/2294 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

### 6.11.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

### 6.11.2 UART features available in LPC2292/2294/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2292/2294/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

## 6.12 $I^2C$-bus serial I/O controller

The $I^2C$-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or

## 6.14 SSP controller (LPC2292/94/01 only)

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

While the SSP and SPI1 peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI1 to SSP and back.

### 6.14.1 Features

- Compatible with Motorola's SPI, Texas Instrument's 4-wire SSI, and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

## 6.15 General purpose timers

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

### 6.15.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Timer or external event counter operation
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

### 6.15.2 Features available in LPC2292/2294/01 only

The LPC2292/2294/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to PCLK / 4. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than 1 / (2PCLK).

## 6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

### 6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

## 6.17 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

### 6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

### 6.19.7 Power control

The LPC2292/2294 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down, and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode, and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

### 6.19.8 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

## 6.20 Emulation and debugging

The LPC2292/2294 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

### 6.20.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. EmbeddedICE protocol converter converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug

# 7. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD(1V8)}$ | supply voltage (1.8 V) | | [2] | −0.5 | +2.5 | V |
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | | [3] | −0.5 | +3.6 | V |
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | | | −0.5 | +4.6 | V |
| $V_{IA}$ | analog input voltage | | | −0.5 | +5.1 | V |
| $V_I$ | input voltage | 5 V tolerant I/O pins | [4][5] | −0.5 | +6.0 | V |
| | | other I/O pins | [4][6] | −0.5 | $V_{DD(3V3)}$ + 0.5 | V |
| $I_{DD}$ | supply current | | [7][8] | - | 100 | mA |
| $I_{SS}$ | ground current | | [8][9] | - | 100 | mA |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{stg}$ | storage temperature | | [10] | −65 | +150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | | - | 1.5 | W |
| $V_{esd}$ | electrostatic discharge voltage | human body model | [11] | | | |
| | | all pins | | −2000 | +2000 | V |

[1] The following applies to Table 6:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

**Table 7. Static characteristics** *…continued*
*$T_{amb}$ = −40 °C to +125 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| **Oscillator pins** | | | | | | |
| $V_{i(XTAL1)}$ | input voltage on pin XTAL1 | | 0 | - | 1.8 | V |
| $V_{o(XTAL2)}$ | output voltage on pin XTAL2 | | 0 | - | 1.8 | V |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[9] Minimum condition for $V_I$ = 4.5 V, maximum condition for $V_I$ = 5.5 V.

[10] Applies to P1[25:16].

[11] See the *LPC2119/2129/2194/2292/2294 User Manual*.

[12] To $V_{SS}$.

**Table 8. ADC static characteristics**
*$V_{DDA}$ = 2.5 V to 3.6 V; $T_{amb}$ = −40 °C to +125 °C unless otherwise specified. ADC frequency 4.5 MHz.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IA}$ | analog input voltage | | 0 | - | $V_{DDA}$ | V |
| $C_{ia}$ | analog input capacitance | | - | - | 1 | pF |
| $E_D$ | differential linearity error | [1][2][3] | - | - | ±1 | LSB |
| $E_{L(adj)}$ | integral non-linearity | [1][4] | - | - | ±2 | LSB |
| $E_O$ | offset error | [1][5] | - | - | ±3 | LSB |
| $E_G$ | gain error | [1][6] | - | - | ±0.5 | % |
| $E_T$ | absolute error | [1][7] | - | - | ±4 | LSB |

[1] Conditions: $V_{SSA}$ = 0 V, $V_{DDA}$ = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

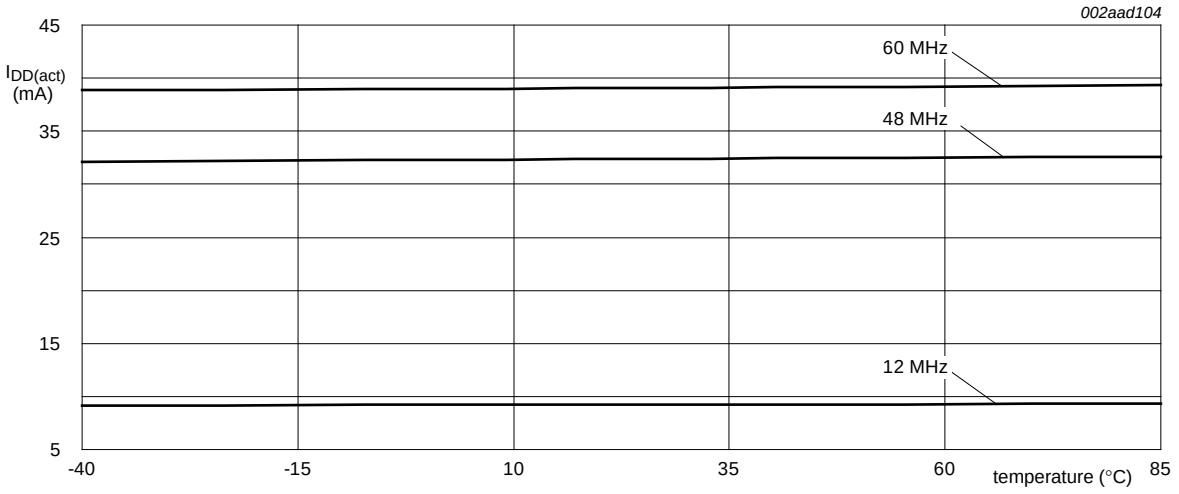
[3] The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

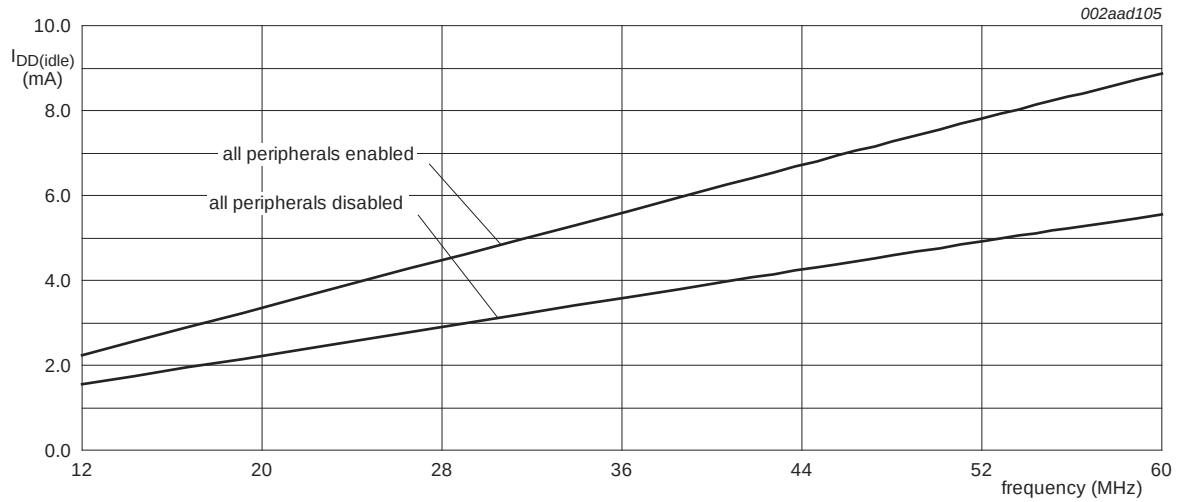
[6] The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute voltage error ($E_T$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.



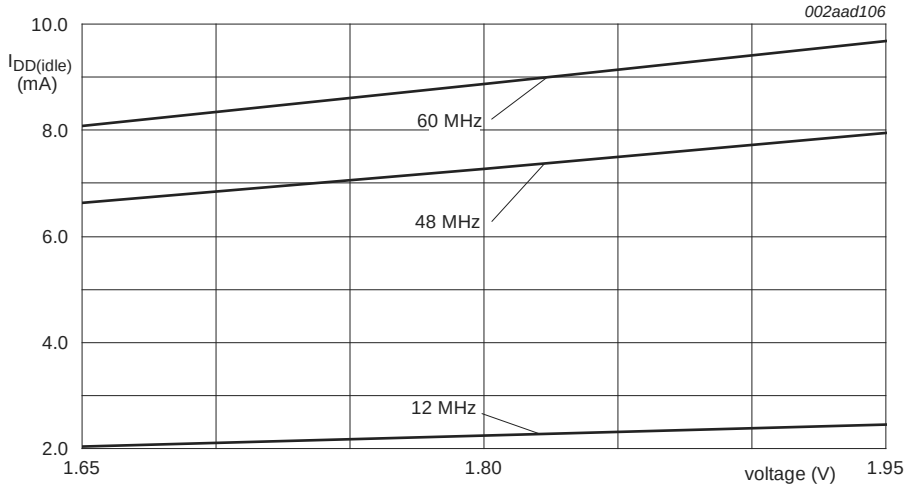

Test conditions: Active mode entered executing code on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

**Fig 8. Typical LPC2292/01 $I_{DD(act)}$ measured at different temperatures**



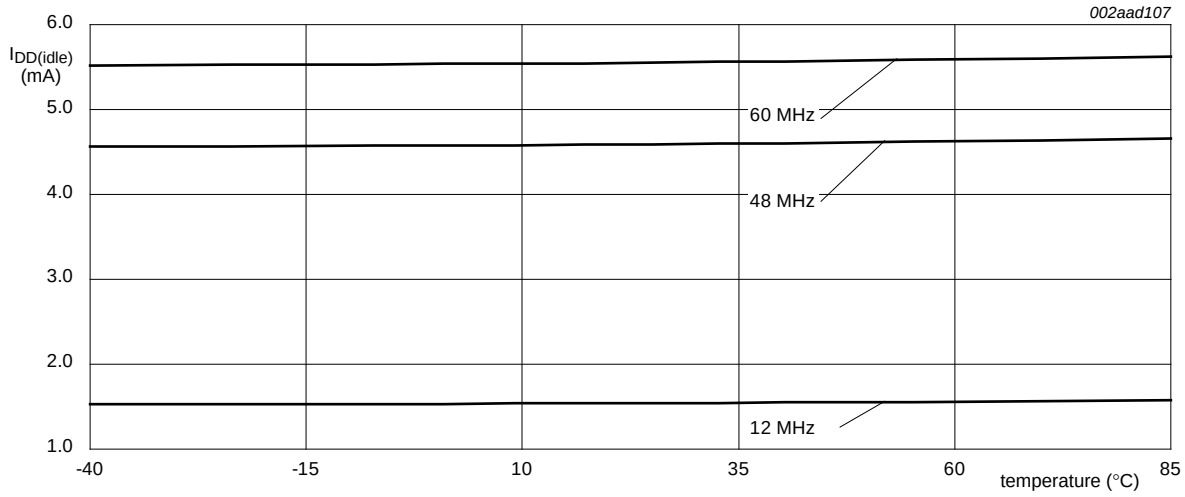

Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; $T_{amb}$ = 25 °C; core voltage 1.8 V.

**Fig 9. Typical LPC2292/01 $I_{DD(idle)}$ measured at different frequencies**



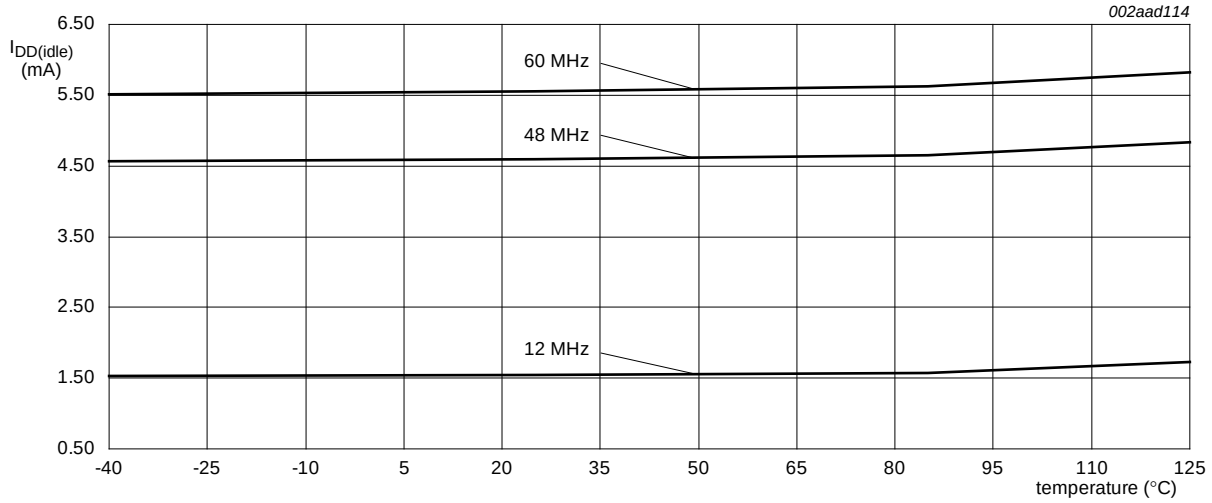

Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
$T_{amb}$ = 25 °C; all peripherals enabled but not active.

**Fig 10. Typical LPC2292/01 $I_{DD(idle)}$ measured at different core voltages**



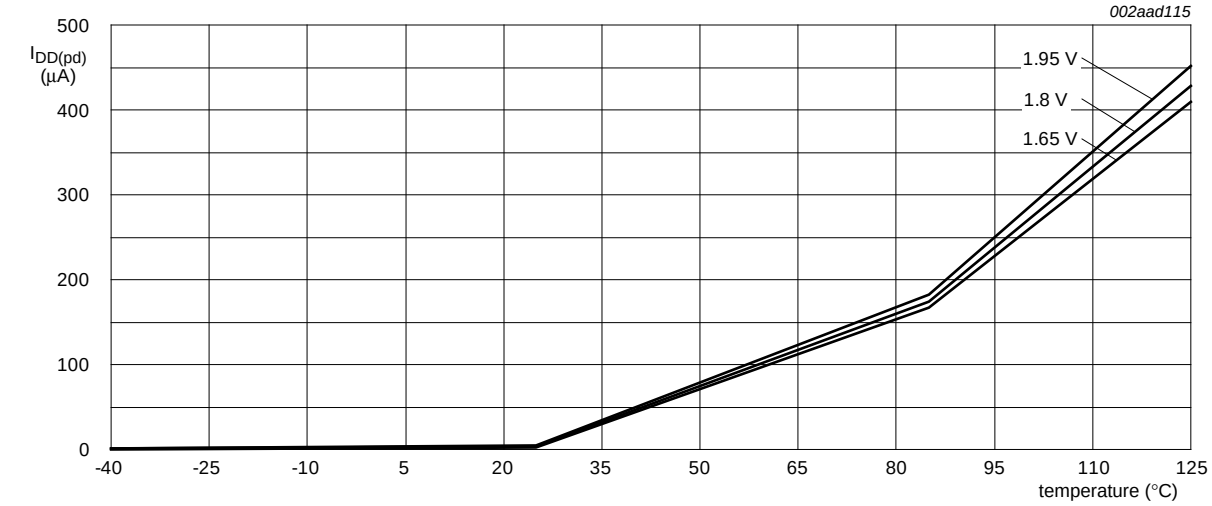

Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Core voltage 1.8 V; all peripherals disabled.

**Fig 11. Typical LPC2292/01 $I_{DD(idle)}$ measured at different temperatures**




Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

**Fig 18. Typical LPC2294/01 $I_{DD(idle)}$ measured at different temperatures**




Test conditions: Power-down mode entered executing code from on-chip flash.

**Fig 19. Typical LPC2294/01 core power-down current $I_{DD(pd)}$ measured at different temperatures**

**Table 9. Typical LPC2292/01 peripheral power consumption in active mode** *...continued*
*Core voltage 1.8 V; $T_{amb}$ = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.*

| Peripheral | CCLK = 12 MHz | CCLK = 48 MHz | CCLK = 60 MHz |
|---|---|---|---|
| PWM0 | 103 | 341 | 407 |
| $I^2C$-bus | 9 | 37 | 53 |
| SPI0/1 | 6 | 27 | 29 |
| RTC | 16 | 55 | 78 |
| PCEMC | 306 | 994 | 1205 |
| ADC | 33 | 128 | 167 |
| CAN1/2 | 229 | 771 | 914 |

**Table 10. Typical LPC2294/01 peripheral power consumption in active mode**
*Core voltage 1.8 V; $T_{amb}$ = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.*

| Peripheral | CCLK = 12 MHz | CCLK = 48 MHz | CCLK = 60 MHz |
|---|---|---|---|
| Timer0 | 43 | 141 | 184 |
| Timer1 | 46 | 150 | 180 |
| UART0 | 98 | 320 | 398 |
| UART1 | 103 | 351 | 421 |
| PWM0 | 103 | 341 | 407 |
| $I^2C$-bus | 9 | 37 | 53 |
| SPI0/1 | 6 | 27 | 29 |
| RTC | 16 | 55 | 78 |
| PCEMC | 306 | 994 | 1205 |
| ADC | 33 | 128 | 167 |
| CAN1/2/3/4 | 230 | 769 | 912 |

# 9. Dynamic characteristics

**Table 11. Dynamic characteristics**
*$T_{amb}$ = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.*[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **External clock** | | | | | | |
| $f_{osc}$ | oscillator frequency | supplied by an external oscillator (signal generator) | 1 | - | 25 | MHz |
| | | external clock frequency supplied by an external crystal oscillator | 1 | - | 25 | MHz |
| | | external clock frequency if on-chip PLL is used | 10 | - | 25 | MHz |
| | | external clock frequency if on-chip bootloader is used for initial code download | 10 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | 20 | - | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |

**Table 12. External memory interface dynamic characteristics**
$C_L$ = 25 pF; $T_{amb}$ = 40 °C

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Common to read and write cycles** | | | | | | |
| $t_{CHAV}$ | XCLK HIGH to address valid time | | - | - | 10 | ns |
| $t_{CHCSL}$ | XCLK HIGH to $\overline{CS}$ LOW time | | - | - | 10 | ns |
| $t_{CHCSH}$ | XCLK HIGH to $\overline{CS}$ HIGH time | | - | - | 10 | ns |
| $t_{CHANV}$ | XCLK HIGH to address invalid time | | - | - | 10 | ns |
| **Read cycle parameters** | | | | | | |
| $t_{CSLAV}$ | $\overline{CS}$ LOW to address valid time | [1] | −5 | - | +10 | ns |
| $t_{OELAV}$ | $\overline{OE}$ LOW to address valid time | [1] | −5 | - | +10 | ns |
| $t_{CSLOEL}$ | $\overline{CS}$ LOW to $\overline{OE}$ LOW time | | −5 | - | +5 | ns |
| $t_{am}$ | memory access time | [2][3] | $(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$ | - | - | ns |
| $t_{am(ibr)}$ | memory access time (initial burst-ROM) | [2][3] | $(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$ | - | - | ns |
| $t_{am(sbr)}$ | memory access time (subsequent burst-ROM) | [2][4] | $T_{cy(CCLK)} + (-20)$ | - | - | ns |
| $t_{h(D)}$ | data input hold time | [5] | 0 | - | - | ns |
| $t_{CSHOEH}$ | $\overline{CS}$ HIGH to $\overline{OE}$ HIGH time | | −5 | - | +5 | ns |
| $t_{OEHANV}$ | $\overline{OE}$ HIGH to address invalid time | | −5 | - | +5 | ns |
| $t_{CHOEL}$ | XCLK HIGH to $\overline{OE}$ LOW time | | −5 | - | +5 | ns |
| $t_{CHOEH}$ | XCLK HIGH to $\overline{OE}$ HIGH time | | −5 | - | +5 | ns |
| **Write cycle parameters** | | | | | | |
| $t_{AVCSL}$ | address valid to $\overline{CS}$ LOW time | [1] | $T_{cy(CCLK)} - 10$ | - | - | ns |
| $t_{CSLDV}$ | $\overline{CS}$ LOW to data valid time | | −5 | - | +5 | ns |
| $t_{CSLWEL}$ | $\overline{CS}$ LOW to $\overline{WE}$ LOW time | | −5 | - | +5 | ns |
| $t_{CSLBLSL}$ | $\overline{CS}$ LOW to $\overline{BLS}$ LOW time | | −5 | - | +5 | ns |
| $t_{WELDV}$ | $\overline{WE}$ LOW to data valid time | | −5 | - | +5 | ns |
| $t_{CSLDV}$ | $\overline{CS}$ LOW to data valid time | | −5 | - | +5 | ns |
| $t_{WELWEH}$ | $\overline{WE}$ LOW to $\overline{WE}$ HIGH time | [2] | $T_{cy(CCLK)} \times (1 + WST2) - 5$ | - | $T_{cy(CCLK)} \times (1 + WST2) + 5$ | ns |
| $t_{BLSLBLSH}$ | $\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time | [2] | $T_{cy(CCLK)} \times (1 + WST2) - 5$ | - | $T_{cy(CCLK)} \times (1 + WST2) + 5$ | ns |
| $t_{WEHANV}$ | $\overline{WE}$ HIGH to address invalid time | [2] | $T_{cy(CCLK)} - 5$ | - | $T_{cy(CCLK)} + 5$ | ns |
| $t_{WEHDNV}$ | $\overline{WE}$ HIGH to data invalid time | [2] | $(2 \times T_{cy(CCLK)}) - 5$ | - | $(2 \times T_{cy(CCLK)}) + 5$ | ns |
| $t_{BLSHANV}$ | $\overline{BLS}$ HIGH to address invalid time | [2] | $T_{cy(CCLK)} - 5$ | - | $T_{cy(CCLK)} + 5$ | ns |

# 13. Legal information

## 13.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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# 15. Contents





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