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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2294hbd144-01-5

- 16 kB on-chip static RAM and 256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip bootloader software. Single flash sector or full chip erase in 400 ms and programming of 256 B in 1 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software as well as high-speed real-time tracing of instruction execution.
- Two/four (LPC2292/2294) interconnected CAN interfaces with advanced acceptance filters. Additional serial interfaces include two UARTs (16C550), Fast I^2C-bus (400 kbit/s) and two SPIs.
- Eight channel 10-bit ADC with conversion time as low as 2.44 μs.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC), and watchdog.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 112 general purpose I/O pins (5 V tolerant). Up to nine edge/level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2292FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2292FET144/00	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/01	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2

5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/ PWM1	42[2]	L4[2]	O	**TXD0 —** Transmitter output for UART0.
			O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	49[4]	K6[4]	I	**RXD0 —** Receiver input for UART0.
			O	**PWM3 —** Pulse Width Modulator output 3.
			I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/ CAP0[0]	50[5]	L6[5]	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	58[5]	M8[5]	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
			I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	59[2]	L8[2]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	61[2]	N9[2]	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	68[2]	N11[2]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	69[4]	M11[4]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**PWM2 —** Pulse Width Modulator output 2.
			I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4	75[2]	L12[2]	O	**TXD1 —** Transmitter output for UART1.
			O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	76[4]	L13[4]	I	**RXD1 —** Receiver input for UART1.
			O	**PWM6 —** Pulse Width Modulator output 6.
			I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	78[2]	K11[2]	O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	83[2]	J12[2]	I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[12]/DSR1/ MAT1[0]/RD4	84[2]	J13[2]	I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
			I	**RD4 —** CAN4 receiver input (LPC2294 only).
P0[13]/DTR1/ MAT1[1]/TD4	85[2]	H10[2]	O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
			O	**TD4 —** CAN4 transmitter output (LPC2294 only).
P0[14]/DCD1/ EINT1	92[4]	G10[4]	I	**DCD1 —** Data Carrier Detect input for UART1.
			I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/ EINT2	99[4]	E11[4]	I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0[16]/EINT0/ MAT0[2]/ CAP0[2]	100[4]	E10[4]	I	**EINT0 —** External interrupt 0 input.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	101[2]	D13[2]	I	**CAP1[2] —** Capture input for Timer 1, channel 2.
			I/O	**SCK1 —** Serial Clock for SPI1/SSP[3]. SPI clock output from master or input to slave.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	121[2]	D8[2]	I	**CAP1[3] —** Capture input for Timer 1, channel 3.
			I/O	**MISO1 —** Master In Slave Out for SPI1/SSP[3]. Data input to SPI master or data output from SPI slave.
			O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	122[2]	C8[2]	O	**MAT1[2] —** Match output for Timer 1, channel 2.
			I/O	**MOSI1 —** Master Out Slave In for SPI1/SSP[3]. Data output from SPI master or data input to SPI slave.
			I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	123[4]	B8[4]	O	**MAT1[3] —** Match output for Timer 1, channel 3.
			I	**SSEL1 —** Slave Select for SPI1/SSP[3]. Selects the SPI interface as a slave.
			I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ RD3/CAP1[3]	4[2]	C1[2]	O	**PWM5 —** Pulse Width Modulator output 5.
			I	**RD3 —** CAN3 receiver input (LPC2294 only).
			I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/TD3/ CAP0[0]/ MAT0[0]	5[2]	D4[2]	O	**TD3 —** CAN3 transmitter output (LPC2294 only).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]/RD2	6[2]	D3[2]	I	**RD2 —** CAN2 receiver input.
P0[24]/TD2	8[2]	D1[2]	O	**TD2 —** CAN2 transmitter output.
P0[25]/RD1	21[2]	H1[2]	I	**RD1 —** CAN1 receiver input.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[27]/AIN0/ CAP0[1]/ MAT0[1]	23[6]	H3[6]	I	**AIN0 —** ADC, input 0. This analog input is always connected to its pin.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[28]/AIN1/ CAP0[2]/ MAT0[2]	25[6]	J1[6]	I	**AIN1 —** ADC, input 1. This analog input is always connected to its pin.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AIN2/ CAP0[3]/ MAT0[3]	32[6]	L1[6]	I	**AIN2 —** ADC, input 2. This analog input is always connected to its pin.
			I	**CAP0[3] —** Capture input for Timer 0, Channel 3.
			O	**MAT0[3] —** Match output for Timer 0, channel 3.
P0[30]/AIN3/ EINT3/CAP0[0]	33[6]	L2[6]	I	**AIN3 —** ADC, input 3. This analog input is always connected to its pin.
			I	**EINT3 —** External interrupt 3 input.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available.
P1[0]/$\overline{\text{CS0}}$	91[7]	G11[7]	O	**$\overline{\text{CS0}}$ —** LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1[1]/$\overline{\text{OE}}$	90[7]	G13[7]	O	**$\overline{\text{OE}}$ —** LOW-active Output Enable signal.
P1[16]/ TRACEPKT0	34[7]	L3[7]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/ TRACEPKT1	24[7]	H4[7]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/ TRACEPKT2	15[7]	F2[7]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/ TRACEPKT3	7[7]	D2[7]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/ TRACESYNC	102[7]	D12[7]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/ PIPESTAT0	95[7]	F11[7]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/ PIPESTAT1	86[7]	H11[7]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/ PIPESTAT2	82[7]	J11[7]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/ TRACECLK	70[7]	L11[7]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P1[25]/EXTIN0	60[7]	K8[7]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	52[7]	N6[7]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	144[7]	B2[7]	O	**TDO —** Test Data out for JTAG interface.
P1[28]/TDI	140[7]	A3[7]	I	**TDI —** Test Data in for JTAG interface.
P1[29]/TCK	126[7]	A7[7]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	113[7]	D10[7]	I	**TMS —** Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	43[7]	M4[7]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
P2[0] to P2[31]			I/O	**Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2[0]/D0	98[7]	E12[7]	I/O	**D0 —** External memory data line 0.
P2[1]/D1	105[7]	C12[7]	I/O	**D1 —** External memory data line 1.
P2[2]/D2	106[7]	C11[7]	I/O	**D2 —** External memory data line 2.
P2[3]/D3	108[7]	B12[7]	I/O	**D3 —** External memory data line 3.
P2[4]/D4	109[7]	A13[7]	I/O	**D4 —** External memory data line 4.
P2[5]/D5	114[7]	C10[7]	I/O	**D5 —** External memory data line 5.
P2[6]/D6	115[7]	B10[7]	I/O	**D6 —** External memory data line 6.
P2[7]/D7	116[7]	A10[7]	I/O	**D7 —** External memory data line 7.
P2[8]/D8	117[7]	D9[7]	I/O	**D8 —** External memory data line 8.
P2[9]/D9	118[7]	C9[7]	I/O	**D9 —** External memory data line 9.
P2[10]/D10	120[7]	A9[7]	I/O	**D10 —** External memory data line 10.
P2[11]/D11	124[7]	A8[7]	I/O	**D11 —** External memory data line 11.
P2[12]/D12	125[7]	B7[7]	I/O	**D12 —** External memory data line 12.
P2[13]/D13	127[7]	C7[7]	I/O	**D13 —** External memory data line 13.
P2[14]/D14	129[7]	A6[7]	I/O	**D14 —** External memory data line 14.
P2[15]/D15	130[7]	B6[7]	I/O	**D15 —** External memory data line 15.
P2[16]/D16	131[7]	C6[7]	I/O	**D16 —** External memory data line 16.
P2[17]/D17	132[7]	D6[7]	I/O	**D17 —** External memory data line 17.
P2[18]/D18	133[7]	A5[7]	I/O	**D18 —** External memory data line 18.
P2[19]/D19	134[7]	B5[7]	I/O	**D19 —** External memory data line 19.
P2[20]/D20	136[7]	D5[7]	I/O	**D20 —** External memory data line 20.
P2[21]/D21	137[7]	A4[7]	I/O	**D21 —** External memory data line 21.
P2[22]/D22	1[7]	A1[7]	I/O	**D22 —** External memory data line 22.
P2[23]/D23	10[7]	E3[7]	I/O	**D23 —** External memory data line 23.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P2[24]/D24	11[7]	E2[7]	I/O	**D24 —** External memory data line 24.
P2[25]/D25	12[7]	E1[7]	I/O	**D25 —** External memory data line 25.
P2[26]/D26/ BOOT0	13[7]	F4[7]	I/O	**D26 —** External memory data line 26.
			I	**BOOT0 —** While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected.
P2[27]/D27/ BOOT1	16[7]	F1[7]	I/O	**D27 —** External memory data line 27.
			I	**BOOT1 —** While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. BOOT1:0 = 00 selects 8-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 01 selects 16-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 10 selects 32-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 11 selects internal flash memory.
P2[28]/D28	17[7]	G2[7]	I/O	**D28 —** External memory data line 28.
P2[29]/D29	18[7]	G1[7]	I/O	**D29 —** External memory data line 29.
P2[30]/D30/ AIN4	19[6]	G3[6]	I/O	**D30 —** External memory data line 30.
			I	**AIN4 —** ADC, input 4. This analog input is always connected to its pin.
P2[31]/D31/ AIN5	20[6]	G4[6]	I/O	**D31 —** External memory data line 31.
			I	**AIN5 —** ADC, input 5. This analog input is always connected to its pin.
P3[0] to P3[31]			I/O	**Port 3 —** Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3[0]/A0	89[7]	G12[7]	O	**A0 —** External memory address line 0.
P3[1]/A1	88[7]	H13[7]	O	**A1 —** External memory address line 1.
P3[2]/A2	87[7]	H12[7]	O	**A2 —** External memory address line 2.
P3[3]/A3	81[7]	J10[7]	O	**A3 —** External memory address line 3.
P3[4]/A4	80[7]	K13[7]	O	**A4 —** External memory address line 4.
P3[5]/A5	74[7]	M13[7]	O	**A5 —** External memory address line 5.
P3[6]/A6	73[7]	N13[7]	O	**A6 —** External memory address line 6.
P3[7]/A7	72[7]	M12[7]	O	**A7 —** External memory address line 7.
P3[8]/A8	71[7]	N12[7]	O	**A8 —** External memory address line 8.
P3[9]/A9	66[7]	M10[7]	O	**A9 —** External memory address line 9.
P3[10]/A10	65[7]	N10[7]	O	**A10 —** External memory address line 10.
P3[11]/A11	64[7]	K9[7]	O	**A11 —** External memory address line 11.
P3[12]/A12	63[7]	L9[7]	O	**A12 —** External memory address line 12.
P3[13]/A13	62[7]	M9[7]	O	**A13 —** External memory address line 13.
P3[14]/A14	56[7]	K7[7]	O	**A14 —** External memory address line 14.
P3[15]/A15	55[7]	L7[7]	O	**A15 —** External memory address line 15.
P3[16]/A16	53[7]	M7[7]	O	**A16 —** External memory address line 16.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P3[17]/A17	48[7]	N5[7]	O	**A17 —** External memory address line 17.
P3[18]/A18	47[7]	M5[7]	O	**A18 —** External memory address line 18.
P3[19]/A19	46[7]	L5[7]	O	**A19 —** External memory address line 19.
P3[20]/A20	45[7]	K5[7]	O	**A20 —** External memory address line 20.
P3[21]/A21	44[7]	N4[7]	O	**A21 —** External memory address line 21.
P3[22]/A22	41[7]	K4[7]	O	**A22 —** External memory address line 22.
P3[23]/A23/ XCLK	40[7]	N3[7]	I/O	**A23 —** External memory address line 23.
			O	**XCLK —** Clock output.
P3[24]/$\overline{CS3}$	36[7]	M2[7]	O	**$\overline{CS3}$ —** LOW-active Chip Select 3 signal. (Bank 3 addresses range 0x8300 0000 to 0x83FF FFFF)
P3[25]/$\overline{CS2}$	35[7]	M1[7]	O	**$\overline{CS2}$ —** LOW-active Chip Select 2 signal. (Bank 2 addresses range 0x8200 0000 to 0x82FF FFFF)
P3[26]/$\overline{CS1}$	30[7]	K2[7]	O	**$\overline{CS1}$ —** LOW-active Chip Select 1 signal. (Bank 1 addresses range 0x8100 0000 to 0x81FF FFFF)
P3[27]/$\overline{WE}$	29[7]	K1[7]	O	**$\overline{WE}$ —** LOW-active Write enable signal.
P3[28]/$\overline{BLS3}$/ AIN7	28[6]	J4[6]	O	**$\overline{BLS3}$ —** LOW-active Byte Lane Select signal (Bank 3).
			I	**AIN7 —** ADC, input 7. This analog input is always connected to its pin.
P3[29]/$\overline{BLS2}$/ AIN6	27[6]	J3[6]	O	**$\overline{BLS2}$ —** LOW-active Byte Lane Select signal (Bank 2).
			I	**AIN6 —** ADC, input 6. This analog input is always connected to its pin.
P3[30]/$\overline{BLS1}$	97[7]	E13[7]	O	**$\overline{BLS1}$ —** LOW-active Byte Lane Select signal (Bank 1).
P3[31]/$\overline{BLS0}$	96[7]	F10[7]	O	**$\overline{BLS0}$ —** LOW-active Byte Lane Select signal (Bank 0).
TD1	22[7]	H2[7]	O	**TD1:** CAN1 transmitter output.
$\overline{RESET}$	135[8]	C5[8]	I	**External Reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142[9]	C3[9]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	141[9]	B3[9]	O	Output from the oscillator amplifier.
V_{SS}	3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128	C2, E4, J2, N2, N7, L10, K12, F13, D11, B13, B11, D7	I	**Ground:** 0 V reference.
V_{SSA}	139	C4	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{SSA(PLL)}$	138	B4	I	**PLL analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(1V8)}$	37, 110	N1, A12	I	**1.8 V core power supply:** This is the power supply voltage for internal circuitry.

6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 5 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 5. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register Empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Auto-baud time-out (ABTO)[1]End of auto-baud (ABEO)[1]	6

receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2292/2294 supports bit rate up to 400 kbit/s (Fast I^2C-bus).

6.12.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2292/2294 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.13.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $\frac{1}{8}$ of the input clock rate.

6.13.2 Features available in LPC2292/2294/01 only

- Eight to 16 bits per frame.
- When the SPI interface is used in Master mode, the SSELn pin is not needed (can be used for a different function).

6.15.2 Features available in LPC2292/2294/01 only

The LPC2292/2294/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to PCLK / 4. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than 1 / (2PCLK).

6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.

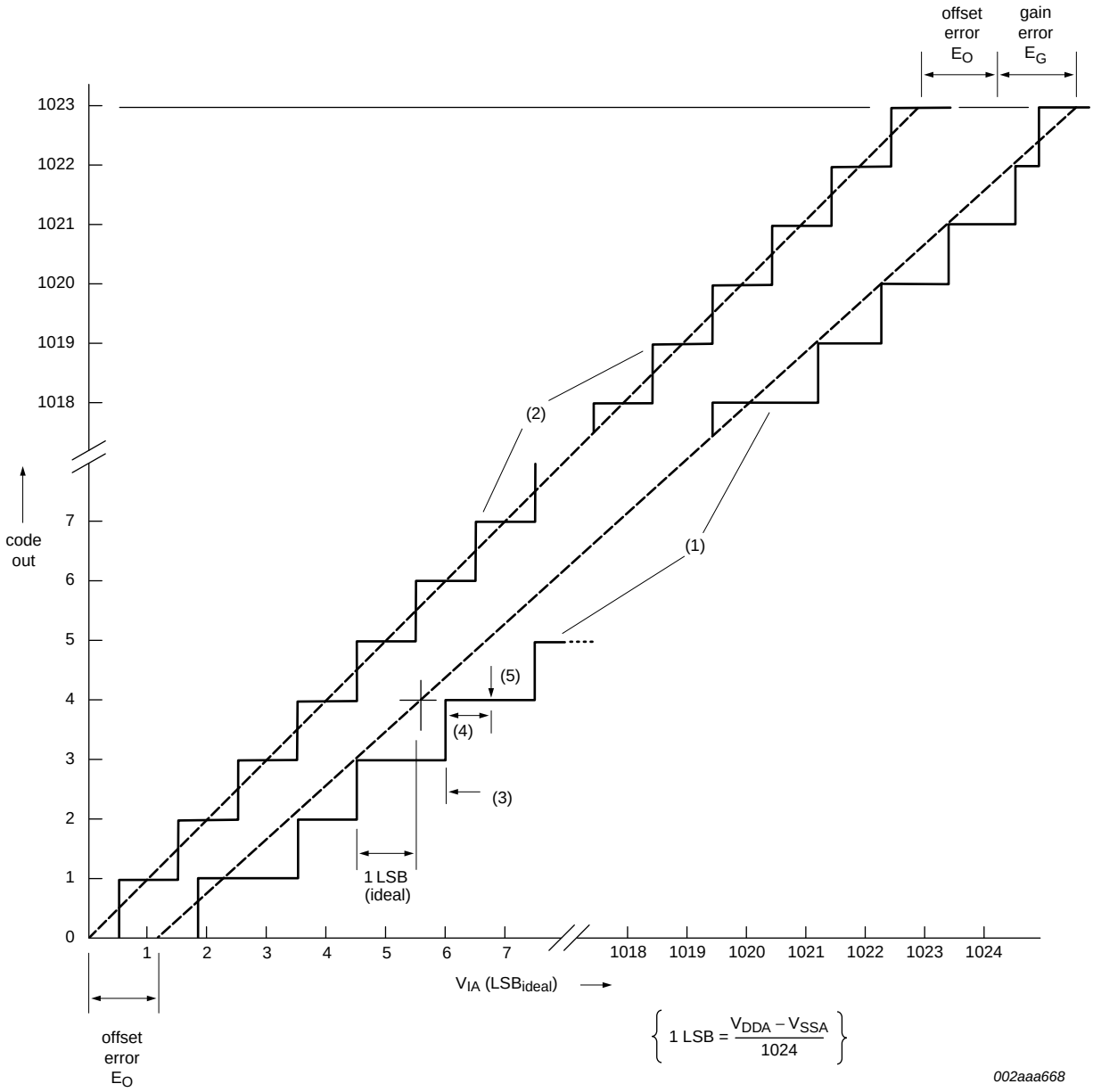
6.20.2 Embedded trace

Since the LPC2292/2294 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.20.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the Debug Communications Channel (DCC), which is present in the EmbeddedICE logic. The LPC2292/2294 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.



(1) Example of an actual transfer curve.

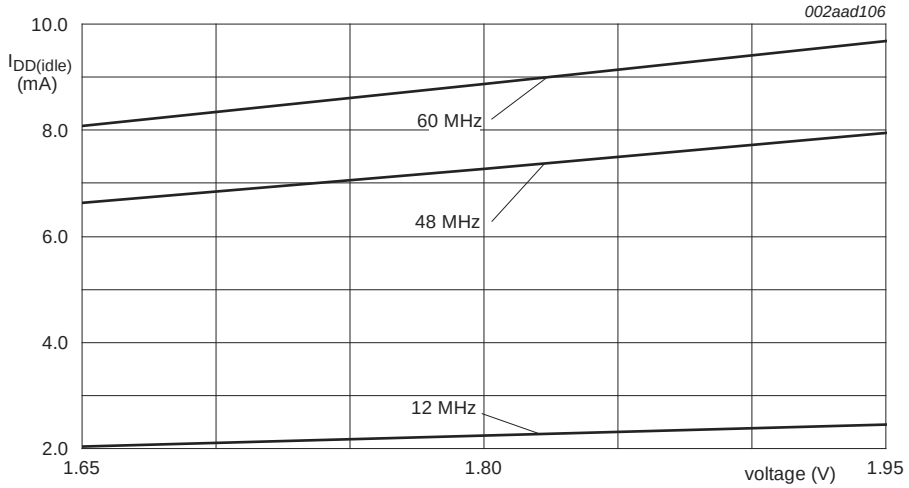
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

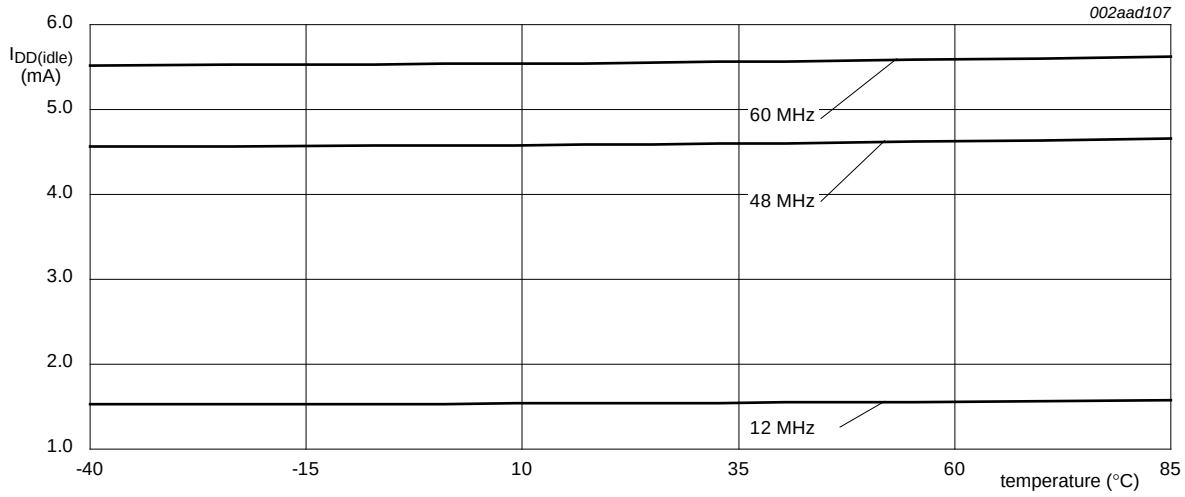
(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics



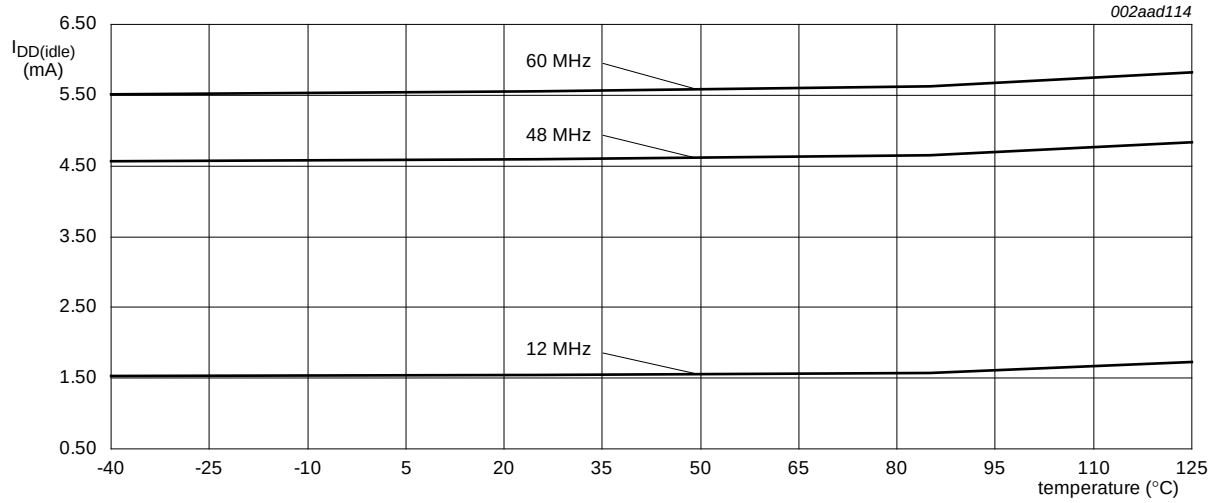
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 10. Typical LPC2292/01 $I_{DD(idle)}$ measured at different core voltages



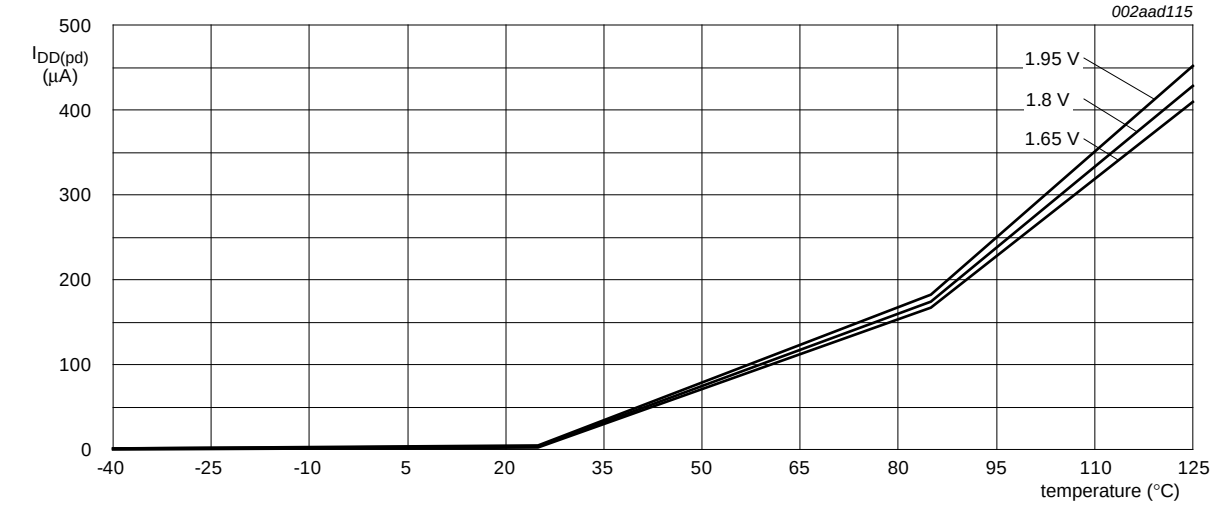
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Core voltage 1.8 V; all peripherals disabled.

Fig 11. Typical LPC2292/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 18. Typical LPC2294/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 19. Typical LPC2294/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 11. Dynamic characteristics *...continued*
T_{amb} = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.1 Timing

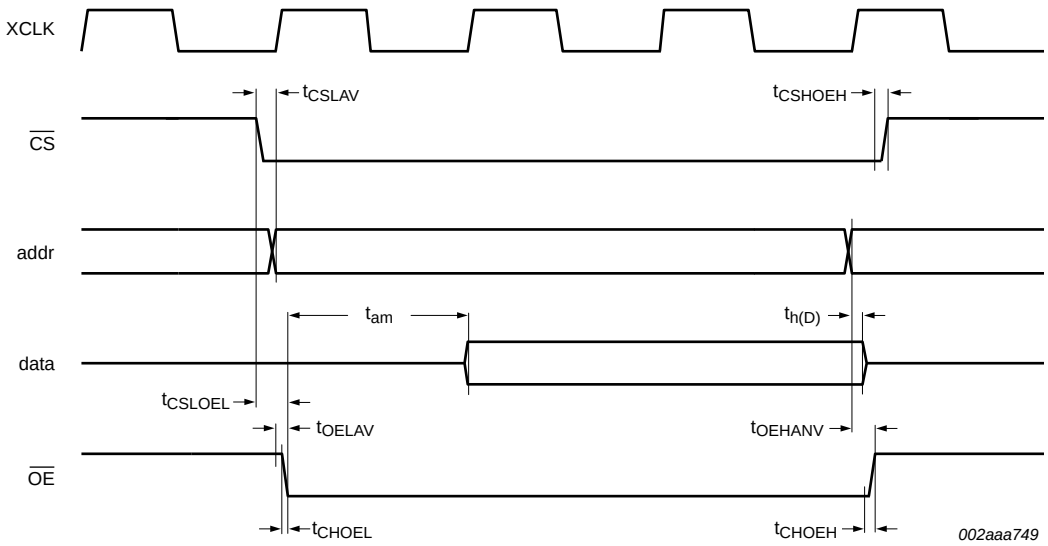


Fig 22. External memory read access

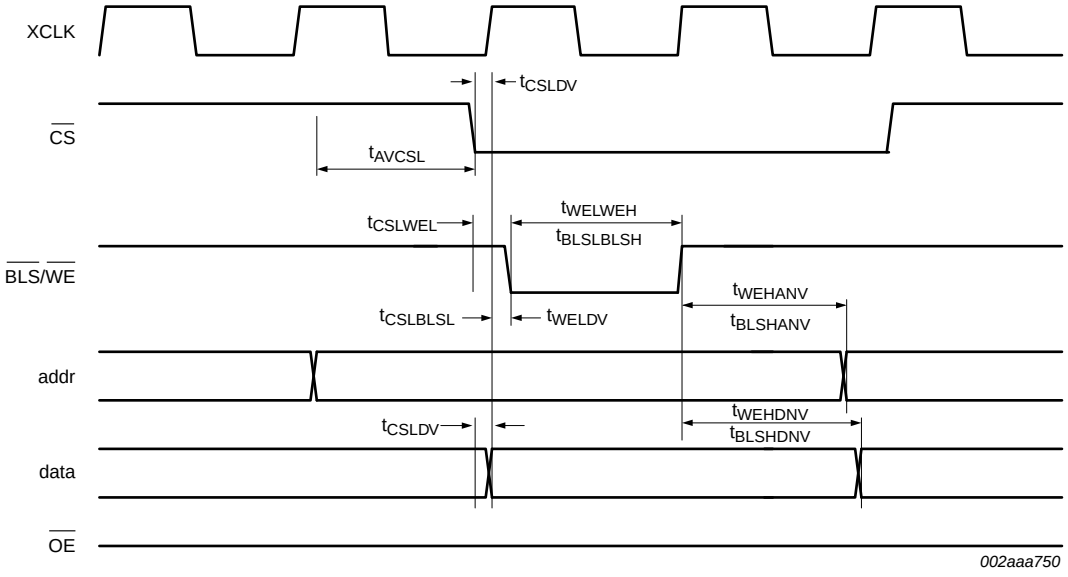
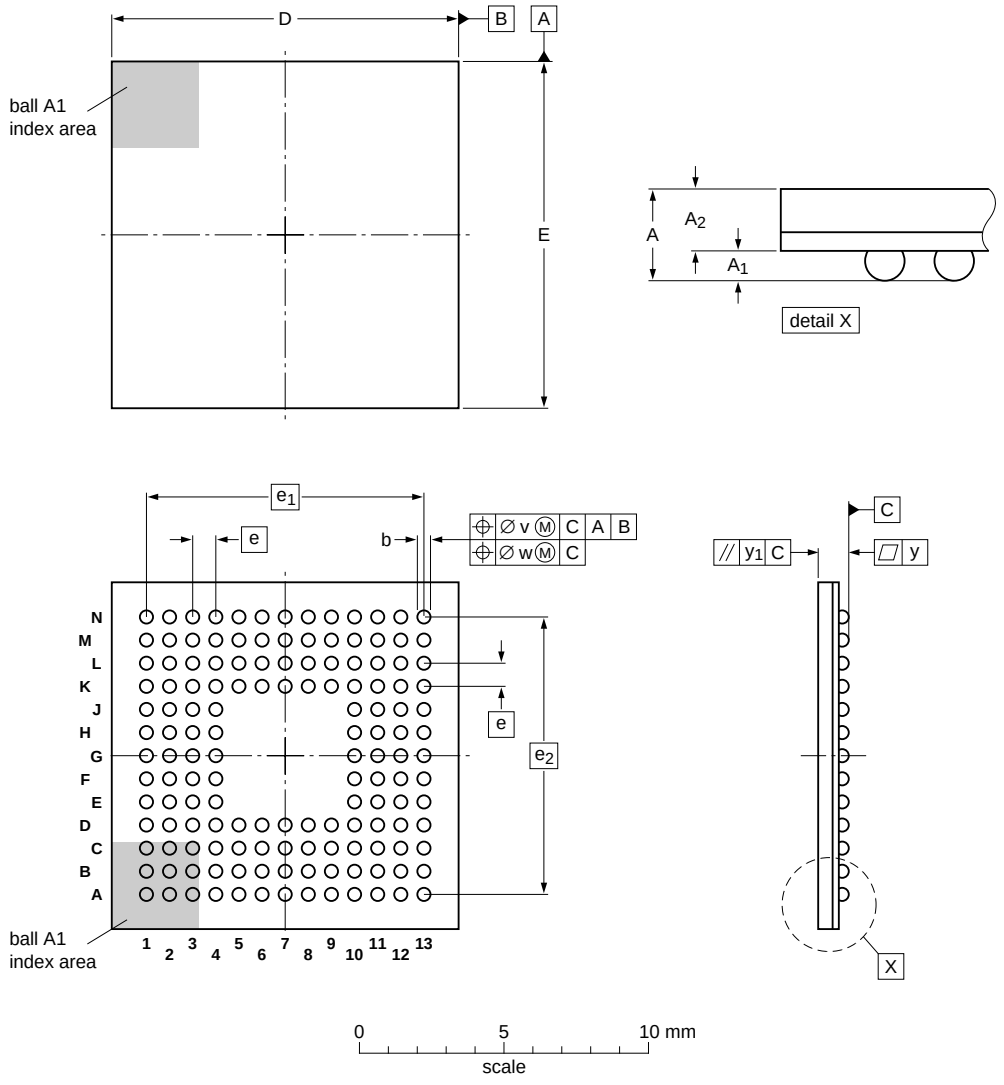


Fig 23. External memory write access

TFBGA144: plastic thin fine-pitch ball grid array package; 144 balls **SOT569-2**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	9.6	9.6	0.15	0.05	0.1	0.08
	nom	1.05	0.35	0.70	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT569-2						~~08-01-29~~ 08-03-14

Fig 26. Package outline SOT569-2 (TFBGA144)

11. Abbreviations

Table 14. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CISC	Complex Instruction Set Computer
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I/O	Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RISC	Reduced Instruction Set Computer
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

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14. Contact information

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